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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (Tj)
Mounting Type	Surface Mount
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064zc-5mn132i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064zc-5mn132i</a>

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage ( $V_{CC}$ )	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage ( $V_{CCO}$ )	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied <sup>4, 5</sup>	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature ( $T_j$ ) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of ( $V_{IH}$  (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with  $V_{IN} > 3.6V$  is allowed.

### Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6 <sup>1, 2</sup>	1.9	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V	
	Supply Voltage for 3.3V Devices	3.0	3.6	V	
$T_j$	Junction Temperature (Commercial)	0	90	C	
	Junction Temperature (Industrial)	-40	105	C	
	Junction Temperature (Extended)	-40	130	C	

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

### Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

### Hot Socketing Characteristics<sup>1,2,3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DK}$	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$	—	±30	±200	µA

1. Insensitive to sequence of  $V_{CC}$  or  $V_{CCO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCO}$ , provided  $(V_{IN} - V_{CCO}) \leq 3.6V$ .
2.  $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}, I_{PD}$  or  $I_{BH}$ . Device defaults to pull-up until fuse circuitry is active.

## Supply Current, ispMACH 4000V/B/C

## Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4032V/B/C</b>						
ICC <sup>1,2,3</sup>	Operating Power Supply Current	V <sub>CC</sub> = 3.3V	—	11.8	—	mA
		V <sub>CC</sub> = 2.5V	—	11.8	—	mA
		V <sub>CC</sub> = 1.8V	—	1.8	—	mA
ICC <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	11.3	—	mA
		V <sub>CC</sub> = 2.5V	—	11.3	—	mA
		V <sub>CC</sub> = 1.8V	—	1.3	—	mA
<b>ispMACH 4064V/B/C</b>						
ICC <sup>1,2,3</sup>	Operating Power Supply Current	V <sub>CC</sub> = 3.3V	—	12	—	mA
		V <sub>CC</sub> = 2.5V	—	12	—	mA
		V <sub>CC</sub> = 1.8V	—	2	—	mA
ICC <sup>5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	11.5	—	mA
		V <sub>CC</sub> = 2.5V	—	11.5	—	mA
		V <sub>CC</sub> = 1.8V	—	1.5	—	mA
<b>ispMACH 4128V/B/C</b>						
ICC <sup>1,2,3</sup>	Operating Power Supply Current	V <sub>CC</sub> = 3.3V	—	12	—	mA
		V <sub>CC</sub> = 2.5V	—	12	—	mA
		V <sub>CC</sub> = 1.8V	—	2	—	mA
ICC <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	11.5	—	mA
		V <sub>CC</sub> = 2.5V	—	11.5	—	mA
		V <sub>CC</sub> = 1.8V	—	1.5	—	mA
<b>ispMACH 4256V/B/C</b>						
I <sub>CC</sub> <sup>1,2,3</sup>	Operating Power Supply Current	V <sub>CC</sub> = 3.3V	—	12.5	—	mA
		V <sub>CC</sub> = 2.5V	—	12.5	—	mA
		V <sub>CC</sub> = 1.8V	—	2.5	—	mA
I <sub>CC</sub> <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	12	—	mA
		V <sub>CC</sub> = 2.5V	—	12	—	mA
		V <sub>CC</sub> = 1.8V	—	2	—	mA
<b>ispMACH 4384V/B/C</b>						
I <sub>CC</sub> <sup>1,2,3</sup>	Operating Power Supply Current	V <sub>CC</sub> = 3.3V	—	13.5	—	mA
		V <sub>CC</sub> = 2.5V	—	13.5	—	mA
		V <sub>CC</sub> = 1.8V	—	3.5	—	mA
I <sub>CC</sub> <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	12.5	—	mA
		V <sub>CC</sub> = 2.5V	—	12.5	—	mA
		V <sub>CC</sub> = 1.8V	—	2.5	—	mA
<b>ispMACH 4512V/B/C</b>						
I <sub>CC</sub> <sup>1,2,3</sup>	Operating Power Supply Current	V <sub>CC</sub> = 3.3V	—	14	—	mA
		V <sub>CC</sub> = 2.5V	—	14	—	mA
		V <sub>CC</sub> = 1.8V	—	4	—	mA

### Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I <sub>CC</sub> <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	13	—	mA
		V <sub>CC</sub> = 2.5V	—	13	—	mA
		V <sub>CC</sub> = 1.8V	—	3	—	mA

1. T<sub>A</sub> = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I<sub>CC</sub> varies with specific device configuration and operating frequency.
4. T<sub>A</sub> = 25°C

### Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4032ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	50	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	58	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	60	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	70	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	10	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	13	20	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	15	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	22	—	μA
<b>ispMACH 4064ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	80	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	89	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	92	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	109	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	11	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	15	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	18	35	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	37	—	μA
<b>ispMACH 4128ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	168	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	190	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	195	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	212	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	12	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	16	35	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	19	50	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	42	—	μA



## ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
t <sub>S</sub>	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
t <sub>R</sub>	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
t <sub>RW</sub>	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
t <sub>G<sub>P</sub>TOE/DIS</sub>	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
t <sub>G<sub>O</sub>E/DIS</sub>	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
t <sub>CW</sub>	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
f <sub>MAX</sub> (Ext.)	clock frequency with external feedback, [1 / (t <sub>S</sub> + t <sub>CO</sub> )]	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

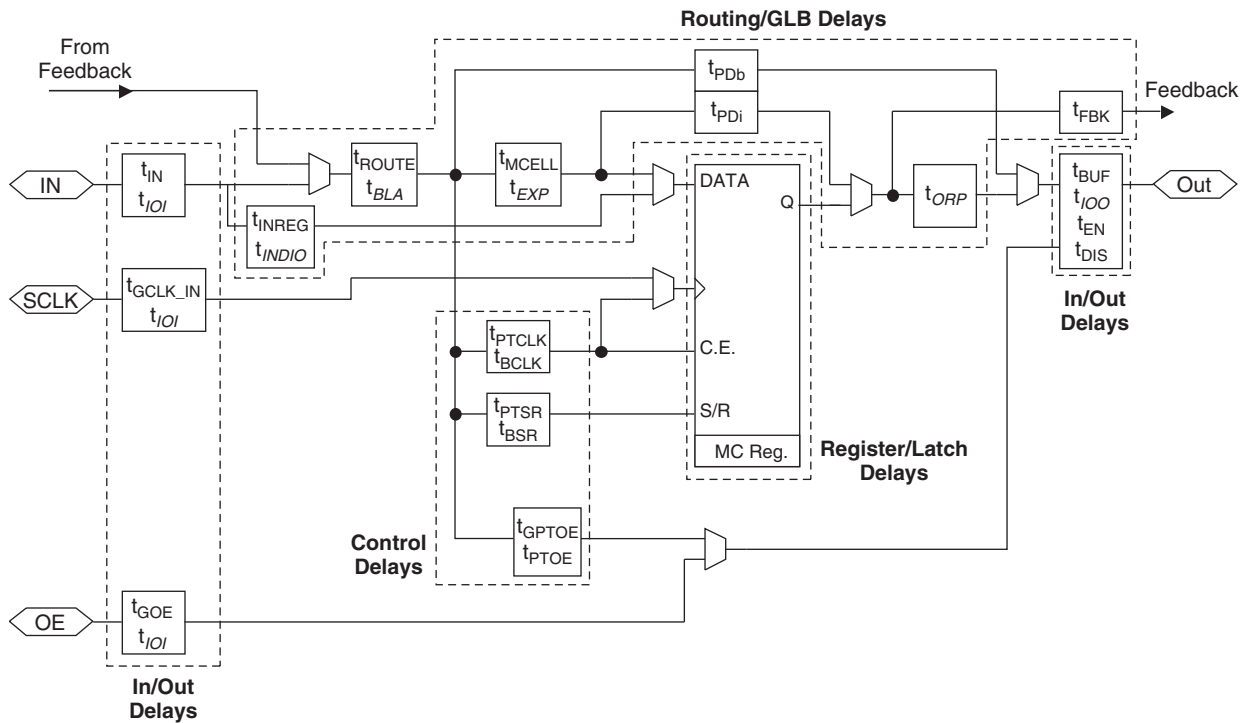
3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

## Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#).

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

**ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>GP</sub> TOE	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
t <sub>P</sub> TOE	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.



**ispMACH 4000V/B/C Timing Adders<sup>1</sup> (Cont.)**

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.00	—	1.00	—	1.00	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

**ispMACH 4000Z Timing Adders <sup>1</sup>**

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.00	—	1.00	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing. Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

**ispMACH 4000Z Timing Adders (Cont.)<sup>1</sup>**

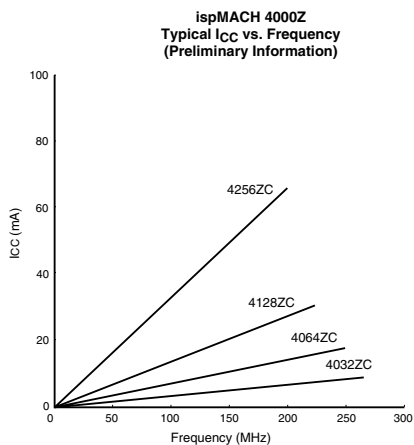
Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.30	—	1.30	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

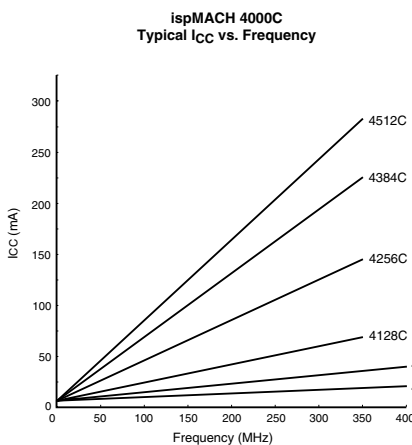
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

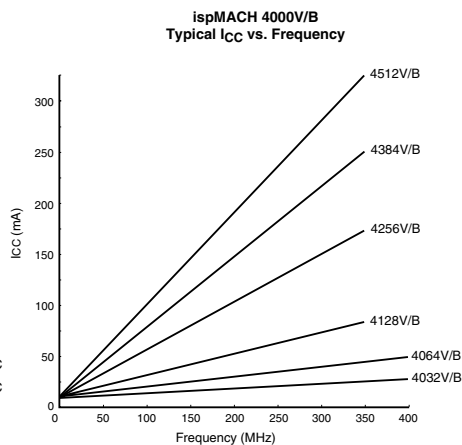
## Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

## Power Estimation Coefficients<sup>1</sup>

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:  
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B <sup>10</sup>	D4	D <sup>2</sup>	D10	D <sup>5</sup>
34	1	B11	B <sup>11</sup>	D6	D <sup>3</sup>	D8	D <sup>4</sup>
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B <sup>12</sup>	D8	D <sup>4</sup>	D6	D <sup>3</sup>
39	1	B13	B <sup>13</sup>	D10	D <sup>5</sup>	D4	D <sup>2</sup>
40	1	B14	B <sup>14</sup>	D12	D <sup>6</sup>	D2	D <sup>1</sup>
41	1	B15/GOE1	B <sup>15</sup>	D14/GOE1	D <sup>7</sup>	D0/GOE1	D <sup>0</sup>
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>
45	0	A1	A <sup>1</sup>	A2	A <sup>1</sup>	A1	A <sup>1</sup>
46	0	A2	A <sup>2</sup>	A4	A <sup>2</sup>	A2	A <sup>2</sup>
47	0	A3	A <sup>3</sup>	A6	A <sup>3</sup>	A4	A <sup>3</sup>
48	0	A4	A <sup>4</sup>	A8	A <sup>4</sup>	A6	A <sup>4</sup>

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A <sup>5</sup>	A8	A <sup>5</sup>
C1	0	A6	A <sup>6</sup>	A10	A <sup>6</sup>
D1	0	A7	A <sup>7</sup>	A11	A <sup>7</sup>
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
E1	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A <sup>8</sup>	B15	B <sup>7</sup>
G3	0	A9	A <sup>9</sup>	B12	B <sup>6</sup>
G1	0	A10	A <sup>10</sup>	B10	B <sup>5</sup>
H1	0	A11	A <sup>11</sup>	B8	B <sup>4</sup>
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC <sup>1</sup>	-	I <sup>1</sup>	-
K4	0	A12	A <sup>12</sup>	B6	B <sup>3</sup>
H4	0	A13	A <sup>13</sup>	B4	B <sup>2</sup>
H5	0	A14	A <sup>14</sup>	B2	B <sup>1</sup>

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C^1	E2	E^1	I6	I^1
43	1	C2	C^2	E4	E^2	I10	I^2
44	1	C3	C^3	E6	E^3	I12	I^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4	J2	J^0
48	1	C5	C^5	E10	E^5	J6	J^1
49	1	C6	C^6	E12	E^6	J10	J^2
50	1	C7	C^7	E14	E^7	J12	J^3
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0	K12	K^3
54	1	C9	C^9	F2	F^1	K10	K^2
55	1	C10	C^10	F4	F^2	K6	K^1
56	1	C11	C^11	F6	F^3	K2	K^0
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4	L12	L^3
59	1	C13	C^13	F10	F^5	L10	L^2
60	1	C14	C^14	F12	F^6	L6	L^1
61	1	C15	C^15	F13	F^7	L4	L^0
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7	M4	M^0
65	1	D14	D^14	G12	G^6	M6	M^1
66	1	D13	D^13	G10	G^5	M10	M^2
67	1	D12	D^12	G8	G^4	M12	M^3
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3	N2	N^0
70	1	D10	D^10	G5	G^2	N6	N^1
71	1	D9	D^9	G4	G^1	N10	N^2
72	1	D8	D^8	G2	G^0	N12	N^3
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D^7	H13	H^7	O12	O^3
79	1	D6	D^6	H12	H^6	O10	O^2
80	1	D5	D^5	H10	H^5	O6	O^1
81	1	D4	D^4	H8	H^4	O2	O^0
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

**ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F <sup>9</sup>	L8	L <sup>4</sup>
87	1	F13	F <sup>10</sup>	L6	L <sup>3</sup>
88	1	F14	F <sup>11</sup>	L4	L <sup>2</sup>
89	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
90	1	GND (Bank 1) <sup>1</sup>	-	NC <sup>1</sup>	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
93	1	G14	G <sup>11</sup>	M2	M <sup>1</sup>
94	1	G13	G <sup>10</sup>	M4	M <sup>2</sup>
95	1	G12	G <sup>9</sup>	M6	M <sup>3</sup>
96	1	G10	G <sup>8</sup>	M8	M <sup>4</sup>
97	1	G9	G <sup>7</sup>	M10	M <sup>5</sup>
98	1	G8	G <sup>6</sup>	M12	M <sup>6</sup>
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G <sup>5</sup>	N2	N <sup>1</sup>
101	1	G5	G <sup>4</sup>	N4	N <sup>2</sup>
102	1	G4	G <sup>3</sup>	N6	N <sup>3</sup>
103	1	G2	G <sup>2</sup>	N8	N <sup>4</sup>
104	1	G1	G <sup>1</sup>	N10	N <sup>5</sup>
105	1	G0	G <sup>0</sup>	N12	N <sup>6</sup>
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
111	1	H14	H <sup>11</sup>	O12	O <sup>6</sup>
112	1	H13	H <sup>10</sup>	O10	O <sup>5</sup>
113	1	H12	H <sup>9</sup>	O8	O <sup>4</sup>
114	1	H10	H <sup>8</sup>	O6	O <sup>3</sup>
115	1	H9	H <sup>7</sup>	O4	O <sup>2</sup>
116	1	H8	H <sup>6</sup>	O2	O <sup>1</sup>
117	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H <sup>5</sup>	P12	P <sup>6</sup>
121	1	H5	H <sup>4</sup>	P10	P <sup>5</sup>
122	1	H4	H <sup>3</sup>	P8	P <sup>4</sup>
123	1	H2	H <sup>2</sup>	P6	P <sup>3</sup>
124	1	H1	H <sup>1</sup>	P4	P <sup>2</sup>
125	1	H0/GOE1	H <sup>0</sup>	P2/GOE1	P <sup>1</sup>
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
142	1	O0	O <sup>0</sup>	GX0	GX <sup>0</sup>	OX0	OX <sup>0</sup>
143	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
145	1	P14	P <sup>7</sup>	HX14	HX <sup>7</sup>	PX14	PX <sup>7</sup>
146	1	P12	P <sup>6</sup>	HX12	HX <sup>6</sup>	PX12	PX <sup>6</sup>
147	1	P10	P <sup>5</sup>	HX10	HX <sup>5</sup>	PX10	PX <sup>5</sup>
148	1	P8	P <sup>4</sup>	HX8	HX <sup>4</sup>	PX8	PX <sup>4</sup>
149	1	P6	P <sup>3</sup>	HX6	HX <sup>3</sup>	PX6	PX <sup>3</sup>
150	1	P4	P <sup>2</sup>	HX4	HX <sup>2</sup>	PX4	PX <sup>2</sup>
151	1	P2/GOE1	P <sup>1</sup>	HX2/GOE1	HX <sup>1</sup>	PX2/GOE1	PX <sup>1</sup>
152	1	P0	P <sup>0</sup>	HX0	HX <sup>0</sup>	PX0	PX <sup>0</sup>
153	-	GND	-	GND	-	GND	-
154	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
155	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
156	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
157	-	VCC	-	VCC	-	VCC	-
158	0	A0	A <sup>0</sup>	A0	A <sup>0</sup>	A0	A <sup>0</sup>
159	0	A2/GOE0	A <sup>1</sup>	A2/GOE0	A <sup>1</sup>	A2/GOE0	A <sup>1</sup>
160	0	A4	A <sup>2</sup>	A4	A <sup>2</sup>	A4	A <sup>2</sup>
161	0	A6	A <sup>3</sup>	A6	A <sup>3</sup>	A6	A <sup>3</sup>
162	0	A8	A <sup>4</sup>	A8	A <sup>4</sup>	A8	A <sup>4</sup>
163	0	A10	A <sup>5</sup>	A10	A <sup>5</sup>	A10	A <sup>5</sup>
164	0	A12	A <sup>6</sup>	A12	A <sup>6</sup>	A12	A <sup>6</sup>
165	0	A14	A <sup>7</sup>	A14	A <sup>7</sup>	A14	A <sup>7</sup>
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
167	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
168	0	B0	B <sup>0</sup>	B0	B <sup>0</sup>	B0	B <sup>0</sup>
169	0	B2	B <sup>1</sup>	B2	B <sup>1</sup>	B2	B <sup>1</sup>
170	0	B4	B <sup>2</sup>	B4	B <sup>2</sup>	B4	B <sup>2</sup>
171	0	B6	B <sup>3</sup>	B6	B <sup>3</sup>	B6	B <sup>3</sup>
172	0	B8	B <sup>4</sup>	B8	B <sup>4</sup>	B8	B <sup>4</sup>
173	0	B10	B <sup>5</sup>	B10	B <sup>5</sup>	B10	B <sup>5</sup>
174	0	B12	B <sup>6</sup>	B12	B <sup>6</sup>	B12	B <sup>6</sup>
175	0	B14	B <sup>7</sup>	B14	B <sup>7</sup>	B14	B <sup>7</sup>
176	-	VCC	-	VCC	-	VCC	-



**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J^5	J10	J^7	N10	N^5	BX10	BX^5
P13	1	J12	J^6	J12	J^8	N12	N^6	BX12	BX^6
N13	1	J14	J^7	J14	J^9	N14	N^7	BX14	BX^7
M12	1	NC	-	NC	-	P4	P^2	FX0	FX^0
T15	1	NC	-	NC	-	P6	P^3	FX2	FX^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX^2
R16	1	NC	-	NC	-	P8	P^4	FX6	FX^3
N14	1	NC	-	NC	-	P10	P^5	FX8	FX^4
P15	1	K14	K^7	K14	K^9	O14	O^7	CX14	CX^7
L11	1	K12	K^6	K12	K^8	O12	O^6	CX12	CX^6
P16	1	K10	K^5	K10	K^7	O10	O^5	CX10	CX^5
K11	1	K8	K^4	K9	K^6	O8	O^4	CX8	CX^4
M14	1	K6	K^3	K8	K^5	O6	O^3	CX6	CX^3
K12	1	K4	K^2	K6	K^4	O4	O^2	CX4	CX^2
N15	1	K2	K^1	K4	K^3	O2	O^1	CX2	CX^1
N16	1	K0	K^0	K2	K^2	O0	O^0	CX0	CX^0
M15	1	NC	-	K1	K^1	BX6	BX^3	HX0	HX^0
M13	1	NC	-	K0	K^0	BX4	BX^2	HX4	HX^1
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX^5
L15	1	NC	-	NC	-	P12	P^6	FX12	FX^6
L16	1	NC	-	NC	-	P14	P^7	FX14	FX^7
J11	1	NC	-	L14	L^9	BX2	BX^1	HX8	HX^2
K15	1	NC	-	L12	L^8	BX0	BX^0	HX12	HX^3
J12	1	L14	L^7	L10	L^7	AX14	AX^7	GX14	GX^7
K13	1	L12	L^6	L9	L^6	AX12	AX^6	GX12	GX^6
K14	1	L10	L^5	L8	L^5	AX10	AX^5	GX10	GX^5
K16	1	L8	L^4	L6	L^4	AX8	AX^4	GX8	GX^4
J16	1	L6	L^3	L4	L^3	AX6	AX^3	GX6	GX^3
J15	1	L4	L^2	L2	L^2	AX4	AX^2	GX4	GX^2
H16	1	L2	L^1	L1	L^1	AX2	AX^1	GX2	GX^1
J13	1	L0	L^0	L0	L^0	AX0	AX^0	GX0	GX^0
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M^0	M0	M^0	DX0	DX^0	JX0	JX^0

## ispMACH 4000C (1.8V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92	C
	LC4128C-5T128C	128	1.8	5	TQFP	128	92	C
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92	C
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64	C
	LC4128C-5T100C	128	1.8	5	TQFP	100	64	C
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256C	LC4256C-3FT256AC	256	1.8	3	ftBGA	256	128	C
	LC4256C-5FT256AC	256	1.8	5	ftBGA	256	128	C
	LC4256C-75FT256AC	256	1.8	7.5	ftBGA	256	128	C
	LC4256C-3FT256BC	256	1.8	3	ftBGA	256	160	C
	LC4256C-5FT256BC	256	1.8	5	ftBGA	256	160	C
	LC4256C-75FT256BC	256	1.8	7.5	ftBGA	256	160	C
	LC4256C-3F256AC <sup>1</sup>	256	1.8	3	fpBGA	256	128	C
	LC4256C-5F256AC <sup>1</sup>	256	1.8	5	fpBGA	256	128	C
	LC4256C-75F256AC <sup>1</sup>	256	1.8	7.5	fpBGA	256	128	C
	LC4256C-3F256BC <sup>1</sup>	256	1.8	3	fpBGA	256	160	C
	LC4256C-5F256BC <sup>1</sup>	256	1.8	5	fpBGA	256	160	C
	LC4256C-75F256BC <sup>1</sup>	256	1.8	7.5	fpBGA	256	160	C
	LC4256C-3T176C	256	1.8	3	TQFP	176	128	C
	LC4256C-5T176C	256	1.8	5	TQFP	176	128	C
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256C-3T100C	256	1.8	3	TQFP	100	64	C
LC4256C-5T100C	256	1.8	5	TQFP	100	64	C	
LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C	
LC4384C	LC4384C-35FT256C	384	1.8	3.5	ftBGA	256	192	C
	LC4384C-5FT256C	384	1.8	5	ftBGA	256	192	C
	LC4384C-75FT256C	384	1.8	7.5	ftBGA	256	192	C
	LC4384C-35F256C <sup>1</sup>	384	1.8	3.5	fpBGA	256	192	C
	LC4384C-5F256C <sup>1</sup>	384	1.8	5	fpBGA	256	192	C
	LC4384C-75F256C <sup>1</sup>	384	1.8	7.5	fpBGA	256	192	C
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128	C
	LC4384C-5T176C	384	1.8	5	TQFP	176	128	C
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128	C
LC4512C	LC4512C-35FT256C	512	1.8	3.5	ftBGA	256	208	C
	LC4512C-5FT256C	512	1.8	5	ftBGA	256	208	C
	LC4512C-75FT256C	512	1.8	7.5	ftBGA	256	208	C
	LC4512C-35F256C <sup>1</sup>	512	1.8	3.5	fpBGA	256	208	C
	LC4512C-5F256C <sup>1</sup>	512	1.8	5	fpBGA	256	208	C
	LC4512C-75F256C <sup>1</sup>	512	1.8	7.5	fpBGA	256	208	C
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
	LC4512C-5T176C	512	1.8	5	TQFP	176	128	C
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000C (1.8V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032C-75T48I	32	1.8	7.5	TQFP	48	32	I
	LC4032C-10T48I	32	1.8	10	TQFP	48	32	I
	LC4032C-5T44I	32	1.8	5	TQFP	44	30	I
	LC4032C-75T44I	32	1.8	7.5	TQFP	44	30	I
	LC4032C-10T44I	32	1.8	10	TQFP	44	30	I
LC4064C	LC4064C-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064C-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064C-10T100I	64	1.8	10	TQFP	100	64	I
	LC4064C-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064C-75T48I	64	1.8	7.5	TQFP	48	32	I
	LC4064C-10T48I	64	1.8	10	TQFP	48	32	I
	LC4064C-5T44I	64	1.8	5	TQFP	44	30	I
	LC4064C-75T44I	64	1.8	7.5	TQFP	44	30	I
LC4128C	LC4128C-5T128I	128	1.8	5	TQFP	128	92	I
	LC4128C-75T128I	128	1.8	7.5	TQFP	128	92	I
	LC4128C-10T128I	128	1.8	10	TQFP	128	92	I
	LC4128C-5T100I	128	1.8	5	TQFP	100	64	I
	LC4128C-75T100I	128	1.8	7.5	TQFP	100	64	I
	LC4128C-10T100I	128	1.8	10	TQFP	100	64	I
LC4256C	LC4256C-5FT256AI	256	1.8	5	ftBGA	256	128	I
	LC4256C-75FT256AI	256	1.8	7.5	ftBGA	256	128	I
	LC4256C-10FT256AI	256	1.8	10	ftBGA	256	128	I
	LC4256C-5FT256BI	256	1.8	5	ftBGA	256	160	I
	LC4256C-75FT256BI	256	1.8	7.5	ftBGA	256	160	I
	LC4256C-10FT256BI	256	1.8	10	ftBGA	256	160	I
	LC4256C-5F256AI <sup>1</sup>	256	1.8	5	fpBGA	256	128	I
	LC4256C-75F256AI <sup>1</sup>	256	1.8	7.5	fpBGA	256	128	I
	LC4256C-10F256AI <sup>1</sup>	256	1.8	10	fpBGA	256	128	I
	LC4256C-5F256BI <sup>1</sup>	256	1.8	5	fpBGA	256	160	I
	LC4256C-75F256BI <sup>1</sup>	256	1.8	7.5	fpBGA	256	160	I
	LC4256C-10F256BI <sup>1</sup>	256	1.8	10	fpBGA	256	160	I
	LC4256C-5T176I	256	1.8	5	TQFP	176	128	I
	LC4256C-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256C-10T176I	256	1.8	10	TQFP	176	128	I
	LC4256C-5T100I	256	1.8	5	TQFP	100	64	I
	LC4256C-75T100I	256	1.8	7.5	TQFP	100	64	I
	LC4256C-10T100I	256	1.8	10	TQFP	100	64	I

## ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI <sup>1</sup>	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI <sup>1</sup>	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI <sup>1</sup>	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI <sup>1</sup>	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI <sup>1</sup>	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI <sup>1</sup>	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
LC4256V-10T100I	256	3.3	10	TQFP	100	64	I	
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I <sup>1</sup>	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I <sup>1</sup>	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I <sup>1</sup>	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I <sup>1</sup>	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I <sup>1</sup>	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I <sup>1</sup>	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I