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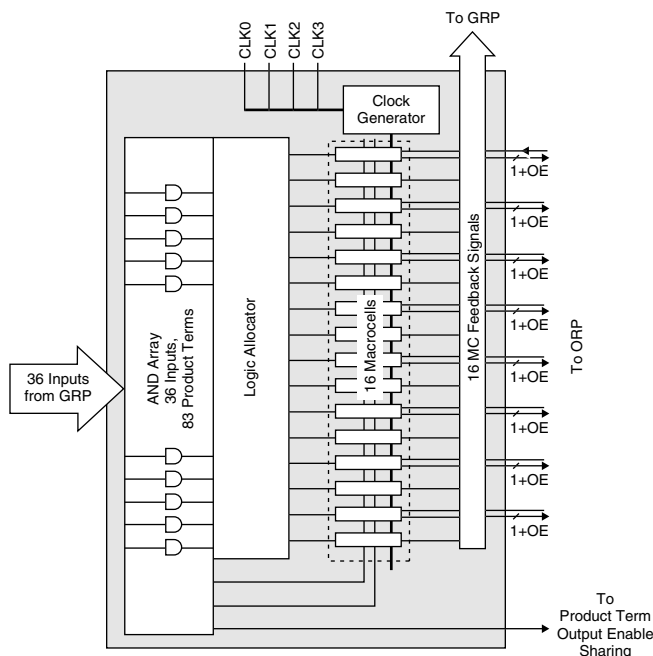
Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	2.7 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128c-27tn100c

Figure 2. Generic Logic Block

AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

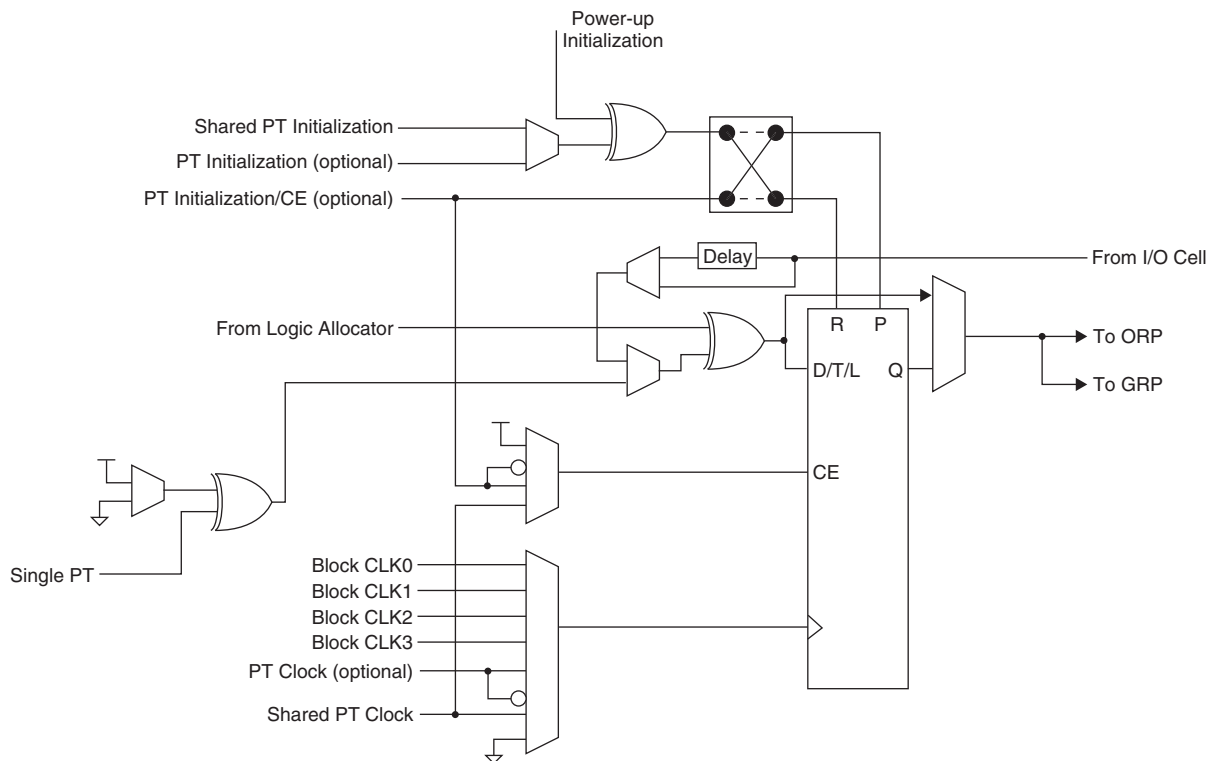
Table 5. Product Term Expansion Capability

Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP} . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell

Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

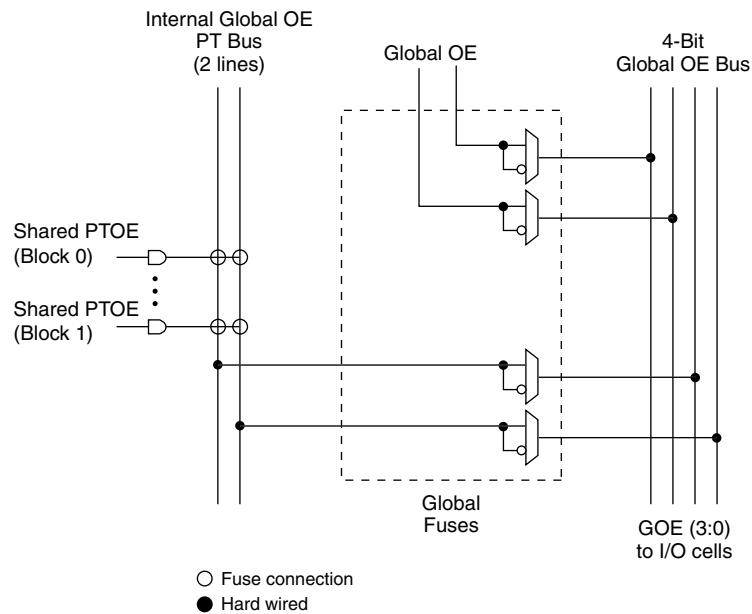
I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

Figure 10. Global OE Generation for ispMACH 4032

Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice’s ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTTL	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	$0.35 * V_{CC}$	$0.65 * V_{CC}$	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	$0.3 * 3.3 * (V_{CC} / 1.8)$	$0.5 * 3.3 * (V_{CC} / 1.8)$	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t _S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t _{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t _{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t _R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t _{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t _{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t _{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f _{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t _S + t _{CO})]	—	250	—	222	—	212	—	212	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.3.2

2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

ispMACH 4000Z Timing Adders (Cont.)¹

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.30	—	1.30	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block load- ing adder	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

Signal Descriptions

Signal Names	Description
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.
GND	Ground
NC	Not Connected
V _{CC}	The power supply pins for logic core and JTAG port.
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.
V _{CC00} , V _{CC01}	The power supply pins for each I/O bank.
yzz	Input/Output ¹ – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.
	ispMACH 4032 y: A-B
	ispMACH 4064 y: A-D
	ispMACH 4128 y: A-H
	ispMACH 4256 y: A-P
	ispMACH 4384 y: A-P, AX-HX
	ispMACH 4512 y: A-P, AX-PX

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

ispMACH 4000V/B/C ORP Reference Table

	4032V/B/C		4064V/B/C			4128V/B/C			4256V/B/C				4384V/B/C		4512V/B/C	
Number of I/Os	30 ¹	32	30 ²	32	64	64	92 ³	96	64	96 ⁴	128	160	128	192	128	208
Number of GLBs	2	2	4	4	4	8	8	8	16	16	16	16	16	16	16	16
Number of I/Os / GLB	16	16	8	8	16	8	12	12	4	8	8	10	8	8	8	Mixture of 8 & 4 ⁵
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	10 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB 4 I/Os / GLB	

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.

2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.

3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os

4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per

5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

ispMACH 4000Z ORP Reference Table

	4032Z	4064Z		4128Z		4256Z		
Number of I/Os	32	32	64	64	96	64	96 ¹	128
Number of GLBs	2	4	4	8	8	16	16	16
Number of I/Os / GLB	16	8	16	8	12	4	8	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹

Signal	44-pin TQFP ²	48-pin TQFP ²	56-ball csBGA ³	100-pin TQFP ²	128-pin TQFP ²
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	4032Z: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹ (Cont.)

Signal	132-ball csBGA ⁷	144-pin TQFP ⁴	176-pin TQFP ⁴	256-ball ftBGA/fpBGA ^{2,3,7,9}
VCC	P1, A14, B7, N8	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
VCCO0 VCCO (Bank 0)	G3, P5, C1 ⁸ , M2 ⁸ , C5	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1 VCCO (Bank 1)	M10, M14 ⁸ , H12, A10, C13 ⁸	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	B1, P2, N14, A13	1, 37, 73, 109	2, 46 ⁵ , 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank 0)	E2, K2, N4, B4	10, 18 ⁶ , 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	N11, K13, E13, B11	55, 65, 82, 90 ⁶ , 99, 118	67, 79, 101, 119, 143	
NC	4064Z: C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1 4128Z: P8, A7	4128V: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 4256V: 18, 90	1, 43, 44, 45, 89, 131, 132, 133	4256V/B/C, 128 I/O: A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15 4256V/B/C, 160 I/O: A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15 4384V/B/C: B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4 4512V/B/C: None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. VCCO balls connect to two power planes within the package, one for VCCO0 and one for VCCO1.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C ¹	E2	E ¹	I6	I ¹
43	1	C2	C ²	E4	E ²	I10	I ²
44	1	C3	C ³	E6	E ³	I12	I ³
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C ⁴	E8	E ⁴	J2	J ⁰
48	1	C5	C ⁵	E10	E ⁵	J6	J ¹
49	1	C6	C ⁶	E12	E ⁶	J10	J ²
50	1	C7	C ⁷	E14	E ⁷	J12	J ³
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C ⁸	F0	F ⁰	K12	K ³
54	1	C9	C ⁹	F2	F ¹	K10	K ²
55	1	C10	C ¹⁰	F4	F ²	K6	K ¹
56	1	C11	C ¹¹	F6	F ³	K2	K ⁰
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C ¹²	F8	F ⁴	L12	L ³
59	1	C13	C ¹³	F10	F ⁵	L10	L ²
60	1	C14	C ¹⁴	F12	F ⁶	L6	L ¹
61	1	C15	C ¹⁵	F13	F ⁷	L4	L ⁰
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D ¹⁵	G14	G ⁷	M4	M ⁰
65	1	D14	D ¹⁴	G12	G ⁶	M6	M ¹
66	1	D13	D ¹³	G10	G ⁵	M10	M ²
67	1	D12	D ¹²	G8	G ⁴	M12	M ³
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D ¹¹	G6	G ³	N2	N ⁰
70	1	D10	D ¹⁰	G5	G ²	N6	N ¹
71	1	D9	D ⁹	G4	G ¹	N10	N ²
72	1	D8	D ⁸	G2	G ⁰	N12	N ³
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D ⁷	H13	H ⁷	O12	O ³
79	1	D6	D ⁶	H12	H ⁶	O10	O ²
80	1	D5	D ⁵	H10	H ⁵	O6	O ¹
81	1	D4	D ⁴	H8	H ⁴	O2	O ⁰
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D ³	H6	H ³	P12	P ³
85	1	D2	D ²	H4	H ²	P10	P ²
86	1	D1	D ¹	H2	H ¹	P6	P ¹
87	1	D0/GOE1	D ⁰	H0/GOE1	H ⁰	P2/OE1	P ⁰
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰	A2/GOE0	A ⁰
92	0	A1	A ¹	A2	A ¹	A6	A ¹
93	0	A2	A ²	A4	A ²	A10	A ²
94	0	A3	A ³	A6	A ³	A12	A ³
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A ⁴	A8	A ⁴	B2	B ⁰
98	0	A5	A ⁵	A10	A ⁵	B6	B ¹
99	0	A6	A ⁶	A12	A ⁶	B10	B ²
100	0	A7	A ⁷	A14	A ⁷	B12	B ³

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B ⁰
5	0	B1	B ¹
6	0	B2	B ²
7	0	B4	B ³
8	0	B5	B ⁴
9	0	B6	B ⁵
10	0	GND (Bank 0)	-
11	0	B8	B ⁶
12	0	B9	B ⁷
13	0	B10	B ⁸
14	0	B12	B ⁹
15	0	B13	B ¹⁰
16	0	B14	B ¹¹
17	0	VCCO (Bank 0)	-
18	0	C14	C ¹¹

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
62	1	E10	E ⁸
63	1	E12	E ⁹
64	1	E14	E ¹¹
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F ⁰
69	1	F1	F ¹
70	1	F2	F ²
71	1	F4	F ³
72	1	F5	F ⁴
73	1	F6	F ⁵
74	1	GND (Bank 1)	-
75	1	F8	F ⁶
76	1	F9	F ⁷
77	1	F10	F ⁸
78	1	F12	F ⁹
79	1	F13	F ¹⁰
80	1	F14	F ¹¹
81	1	VCCO (Bank 1)	-
82	1	G14	G ¹¹
83	1	G13	G ¹⁰
84	1	G12	G ⁹
85	1	G10	G ⁸
86	1	G9	G ⁷
87	1	G8	G ⁶
88	1	GND (Bank 1)	-
89	1	G6	G ⁵
90	1	G5	G ⁴
91	1	G4	G ³
92	1	G2	G ²
93	1	G0	G ⁰
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H ¹¹
99	1	H13	H ¹⁰
100	1	H12	H ⁹
101	1	H10	H ⁸
102	1	H9	H ⁷
103	1	H8	H ⁶
104	1	GND (Bank 1)	-

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
142	1	O0	O ⁰	GX0	GX ⁰	OX0	OX ⁰
143	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
145	1	P14	P ⁷	HX14	HX ⁷	PX14	PX ⁷
146	1	P12	P ⁶	HX12	HX ⁶	PX12	PX ⁶
147	1	P10	P ⁵	HX10	HX ⁵	PX10	PX ⁵
148	1	P8	P ⁴	HX8	HX ⁴	PX8	PX ⁴
149	1	P6	P ³	HX6	HX ³	PX6	PX ³
150	1	P4	P ²	HX4	HX ²	PX4	PX ²
151	1	P2/GOE1	P ¹	HX2/GOE1	HX ¹	PX2/GOE1	PX ¹
152	1	P0	P ⁰	HX0	HX ⁰	PX0	PX ⁰
153	-	GND	-	GND	-	GND	-
154	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
155	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
156	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
157	-	VCC	-	VCC	-	VCC	-
158	0	A0	A ⁰	A0	A ⁰	A0	A ⁰
159	0	A2/GOE0	A ¹	A2/GOE0	A ¹	A2/GOE0	A ¹
160	0	A4	A ²	A4	A ²	A4	A ²
161	0	A6	A ³	A6	A ³	A6	A ³
162	0	A8	A ⁴	A8	A ⁴	A8	A ⁴
163	0	A10	A ⁵	A10	A ⁵	A10	A ⁵
164	0	A12	A ⁶	A12	A ⁶	A12	A ⁶
165	0	A14	A ⁷	A14	A ⁷	A14	A ⁷
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
167	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
168	0	B0	B ⁰	B0	B ⁰	B0	B ⁰
169	0	B2	B ¹	B2	B ¹	B2	B ¹
170	0	B4	B ²	B4	B ²	B4	B ²
171	0	B6	B ³	B6	B ³	B6	B ³
172	0	B8	B ⁴	B8	B ⁴	B8	B ⁴
173	0	B10	B ⁵	B10	B ⁵	B10	B ⁵
174	0	B12	B ⁶	B12	B ⁶	B12	B ⁶
175	0	B14	B ⁷	B14	B ⁷	B14	B ⁷
176	-	VCC	-	VCC	-	VCC	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L [^] 1
T5	0	NC	-	NC	-	I2	I [^] 1	L8	L [^] 2
R6	0	NC	-	NC	-	I0	I [^] 0	L12	L [^] 3
T6	0	NC	-	H14	H [^] 9	G12	G [^] 6	M8	M [^] 2
N7	0	NC	-	H12	H [^] 8	G14	G [^] 7	M12	M [^] 3
P7	0	H14	H [^] 7	H10	H [^] 7	L14	L [^] 7	P14	P [^] 7
R7	0	H12	H [^] 6	H9	H [^] 6	L12	L [^] 6	P12	P [^] 6
L8	0	H10	H [^] 5	H8	H [^] 5	L10	L [^] 5	P10	P [^] 5
T7	0	H8	H [^] 4	H6	H [^] 4	L8	L [^] 4	P8	P [^] 4
M8	0	H6	H [^] 3	H4	H [^] 3	L6	L [^] 3	P6	P [^] 3
N8	0	H4	H [^] 2	H2	H [^] 2	L4	L [^] 2	P4	P [^] 2
R8	0	H2	H [^] 1	H1	H [^] 1	L2	L [^] 1	P2	P [^] 1
P8	0	H0	H [^] 0	H0	H [^] 0	L0	L [^] 0	P0	P [^] 0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I [^] 0	I0	I [^] 0	M0	M [^] 0	AX0	AX [^] 0
R9	1	I2	I [^] 1	I1	I [^] 1	M2	M [^] 1	AX2	AX [^] 1
T9	1	I4	I [^] 2	I2	I [^] 2	M4	M [^] 2	AX4	AX [^] 2
T10	1	I6	I [^] 3	I4	I [^] 3	M6	M [^] 3	AX6	AX [^] 3
R10	1	I8	I [^] 4	I6	I [^] 4	M8	M [^] 4	AX8	AX [^] 4
M9	1	I10	I [^] 5	I8	I [^] 5	M10	M [^] 5	AX10	AX [^] 5
P10	1	I12	I [^] 6	I9	I [^] 6	M12	M [^] 6	AX12	AX [^] 6
L9	1	I14	I [^] 7	I10	I [^] 7	M14	M [^] 7	AX14	AX [^] 7
N10	1	NC	-	I12	I [^] 8	BX14	BX [^] 7	DX0	DX [^] 0
T11	1	NC	-	I14	I [^] 9	BX12	BX [^] 6	DX4	DX [^] 1
R11	1	NC	-	NC	-	P0	P [^] 0	EX0	EX [^] 0
T12	1	NC	-	NC	-	P2	P [^] 1	EX4	EX [^] 1
N12	1	NC	-	NC	-	NC	-	EX8	EX [^] 2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX [^] 3
T13	1	NC	-	J0	J [^] 0	BX10	BX [^] 5	DX8	DX [^] 2
P12	1	NC	-	J1	J [^] 1	BX8	BX [^] 4	DX12	DX [^] 3
M10	1	J0	J [^] 0	J2	J [^] 2	N0	N [^] 0	BX0	BX [^] 0
R13	1	J2	J [^] 1	J4	J [^] 3	N2	N [^] 1	BX2	BX [^] 1
L10	1	J4	J [^] 2	J6	J [^] 4	N4	N [^] 2	BX4	BX [^] 2
T14	1	J6	J [^] 3	J8	J [^] 5	N6	N [^] 3	BX6	BX [^] 3
M11	1	J8	J [^] 4	J9	J [^] 6	N8	N [^] 4	BX8	BX [^] 4

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC ¹	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC ¹	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC ¹	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC ¹	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC ¹	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC ¹	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C ¹	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C ¹	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C ¹	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C ¹	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C ¹	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C ¹	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512C	LC4512C-35FTN256C	512	1.8	3.5	Lead-free ftBGA	256	208	C
	LC4512C-5FTN256C	512	1.8	5	Lead-free ftBGA	256	208	C
	LC4512C-75FTN256C	512	1.8	7.5	Lead-free ftBGA	256	208	C
	LC4512C-35FN256C ¹	512	1.8	3.5	Lead-free fpBGA	256	208	C
	LC4512C-5FN256C ¹	512	1.8	5	Lead-free fpBGA	256	208	C
	LC4512C-75FN256C ¹	512	1.8	7.5	Lead-free fpBGA	256	208	C
	LC4512C-35TN176C	512	1.8	3.5	Lead-free TQFP	176	128	C
	LC4512C-5TN176C	512	1.8	5	Lead-free TQFP	176	128	C
	LC4512C-75TN176C	512	1.8	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000C (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032C-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I
	LC4032C-10TN48I	32	1.8	10	Lead-free TQFP	48	32	I
	LC4032C-5TN44I	32	1.8	5	Lead-free TQFP	44	30	I
	LC4032C-75TN44I	32	1.8	7.5	Lead-free TQFP	44	30	I
	LC4032C-10TN44I	32	1.8	10	Lead-free TQFP	44	30	I
LC4064C	LC4064C-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064C-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064C-10TN100I	64	1.8	10	Lead-free TQFP	100	64	I
	LC4064C-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064C-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
	LC4064C-10TN48I	64	1.8	10	Lead-free TQFP	48	32	I
	LC4064C-5TN44I	64	1.8	5	Lead-free TQFP	44	30	I
	LC4064C-75TN44I	64	1.8	5	Lead-free TQFP	44	30	I
	LC4064C-10TN44I	64	1.8	10	Lead-free TQFP	44	30	I
LC4128C	LC4128C-5TN128I	128	1.8	5	Lead-free TQFP	128	92	I
	LC4128C-75TN128I	128	1.8	7.5	Lead-free TQFP	128	92	I
	LC4128C-10TN128I	128	1.8	10	Lead-free TQFP	128	92	I
	LC4128C-5TN100I	128	1.8	5	Lead-free TQFP	100	64	I
	LC4128C-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
	LC4128C-10TN100I	128	1.8	10	Lead-free TQFP	100	64	I

ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C ¹	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C ¹	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
	LC4384B-75TN176C	384	2.5	7.5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C ¹	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C ¹	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

ispMACH 4000V (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25TN48C	32	3.3	2.5	Lead-free TQFP	48	32	C
	LC4032V-5TN48C	32	3.3	5	Lead-free TQFP	48	32	C
	LC4032V-75TN48C	32	3.3	7.5	Lead-free TQFP	48	32	C
	LC4032V-25TN44C	32	3.3	2.5	Lead-free TQFP	44	30	C
	LC4032V-5TN44C	32	3.3	5	Lead-free TQFP	44	30	C
	LC4032V-75TN44C	32	3.3	7.5	Lead-free TQFP	44	30	C
LC4064V	LC4064V-25TN100C	64	3.3	2.5	Lead-free TQFP	100	64	C
	LC4064V-5TN100C	64	3.3	5	Lead-free TQFP	100	64	C
	LC4064V-75TN100C	64	3.3	7.5	Lead-free TQFP	100	64	C
	LC4064V-25TN48C	64	3.3	2.5	Lead-free TQFP	48	32	C
	LC4064V-5TN48C	64	3.3	5	Lead-free TQFP	48	32	C
	LC4064V-75TN48C	64	3.3	7.5	Lead-free TQFP	48	32	C
	LC4064V-25TN44C	64	3.3	2.5	Lead-free TQFP	44	30	C
	LC4064V-5TN44C	64	3.3	5	Lead-free TQFP	44	30	C
	LC4064V-75TN44C	64	3.3	7.5	Lead-free TQFP	44	30	C
LC4128V	LC4128V-27TN144C	128	3.3	2.7	Lead-free TQFP	144	96	C
	LC4128V-5TN144C	128	3.3	5	Lead-free TQFP	144	96	C
	LC4128V-75TN144C	128	3.3	7.5	Lead-free TQFP	144	96	C
	LC4128V-27TN128C	128	3.3	2.7	Lead-free TQFP	128	92	C
	LC4128V-5TN128C	128	3.3	5	Lead-free TQFP	128	92	C
	LC4128V-75TN128C	128	3.3	7.5	Lead-free TQFP	128	92	C
	LC4128V-27TN100C	128	3.3	2.7	Lead-free TQFP	100	64	C
	LC4128V-5TN100C	128	3.3	5	Lead-free TQFP	100	64	C
	LC4128V-75TN100C	128	3.3	7.5	Lead-free TQFP	100	64	C

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I