Lattice Semiconductor Corporation - LC4128V-27TN100C Datasheet

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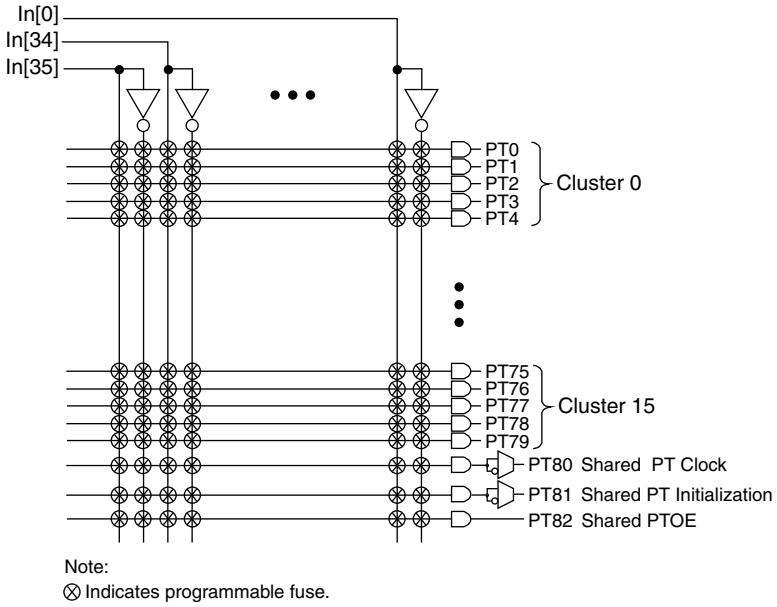
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	2.7 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128v-27tn100c

Figure 3. AND Array



Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice

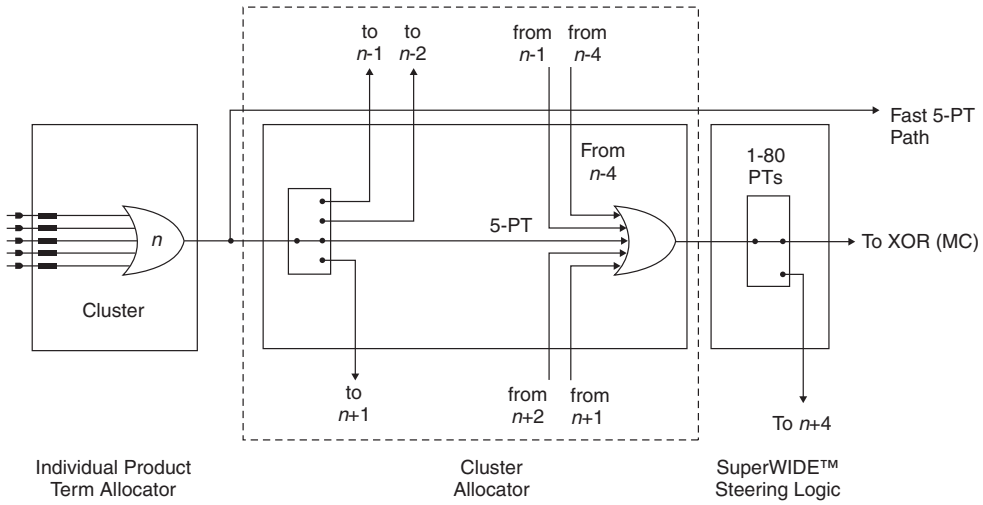


Table 5. Product Term Expansion Capability

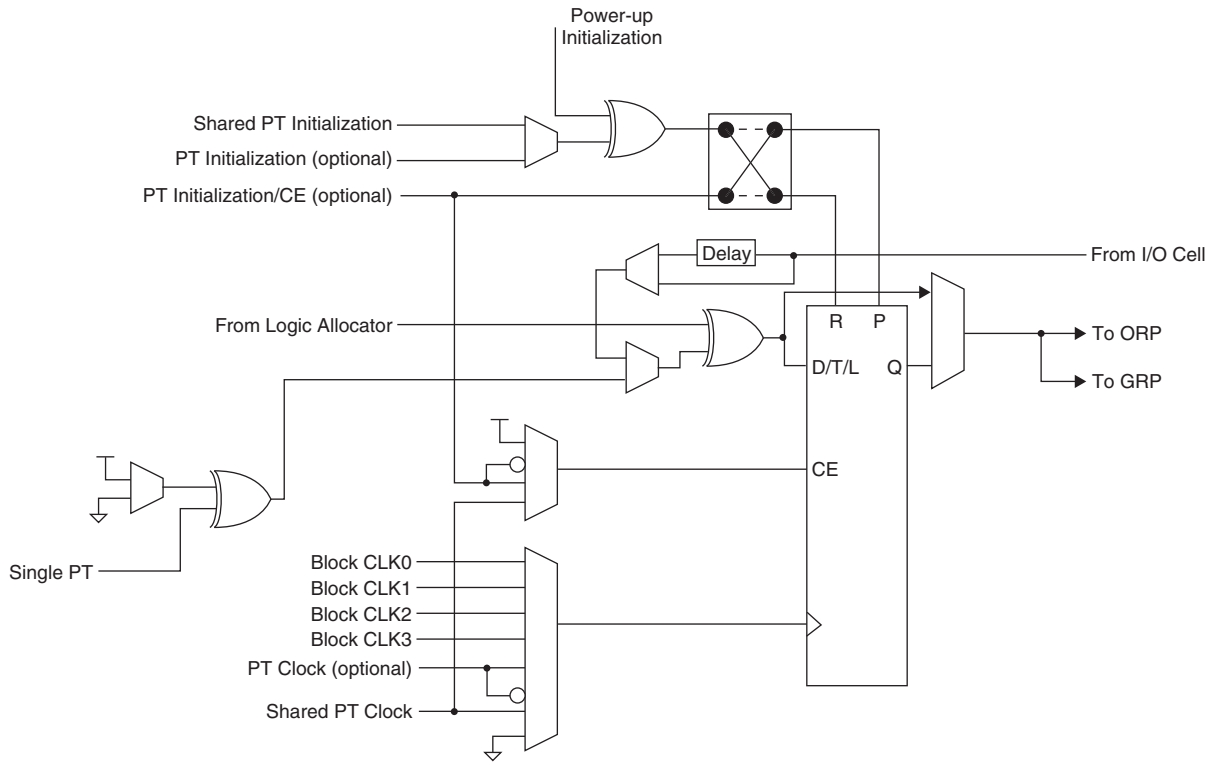
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

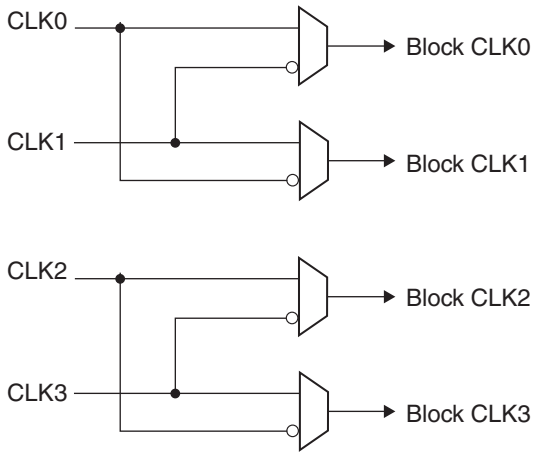
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The ispMACH 4000 device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

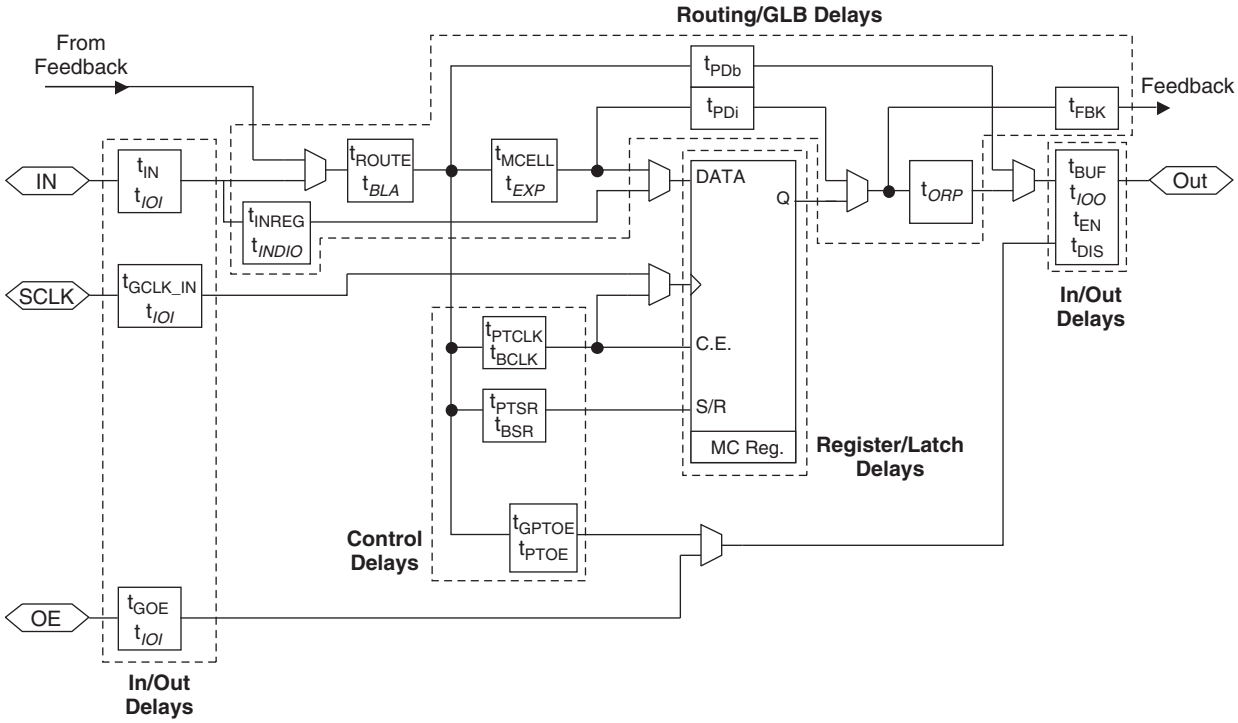
Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t_S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_H	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{GPTOE}	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
t_{PTOE}	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

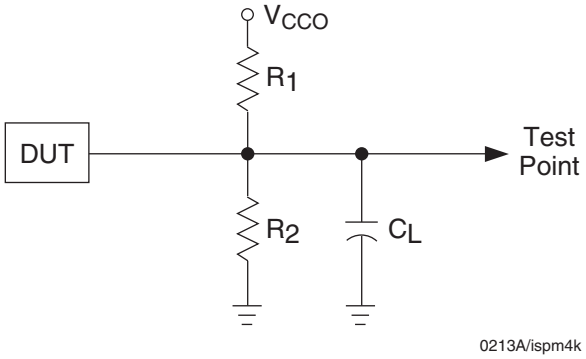


Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC[2]	-	I[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D^2	E4	E^2	G4	G^2
20	0	D2	D^1	E2	E^1	G2	G^1
21	0	D0	D^0	E0	E^0	G0	G^0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E^0	H0	H^0	J0	J^0
24	0	E2	E^1	H2	H^1	J2	J^1
25	0	E4	E^2	H4	H^2	J4	J^2
26	0	E6	E^3	H6	H^3	J6	J^3
27	0	E8	E^4	H8	H^4	J8	J^4
28	0	E10	E^5	H10	H^5	J10	J^5
29	0	E12	E^6	H12	H^6	J12	J^6
30	0	E14	E^7	H14	H^7	J14	J^7
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F^0	J0	J^0	N0	N^0
33	0	F2	F^1	J2	J^1	N2	N^1
34	0	F4	F^2	J4	J^2	N4	N^2
35	0	F6	F^3	J6	J^3	N6	N^3
36	0	F8	F^4	J8	J^4	N8	N^4
37	0	F10	F^5	J10	J^5	N10	N^5
38	0	F12	F^6	J12	J^6	N12	N^6
39	0	F14	F^7	J14	J^7	N14	N^7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G^7	K14	K^7	O14	O^7
48	0	G12	G^6	K12	K^6	O12	O^6
49	0	G10	G^5	K10	K^5	O10	O^5
50	0	G8	G^4	K8	K^4	O8	O^4
51	0	G6	G^3	K6	K^3	O6	O^3
52	0	G4	G^2	K4	K^2	O4	O^2
53	0	G2	G^1	K2	K^1	O2	O^1
54	0	G0	G^0	K0	K^0	O0	O^0
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H^7	L14	L^7	P14	P^7
58	0	H12	H^6	L12	L^6	P12	P^6
59	0	H10	H^5	L10	L^5	P10	P^5

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M^1	M1	M^1	DX2	DX^1	JX2	JX^1
H14	1	M4	M^2	M2	M^2	DX4	DX^2	JX4	JX^2
H13	1	M6	M^3	M4	M^3	DX6	DX^3	JX6	JX^3
G16	1	M8	M^4	M6	M^4	DX8	DX^4	JX8	JX^4
H12	1	M10	M^5	M8	M^5	DX10	DX^5	JX10	JX^5
G15	1	M12	M^6	M9	M^6	DX12	DX^6	JX12	JX^6
H11	1	M14	M^7	M10	M^7	DX14	DX^7	JX14	JX^7
F16	1	NC	-	M12	M^8	CX0	CX^0	IX0	IX^0
G13	1	NC	-	M14	M^9	CX2	CX^1	IX4	IX^1
G14	1	NC	-	NC	-	EX14	EX^7	KX0	KX^0
F15	1	NC	-	NC	-	EX12	EX^6	KX2	KX^1
E16	1	NC	-	NC	-	NC	-	KX4	KX^2
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX^3
G12	1	NC	-	NC	-	EX10	EX^5	KX8	KX^4
E13	1	NC	-	NC	-	EX8	EX^4	KX10	KX^5
D16	1	NC	-	N0	N^0	CX4	CX^2	IX8	IX^2
E14	1	NC	-	N1	N^1	CX6	CX^3	IX12	IX^3
G11	1	N0	N^0	N2	N^2	FX0	FX^0	NX0	NX^0
D15	1	N2	N^1	N4	N^3	FX2	FX^1	NX2	NX^1
F11	1	N4	N^2	N6	N^4	FX4	FX^2	NX4	NX^2
C16	1	N6	N^3	N8	N^5	FX6	FX^3	NX6	NX^3
F12	1	N8	N^4	N9	N^6	FX8	FX^4	NX8	NX^4
D14	1	N10	N^5	N10	N^7	FX10	FX^5	NX10	NX^5
C15	1	N12	N^6	N12	N^8	FX12	FX^6	NX12	NX^6
B16	1	N14	N^7	N14	N^9	FX14	FX^7	NX14	NX^7
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX^3	KX12	KX^6
B14	1	NC	-	NC	-	EX4	EX^2	KX14	KX^7
E12	1	O14	O^7	O14	O^9	GX14	GX^7	OX14	OX^7
A14	1	O12	O^6	O12	O^8	GX12	GX^6	OX12	OX^6
C13	1	O10	O^5	O10	O^7	GX10	GX^5	OX10	OX^5
D13	1	O8	O^4	O9	O^6	GX8	GX^4	OX8	OX^4
E11	1	O6	O^3	O8	O^5	GX6	GX^3	OX6	OX^3
B13	1	O4	O^2	O6	O^4	GX4	GX^2	OX4	OX^2
F10	1	O2	O^1	O4	O^3	GX2	GX^1	OX2	OX^1

Part Number Description

LC XXXX X X – XX XX XXX X X XX

Device Family

Device Number
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells
4384 = 384 Macrocells
4512 = 512 Macrocells

Power
Z = Zero Power
Blank = Low Power

Supply Voltage
V = 3.3V
B = 2.5V
C = 1.8V

Speed
25 = 2.5ns
27 = 2.7ns
3 = 3.0ns
35 = 3.5ns
37 = 3.7ns
42 = 4.2ns
45 = 4.5ns
5 = 5.0ns
75 = 7.5ns
10 = 10.0ns

Package

T = TQFP	TN = Lead-free TQFP
FT = ftBGA	FTN= Lead-free ftBGA
F = fpBGA[2]	FN = Lead-free fpBGA[2]
M = csBGA	MN = Lead-free csBGA

Pin/Ball Count
44 (1.0mm thickness)
48 (1.0mm thickness)
56
100
128
132
144
176
256

I/O Designator (if applicable)
A = 128 I/Os
B = 160 I/Os

Operating Temperature Range
C = Commercial
I = Industrial
E = Extended[1]

Production Status
Blank = Final production
ES = Engineering Samples

1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	tPD	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5M132I	64	1.8	5	csBGA	132	64	I
	LC4064ZC-75M132I	64	1.8	7.5	csBGA	132	64	I
	LC4064ZC-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064ZC-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064ZC-5M56I	64	1.8	5	csBGA	56	34	I
	LC4064ZC-75M56I	64	1.8	7.5	csBGA	56	34	I
	LC4064ZC-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064ZC-75T48I	64	1.8	7.5	TQFP	48	32	I
LC4128ZC	LC4128ZC-75M132I	128	1.8	7.5	csBGA	132	96	I
	LC4128ZC-75T100I	128	1.8	7.5	TQFP	100	64	I
LC4256ZC	LC4256ZC-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256ZC-75M132I	256	1.8	7.5	csBGA	132	96	I
	LC4256ZC-75T100I	256	1.8	7.5	TQFP	100	64	I

ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75T48E	32	1.8	7.5	TQFP	48	32	E
LC4064ZC	LC4064ZC-75T100E	64	1.8	7.5	TQFP	100	64	E
	LC4064ZC-75T48E	64	1.8	7.5	TQFP	48	32	E
LC4128ZC	LC4128ZC-75T100E	128	1.8	7.5	TQFP	100	64	E
LC4256ZC	LC4256ZC-75T176E	256	1.8	7.5	TQFP	176	128	E
	LC4256ZC-75T100E	256	1.8	7.5	TQFP	100	64	E

ispMACH 4000C (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25T48C	32	1.8	2.5	TQFP	48	32	C
	LC4032C-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032C-75T48C	32	1.8	7.5	TQFP	48	32	C
	LC4032C-25T44C	32	1.8	2.5	TQFP	44	30	C
	LC4032C-5T44C	32	1.8	5	TQFP	44	30	C
	LC4032C-75T44C	32	1.8	7.5	TQFP	44	30	C
LC4064C	LC4064C-25T100C	64	1.8	2.5	TQFP	100	64	C
	LC4064C-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064C-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064C-25T48C	64	1.8	2.5	TQFP	48	32	C
	LC4064C-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064C-75T48C	64	1.8	7.5	TQFP	48	32	C
	LC4064C-25T44C	64	1.8	2.5	TQFP	44	30	C
	LC4064C-5T44C	64	1.8	5	TQFP	44	30	C
	LC4064C-75T44C	64	1.8	7.5	TQFP	44	30	C

ispMACH 4000C (1.8V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92	C
	LC4128C-5T128C	128	1.8	5	TQFP	128	92	C
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92	C
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64	C
	LC4128C-5T100C	128	1.8	5	TQFP	100	64	C
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256C	LC4256C-3FT256AC	256	1.8	3	ftBGA	256	128	C
	LC4256C-5FT256AC	256	1.8	5	ftBGA	256	128	C
	LC4256C-75FT256AC	256	1.8	7.5	ftBGA	256	128	C
	LC4256C-3FT256BC	256	1.8	3	ftBGA	256	160	C
	LC4256C-5FT256BC	256	1.8	5	ftBGA	256	160	C
	LC4256C-75FT256BC	256	1.8	7.5	ftBGA	256	160	C
	LC4256C-3F256AC[1]	256	1.8	3	fpBGA	256	128	C
	LC4256C-5F256AC[1]	256	1.8	5	fpBGA	256	128	C
	LC4256C-75F256AC[1]	256	1.8	7.5	fpBGA	256	128	C
	LC4256C-3F256BC[1]	256	1.8	3	fpBGA	256	160	C
	LC4256C-5F256BC[1]	256	1.8	5	fpBGA	256	160	C
	LC4256C-75F256BC[1]	256	1.8	7.5	fpBGA	256	160	C
	LC4256C-3T176C	256	1.8	3	TQFP	176	128	C
	LC4256C-5T176C	256	1.8	5	TQFP	176	128	C
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256C-3T100C	256	1.8	3	TQFP	100	64	C
	LC4256C-5T100C	256	1.8	5	TQFP	100	64	C
	LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C
LC4384C	LC4384C-35FT256C	384	1.8	3.5	ftBGA	256	192	C
	LC4384C-5FT256C	384	1.8	5	ftBGA	256	192	C
	LC4384C-75FT256C	384	1.8	7.5	ftBGA	256	192	C
	LC4384C-35F256C[1]	384	1.8	3.5	fpBGA	256	192	C
	LC4384C-5F256C[1]	384	1.8	5	fpBGA	256	192	C
	LC4384C-75F256C[1]	384	1.8	7.5	fpBGA	256	192	C
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128	C
	LC4384C-5T176C	384	1.8	5	TQFP	176	128	C
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128	C
LC4512C	LC4512C-35FT256C	512	1.8	3.5	ftBGA	256	208	C
	LC4512C-5FT256C	512	1.8	5	ftBGA	256	208	C
	LC4512C-75FT256C	512	1.8	7.5	ftBGA	256	208	C
	LC4512C-35F256C[1]	512	1.8	3.5	fpBGA	256	208	C
	LC4512C-5F256C[1]	512	1.8	5	fpBGA	256	208	C
	LC4512C-75F256C[1]	512	1.8	7.5	fpBGA	256	208	C
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
	LC4512C-5T176C	512	1.8	5	TQFP	176	128	C
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

ispMACH 4000V (3.3V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-3FTN256AC	256	3.3	3	Lead-free ftBGA	256	128	C
	LC4256V-5FTN256AC	256	3.3	5	Lead-free ftBGA	256	128	C
	LC4256V-75FTN256AC	256	3.3	7.5	Lead-free ftBGA	256	128	C
	LC4256V-3FTN256BC	256	3.3	3	Lead-free ftBGA	256	160	C
	LC4256V-5FTN256BC	256	3.3	5	Lead-free ftBGA	256	160	C
	LC4256V-75FTN256BC	256	3.3	7.5	Lead-free ftBGA	256	160	C
	LC4256V-3FN256AC[1]	256	3.3	3	Lead-free fpBGA	256	128	C
	LC4256V-5FN256AC[1]	256	3.3	5	Lead-free fpBGA	256	128	C
	LC4256V-75FN256AC[1]	256	3.3	7.5	Lead-free fpBGA	256	128	C
	LC4256V-3FN256BC[1]	256	3.3	3	Lead-free fpBGA	256	160	C
	LC4256V-5FN256BC[1]	256	3.3	5	Lead-free fpBGA	256	160	C
	LC4256V-75FN256BC[1]	256	3.3	7.5	Lead-free fpBGA	256	160	C
	LC4256V-3TN176C	256	3.3	3	Lead-free TQFP	176	128	C
	LC4256V-5TN176C	256	3.3	5	Lead-free TQFP	176	128	C
	LC4256V-75TN176C	256	3.3	7.5	Lead-free TQFP	176	128	C
	LC4256V-3TN144C	256	3.3	3	Lead-free TQFP	144	96	C
	LC4256V-5TN144C	256	3.3	5	Lead-free TQFP	144	96	C
	LC4256V-75TN144C	256	3.3	7.5	Lead-free TQFP	144	96	C
	LC4256V-3TN100C	256	3.3	3	Lead-free TQFP	100	64	C
	LC4256V-5TN100C	256	3.3	5	Lead-free TQFP	100	64	C
	LC4256V-75TN100C	256	3.3	7.5	Lead-free TQFP	100	64	C
LC4384V	LC4384V-35FTN256C	384	3.3	3.5	Lead-free ftBGA	256	192	C
	LC4384V-5FTN256C	384	3.3	5	Lead-free ftBGA	256	192	C
	LC4384V-75FTN256C	384	3.3	7.5	Lead-free ftBGA	256	192	C
	LC4384V-35FN256C[1]	384	3.3	3.5	Lead-free fpBGA	256	192	C
	LC4384V-5FN256C[1]	384	3.3	5	Lead-free fpBGA	256	192	C
	LC4384V-75FN256C[1]	384	3.3	7.5	Lead-free fpBGA	256	192	C
	LC4384V-35TN176C	384	3.3	3.5	Lead-free TQFP	176	128	C
	LC4384V-5TN176C	384	3.3	5	Lead-free TQFP	176	128	C
	LC4384V-75TN176C	384	3.3	7.5	Lead-free TQFP	176	128	C
LC4512V	LC4512V-35FTN256C	512	3.3	3.5	Lead-free ftBGA	256	208	C
	LC4512V-5FTN256C	512	3.3	5	Lead-free ftBGA	256	208	C
	LC4512V-75FTN256C	512	3.3	7.5	Lead-free ftBGA	256	208	C
	LC4512V-35FN256C[1]	512	3.3	3.5	Lead-free fpBGA	256	208	C
	LC4512V-5FN256C[1]	512	3.3	5	Lead-free fpBGA	256	208	C
	LC4512V-75FN256C[1]	512	3.3	7.5	Lead-free fpBGA	256	208	C
	LC4512V-35TN176C	512	3.3	3.5	Lead-free TQFP	176	128	C
	LC4512V-5TN176C	512	3.3	5	Lead-free TQFP	176	128	C
	LC4512V-75TN176C	512	3.3	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points (0 ≤ VIN ≤ 3.6V).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided (VIN - VCCO) ≤ 3.6V.
		Improved LC4064ZC t_S to 2.5ns, t_{ST} to 2.7ns and f_{MAX} (Ext.) to 175MHz, LC4128ZC t_{CO} to 3.5ns and f_{MAX} (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150µA to -200µA.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.