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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 128 |
| Number of Gates | - |
| Number of I/O | 64 |
| Operating Temperature | 0°C ~ 90°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128v-5t100c |

*Table 2. ispMACH 4000Z Family Selection Guide*

| | ispMACH 4032ZC | ispMACH 4064ZC | ispMACH 4128ZC | ispMACH 4256ZC |
|---|---|---|---|---|
| Macrocells | 32 | 64 | 128 | 256 |
| I/O + Dedicated Inputs | 32+4/32+4 | 32+4/32+12/ 64+10/64+10 | 64+10/96+4 | 64+10/96+6/ 128+4 |
| $t_{PD}$ (ns) | 3.5 | 3.7 | 4.2 | 4.5 |
| $t_S$ (ns) | 2.2 | 2.5 | 2.7 | 2.9 |
| $t_{CO}$ (ns) | 3.0 | 3.2 | 3.5 | 3.8 |
| $f_{MAX}$ (MHz) | 267 | 250 | 220 | 200 |
| Supply Voltage (V) | 1.8 | 1.8 | 1.8 | 1.8 |
| Max. Standby Icc (µA) | 20 | 25 | 35 | 55 |
| Pins/Package | 48 TQFP<br>56 csBGA | 48 TQFP<br>56 csBGA<br>100 TQFP<br>132 csBGA | 100 TQFP<br>132csBGA | 100 TQFP<br>132 csBGA<br>176 TQFP |

## ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

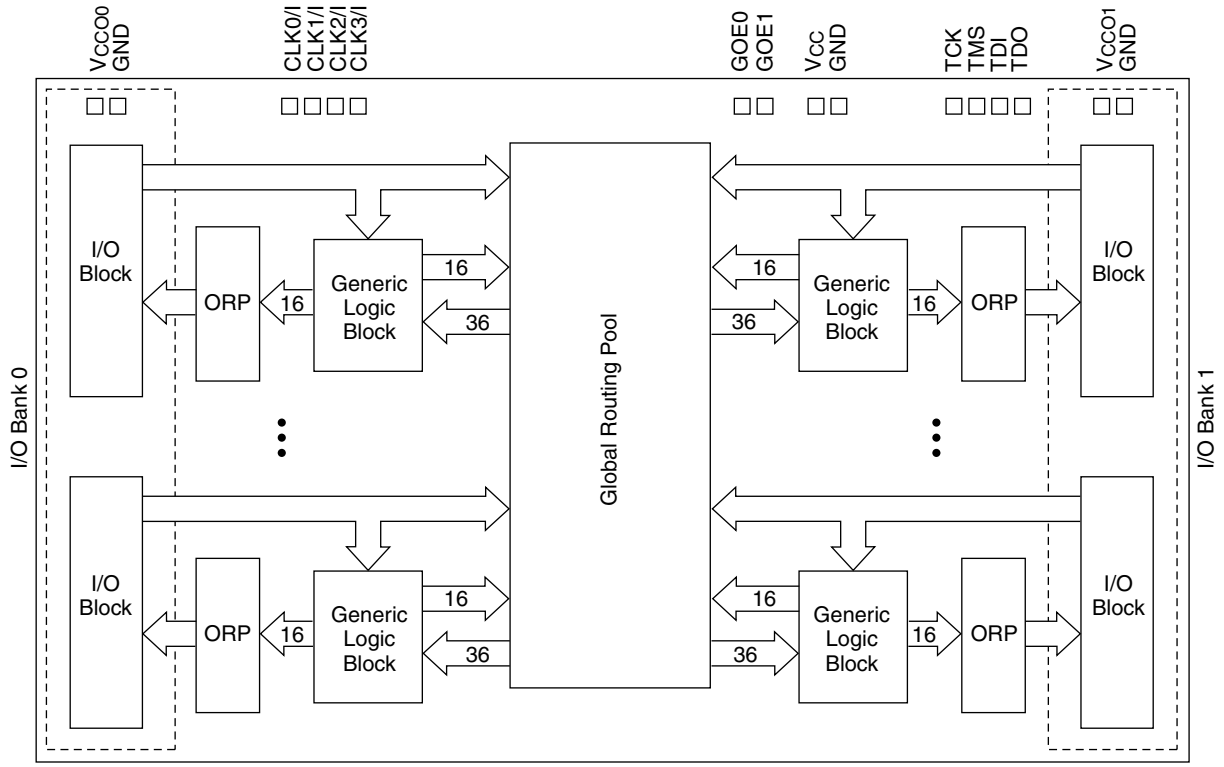
The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to $V_{CC}$ (logic core).

## Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

***Figure 1. Functional Block Diagram***




The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to $V_{CCO}$ of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

## ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

### Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

# I/O DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVTTL | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 3.3 | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.70 | 1.70 | 3.6 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.8 (4000V/B) | -0.3 | 0.63 | 1.17 | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.8 (4000C/Z) | -0.3 | 0.35 * $V_{CC}$ | 0.65 * $V_{CC}$ | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| PCI 3.3 (4000V/B) | -0.3 | 1.08 | 1.5 | 5.5 | 0.1 $V_{CCO}$ | 0.9 $V_{CCO}$ | 1.5 | -0.5 |
| PCI 3.3 (4000C/Z) | -0.3 | 0.3 * 3.3 * ($V_{CC}$ / 1.8) | 0.5 * 3.3 * ($V_{CC}$ / 1.8) | 5.5 | 0.1 $V_{CCO}$ | 0.9 $V_{CCO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

# ispMACH 4000V/B/C Timing Adders[1]

| Adder Type | Base Parameter | Description | -25 | | -27 | | -3 | | -35 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 0.95 | — | 1.00 | — | 1.00 | — | 1.00 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.33 | — | 0.33 | — | 0.33 | — | 0.33 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.05 | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.03 | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

## ispMACH 4000V/B/C Timing Adders[1] (Cont.)

| Adder Type | Base Parameter | Description | -5 | | -75 | | -10 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 1.00 | — | 1.00 | — | 1.00 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.33 | — | 0.33 | — | 0.33 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

# ispMACH 4000Z Timing Adders [1]

| Adder Type | Base Parameter | Description | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 1.00 | — | 1.00 | — | 1.30 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.40 | — | 0.40 | — | 0.45 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.40 | — | 0.40 | — | 0.40 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.04 | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding the use of these adders.

## ispMACH 4000Z Timing Adders (Cont.)[1]

| Adder Type | Base Parameter | Description | -45 | | -5 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 1.30 | — | 1.30 | — | 1.30 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.45 | — | 0.45 | — | 0.50 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.40 | — | 0.40 | — | 0.40 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

## Boundary Scan Waveforms and Timing Specifications

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{BTCP}$ | TCK [BSCAN test] clock cycle | 40 | — | ns |
| $t_{BTCH}$ | TCK [BSCAN test] pulse width high | 20 | — | ns |
| $t_{BTCL}$ | TCK [BSCAN test] pulse width low | 20 | — | ns |
| $t_{BTSU}$ | TCK [BSCAN test] setup time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN test] hold time | 10 | — | ns |
| $t_{BRF}$ | TCK [BSCAN test] rise and fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTOZ}$ | TAP controller falling edge of clock to data output disable | — | 10 | ns |
| $t_{BTVO}$ | TAP controller falling edge of clock to data output enable | — | 10 | ns |
| $t_{BTCPSU}$ | BSCAN test Capture register setup time | 8 | — | ns |
| $t_{BTCPH}$ | BSCAN test Capture register hold time | 10 | — | ns |
| $t_{BTUCO}$ | BSCAN test Update reg, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUOZ}$ | BSCAN test Update reg, falling edge of clock to output disable | — | 25 | ns |
| $t_{BTUOV}$ | BSCAN test Update reg, falling edge of clock to output enable | — | 25 | ns |

## Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

***Figure 12. Output Test Load, LVTTL and LVCMOS Standards***

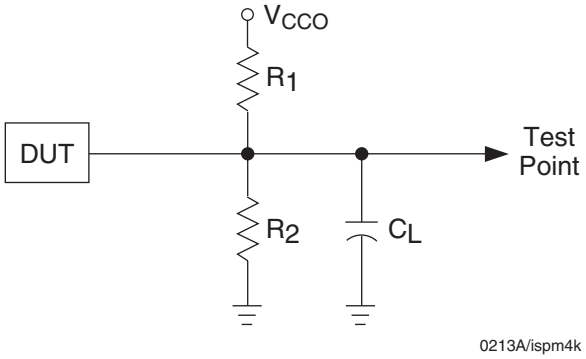



***Table 11. Test Fixture Required Components***

| Test Condition | $R_1$ | $R_2$ | $C_L$[1] | Timing Ref. | $V_{CCO}$ |
|---|---|---|---|---|---|
| LVCMOS I/O, (L -> H, H -> L) | 106Ω | 106Ω | 35pF | LVCMOS 3.3 = 1.5V | LVCMOS 3.3 = 3.0V |
| | | | | LVCMOS 2.5 = $V_{CCO}$/2 | LVCMOS 2.5 = 2.3V |
| | | | | LVCMOS 1.8 = $V_{CCO}$/2 | LVCMOS 1.8 = 1.65V |
| LVCMOS I/O (Z -> H) | ∞ | 106Ω | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (Z -> L) | 106Ω | ∞ | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (H -> Z) | ∞ | 106Ω | 5pF | $V_{OH}$ - 0.3 | 3.0V |
| LVCMOS I/O (L -> Z) | 106Ω | ∞ | 5pF | $V_{OL}$ + 0.3 | 3.0V |

1. $C_L$ includes test fixtures and probe capacitance.

## ispMACH 4000V/B/C/Z Power Supply and NC Connections[1] (Cont.)

| Signal | 132-ball csBGA[7] | 144-pin TQFP[4] | 176-pin TQFP[4] | 256-ball ftBGA/fpBGA[2, 3, 7, 9] |
|---|---|---|---|---|
| VCC | P1, A14, B7, N8 | 36, 57, 108, 129 | 42, 69, 88, 130, 157, 176 | B2, B15, G8, G9, K8, K9, R2, R15 |
| VCCO0<br>VCCO (Bank 0) | G3, P5, C1[8], M2[8], C5 | 3, 19, 34, 47, 136 | 4, 22, 40, 56, 166 | D6, F4, H7, J7, L4, N6 |
| VCCO1<br>VCCO (Bank 1) | M10, M14[8], H12, A10, C13[8] | 64, 75, 91, 106, 119 | 78, 92, 110, 128, 144 | D11, F13, H10, J10, L13, N11 |
| GND | B1, P2, N14, A13 | 1, 37, 73, 109 | 2, 46[5], 65, 90, 134, 153 | A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16 |
| GND (Bank 0) | E2, K2, N4, B4 | 10, 18[6], 27, 46, 127, 137 | 13, 31, 55, 155, 167 | |
| GND (Bank 1) | N11, K13, E13, B11 | 55, 65, 82, 90[6], 99, 118 | 67, 79, 101, 119, 143 | |
| NC | **4064Z:** C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1<br><br>**4128Z:** P8, A7 | **4128V**: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144<br><br>**4256V**: 18, 90 | 1, 43, 44, 45, 89, 131, 132, 133 | **4256V/B/C, 128 I/O:** A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15<br><br>**4256V/B/C, 160 I/O:** A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15<br><br>**4384V/B/C:** B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4<br><br>**4512V/B/C:** None |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. $V_{CCO}$ balls connect to two power planes within the package, one for $V_{CCO0}$ and one for $V_{CCO1}$.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 62 | 1 | E10 | E^8 |
| 63 | 1 | E12 | E^9 |
| 64 | 1 | E14 | E^11 |
| 65 | 1 | GND | - |
| 66 | 1 | TMS | - |
| 67 | 1 | VCCO (Bank 1) | - |
| 68 | 1 | F0 | F^0 |
| 69 | 1 | F1 | F^1 |
| 70 | 1 | F2 | F^2 |
| 71 | 1 | F4 | F^3 |
| 72 | 1 | F5 | F^4 |
| 73 | 1 | F6 | F^5 |
| 74 | 1 | GND (Bank 1) | - |
| 75 | 1 | F8 | F^6 |
| 76 | 1 | F9 | F^7 |
| 77 | 1 | F10 | F^8 |
| 78 | 1 | F12 | F^9 |
| 79 | 1 | F13 | F^10 |
| 80 | 1 | F14 | F^11 |
| 81 | 1 | VCCO (Bank 1) | - |
| 82 | 1 | G14 | G^11 |
| 83 | 1 | G13 | G^10 |
| 84 | 1 | G12 | G^9 |
| 85 | 1 | G10 | G^8 |
| 86 | 1 | G9 | G^7 |
| 87 | 1 | G8 | G^6 |
| 88 | 1 | GND (Bank 1) | - |
| 89 | 1 | G6 | G^5 |
| 90 | 1 | G5 | G^4 |
| 91 | 1 | G4 | G^3 |
| 92 | 1 | G2 | G^2 |
| 93 | 1 | G0 | G^0 |
| 94 | 1 | VCCO (Bank 1) | - |
| 95 | 1 | TDO | - |
| 96 | 1 | VCC | - |
| 97 | 1 | GND | - |
| 98 | 1 | H14 | H^11 |
| 99 | 1 | H13 | H^10 |
| 100 | 1 | H12 | H^9 |
| 101 | 1 | H10 | H^8 |
| 102 | 1 | H9 | H^7 |
| 103 | 1 | H8 | H^6 |
| 104 | 1 | GND (Bank 1) | - |

## ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

| | | ispMACH 4064Z | | ispMACH 4128Z | | ispMACH 4256Z | |
|---|---|---|---|---|---|---|---|
| Ball Number | Bank Number | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| E3 | 0 | NC | - | B8 | B^6 | D12 | D^6 |
| F2 | 0 | A12 | A^12 | B9 | B^7 | D10 | D^5 |
| F1 | 0 | A13 | A^13 | B10 | B^8 | D8 | D^4 |
| F3 | 0 | A14 | A^14 | B12 | B^9 | D6 | D^3 |
| G1 | 0 | A15 | A^15 | B13 | B^10 | D4 | D^2 |
| G2 | 0 | I | - | B14 | B^11 | D2 | D^1 |
| G3 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| H2 | 0 | NC | - | C14 | C^11 | E2 | E^1 |
| H1 | 0 | B15 | B^15 | C13 | C^10 | E4 | E^2 |
| H3 | 0 | B14 | B^14 | C12 | C^9 | E6 | E^3 |
| J1 | 0 | B13 | B^13 | C10 | C^8 | E8 | E^4 |
| J2 | 0 | B12 | B^12 | C9 | C^7 | E10 | E^5 |
| J3 | 0 | NC | - | C8 | C^6 | E12 | E^6 |
| K2 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| K1 | 0 | NC | - | C6 | C^5 | F2 | F^1 |
| K3 | 0 | B11 | B^11 | C5 | C^4 | F4 | F^2 |
| L2 | 0 | B10 | B^10 | C4 | C^3 | F6 | F^3 |
| L1 | 0 | B9 | B^9 | C2 | C^2 | F8 | F^4 |
| L3 | 0 | B8 | B^8 | C1 | C^1 | F10 | F^5 |
| M1 | 0 | I | - | C0 | C^0 | F12 | F^6 |
| M2 | 0 | NC | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| N1 | - | TCK | - | TCK | - | TCK | - |
| P1 | - | VCC | - | VCC | - | VCC | - |
| P2 | - | GND | - | GND | - | GND | - |
| N2 | 0 | I | - | D14 | D^11 | G12 | G^6 |
| P3 | 0 | B7 | B^7 | D13 | D^10 | G10 | G^5 |
| M3 | 0 | B6 | B^6 | D12 | D^9 | G8 | G^4 |
| N3 | 0 | B5 | B^5 | D10 | D^8 | G6 | G^3 |
| P4 | 0 | B4 | B^4 | D9 | D^7 | G4 | G^2 |
| M4 | 0 | NC | - | D8 | D^6 | G2 | G^1 |
| N4 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| P5 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| N5 | 0 | NC | - | D6 | D^5 | H12 | H^6 |
| M5 | 0 | B3 | B^3 | D5 | D^4 | H10 | H^5 |
| N6 | 0 | B2 | B^2 | D4 | D^3 | H8 | H^4 |
| P6 | 0 | B1 | B^1 | D2 | D^2 | H6 | H^3 |
| M6 | 0 | B0 | B^0 | D1 | D^1 | H4 | H^2 |
| P7 | 0 | NC | - | D0 | D^0 | H2 | H^1 |
| N7 | 0 | CLK1/I | - | CLK1/I | - | CLK1/I | - |
| M7 | 1 | CLK2/I | - | CLK2/I | - | CLK2/I | - |
| N8 | - | VCC | - | VCC | - | VCC | - |

## ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

| | | ispMACH 4064Z | | ispMACH 4128Z | | ispMACH 4256Z | |
|---|---|---|---|---|---|---|---|
| Ball Number | Bank Number | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| P8 | 1 | NC[1] | - | NC[1] | - | I[1] | - |
| M8 | 1 | NC | - | E0 | E^0 | I2 | I^1 |
| P9 | 1 | C0 | C^0 | E1 | E^1 | I4 | I^2 |
| N9 | 1 | C1 | C^1 | E2 | E^2 | I6 | I^3 |
| M9 | 1 | C2 | C^2 | E4 | E^3 | I8 | I^4 |
| N10 | 1 | C3 | C^3 | E5 | E^4 | I10 | I^5 |
| P10 | 1 | NC | - | E6 | E^5 | I12 | I^6 |
| M10 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| N11 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| P11 | 1 | NC | - | E8 | E^6 | J2 | J^1 |
| M11 | 1 | C4 | C^4 | E9 | E^7 | J4 | J^2 |
| P12 | 1 | C5 | C^5 | E10 | E^8 | J6 | J^3 |
| N12 | 1 | C6 | C^6 | E12 | E^9 | J8 | J^4 |
| P13 | 1 | C7 | C^7 | E13 | E^10 | J10 | J^5 |
| P14 | 1 | NC | - | E14 | E^11 | J12 | J^6 |
| N14 | - | GND | - | GND | - | GND | - |
| N13 | - | TMS | - | TMS | - | TMS | - |
| M14 | 1 | NC | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| M12 | 1 | NC | - | F0 | F^0 | K12 | K^6 |
| M13 | 1 | C8 | C^8 | F1 | F^1 | K10 | K^5 |
| L14 | 1 | C9 | C^9 | F2 | F^2 | K8 | K^4 |
| L12 | 1 | C10 | C^10 | F4 | F^3 | K6 | K^3 |
| L13 | 1 | C11 | C^11 | F5 | F^4 | K4 | K^2 |
| K14 | 1 | NC | - | F6 | F^5 | K2 | K^1 |
| K13 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| K12 | 1 | NC | - | F8 | F^6 | L12 | L^6 |
| J13 | 1 | C12 | C^12 | F9 | F^7 | L10 | L^5 |
| J14 | 1 | C13 | C^13 | F10 | F^8 | L8 | L^4 |
| J12 | 1 | C14 | C^14 | F12 | F^9 | L6 | L^3 |
| H14 | 1 | C15 | C^15 | F13 | F^10 | L4 | L^2 |
| H13 | 1 | I | - | F14 | F^11 | L2 | L^1 |
| H12 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| G13 | 1 | NC | - | G14 | G^11 | M2 | M^1 |
| G14 | 1 | NC | - | G13 | G^10 | M4 | M^2 |
| G12 | 1 | D15 | D^15 | G12 | G^9 | M6 | M^3 |
| F14 | 1 | D14 | D^14 | G10 | G^8 | M8 | M^4 |
| F13 | 1 | D13 | D^13 | G9 | G^7 | M10 | M^5 |
| F12 | 1 | D12 | D^12 | G8 | G^6 | M12 | M^6 |
| E13 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| E14 | 1 | NC | - | G6 | G^5 | N2 | N^1 |
| E12 | 1 | D11 | D^11 | G5 | G^4 | N4 | N^2 |

## ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

| Pin Number | Bank Number | ispMACH 4128V | | ispMACH 4256V | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 1 | - | GND | - | GND | - |
| 2 | - | TDI | - | TDI | - |
| 3 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 4 | 0 | B0 | B^0 | C12 | C^6 |
| 5 | 0 | B1 | B^1 | C10 | C^5 |
| 6 | 0 | B2 | B^2 | C8 | C^4 |
| 7 | 0 | B4 | B^3 | C6 | C^3 |
| 8 | 0 | B5 | B^4 | C4 | C^2 |
| 9 | 0 | B6 | B^5 | C2 | C^1 |
| 10 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 11 | 0 | B8 | B^6 | D14 | D^7 |
| 12 | 0 | B9 | B^7 | D12 | D^6 |
| 13 | 0 | B10 | B^8 | D10 | D^5 |
| 14 | 0 | B12 | B^9 | D8 | D^4 |
| 15 | 0 | B13 | B^10 | D6 | D^3 |
| 16 | 0 | B14 | B^11 | D4 | D^2 |
| 17 | - | NC[2] | - | I[2] | - |
| 18 | 0 | GND (Bank 0)[1] | - | NC[1] | - |
| 19 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 20 | 0 | NC[2] | - | I[2] | - |
| 21 | 0 | C14 | C^11 | E2 | E^1 |
| 22 | 0 | C13 | C^10 | E4 | E^2 |
| 23 | 0 | C12 | C^9 | E6 | E^3 |
| 24 | 0 | C10 | C^8 | E8 | E^4 |
| 25 | 0 | C9 | C^7 | E10 | E^5 |
| 26 | 0 | C8 | C^6 | E12 | E^6 |
| 27 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 28 | 0 | C6 | C^5 | F2 | F^1 |
| 29 | 0 | C5 | C^4 | F4 | F^2 |
| 30 | 0 | C4 | C^3 | F6 | F^3 |
| 31 | 0 | C2 | C^2 | F8 | F^4 |
| 32 | 0 | C1 | C^1 | F10 | F^5 |
| 33 | 0 | C0 | C^0 | F12 | F^6 |
| 34 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 35 | - | TCK | - | TCK | - |
| 36 | - | VCC | - | VCC | - |
| 37 | - | GND | - | GND | - |
| 38 | 0 | NC[2] | - | I[2] | - |
| 39 | 0 | D14 | D^11 | G12 | G^6 |
| 40 | 0 | D13 | D^10 | G10 | G^5 |
| 41 | 0 | D12 | D^9 | G8 | G^4 |
| 42 | 0 | D10 | D^8 | G6 | G^3 |

## ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4256V/B/C/Z | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 142 | 1 | O0 | O^0 | GX0 | GX^0 | OX0 | OX^0 |
| 143 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| 144 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 145 | 1 | P14 | P^7 | HX14 | HX^7 | PX14 | PX^7 |
| 146 | 1 | P12 | P^6 | HX12 | HX^6 | PX12 | PX^6 |
| 147 | 1 | P10 | P^5 | HX10 | HX^5 | PX10 | PX^5 |
| 148 | 1 | P8 | P^4 | HX8 | HX^4 | PX8 | PX^4 |
| 149 | 1 | P6 | P^3 | HX6 | HX^3 | PX6 | PX^3 |
| 150 | 1 | P4 | P^2 | HX4 | HX^2 | PX4 | PX^2 |
| 151 | 1 | P2/GOE1 | P^1 | HX2/GOE1 | HX^1 | PX2/GOE1 | PX^1 |
| 152 | 1 | P0 | P^0 | HX0 | HX^0 | PX0 | PX^0 |
| 153 | - | GND | - | GND | - | GND | - |
| 154 | 1 | CLK3/I | - | CLK3/I | - | CLK3/I | - |
| 155 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 156 | 0 | CLK0/I | - | CLK0/I | - | CLK0/I | - |
| 157 | - | VCC | - | VCC | - | VCC | - |
| 158 | 0 | A0 | A^0 | A0 | A^0 | A0 | A^0 |
| 159 | 0 | A2/GOE0 | A^1 | A2/GOE0 | A^1 | A2//GOE0 | A^1 |
| 160 | 0 | A4 | A^2 | A4 | A^2 | A4 | A^2 |
| 161 | 0 | A6 | A^3 | A6 | A^3 | A6 | A^3 |
| 162 | 0 | A8 | A^4 | A8 | A^4 | A8 | A^4 |
| 163 | 0 | A10 | A^5 | A10 | A^5 | A10 | A^5 |
| 164 | 0 | A12 | A^6 | A12 | A^6 | A12 | A^6 |
| 165 | 0 | A14 | A^7 | A14 | A^7 | A14 | A^7 |
| 166 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 167 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 168 | 0 | B0 | B^0 | B0 | B^0 | B0 | B^0 |
| 169 | 0 | B2 | B^1 | B2 | B^1 | B2 | B^1 |
| 170 | 0 | B4 | B^2 | B4 | B^2 | B4 | B^2 |
| 171 | 0 | B6 | B^3 | B6 | B^3 | B6 | B^3 |
| 172 | 0 | B8 | B^4 | B8 | B^4 | B8 | B^4 |
| 173 | 0 | B10 | B^5 | B10 | B^5 | B10 | B^5 |
| 174 | 0 | B12 | B^6 | B12 | B^6 | B12 | B^6 |
| 175 | 0 | B14 | B^7 | B14 | B^7 | B14 | B^7 |
| 176 | - | VCC | - | VCC | - | VCC | - |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| E7 | 0 | NC | - | B1 | B^1 | F8 | F^4 | D12 | D^3 |
| A3 | 0 | B0 | B^0 | B2 | B^2 | B0 | B^0 | B0 | B^0 |
| F7 | 0 | B2 | B^1 | B4 | B^3 | B2 | B^1 | B2 | B^1 |
| B4 | 0 | B4 | B^2 | B6 | B^4 | B4 | B^2 | B4 | B^2 |
| C5 | 0 | B6 | B^3 | B8 | B^5 | B6 | B^3 | B6 | B^3 |
| A2 | 0 | B8 | B^4 | B9 | B^6 | B8 | B^4 | B8 | B^4 |
| E6 | 0 | B10 | B^5 | B10 | B^7 | B10 | B^5 | B10 | B^5 |
| B3 | 0 | B12 | B^6 | B12 | B^8 | B12 | B^6 | B12 | B^6 |
| C4 | 0 | B14 | B^7 | B14 | B^9 | B14 | B^7 | B14 | B^7 |
| D4 | 0 | NC | - | NC | - | D10 | D^5 | F0 | F^0 |
| E5 | 0 | NC | - | NC | - | D8 | D^4 | F2 | F^1 |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| - | - | - | - | - | - | GND | - | GND | - |
| - | 0 | - | - | - | - | GND (Bank 0) | - | GND (Bank 0) | - |

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

**ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | tPD | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4064ZC | LC4064ZC-5M132I | 64 | 1.8 | 5 | csBGA | 132 | 64 | I |
| | LC4064ZC-75M132I | 64 | 1.8 | 7.5 | csBGA | 132 | 64 | I |
| | LC4064ZC-5T100I | 64 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4064ZC-75T100I | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4064ZC-5M56I | 64 | 1.8 | 5 | csBGA | 56 | 34 | I |
| | LC4064ZC-75M56I | 64 | 1.8 | 7.5 | csBGA | 56 | 34 | I |
| | LC4064ZC-5T48I | 64 | 1.8 | 5 | TQFP | 48 | 32 | I |
| | LC4064ZC-75T48I | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | I |
| LC4128ZC | LC4128ZC-75M132I | 128 | 1.8 | 7.5 | csBGA | 132 | 96 | I |
| | LC4128ZC-75T100I | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| LC4256ZC | LC4256ZC-75T176I | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4256ZC-75M132I | 256 | 1.8 | 7.5 | csBGA | 132 | 96 | I |
| | LC4256ZC-75T100I | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | I |

**ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZC | LC4032ZC-75T48E | 32 | 1.8 | 7.5 | TQFP | 48 | 32 | E |
| LC4064ZC | LC4064ZC-75T100E | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | E |
| | LC4064ZC-75T48E | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | E |
| LC4128ZC | LC4128ZC-75T100E | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | E |
| LC4256ZC | LC4256ZC-75T176E | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | E |
| | LC4256ZC-75T100E | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | E |

**ispMACH 4000C (1.8V) Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032C | LC4032C-25T48C | 32 | 1.8 | 2.5 | TQFP | 48 | 32 | C |
| | LC4032C-5T48C | 32 | 1.8 | 5 | TQFP | 48 | 32 | C |
| | LC4032C-75T48C | 32 | 1.8 | 7.5 | TQFP | 48 | 32 | C |
| | LC4032C-25T44C | 32 | 1.8 | 2.5 | TQFP | 44 | 30 | C |
| | LC4032C-5T44C | 32 | 1.8 | 5 | TQFP | 44 | 30 | C |
| | LC4032C-75T44C | 32 | 1.8 | 7.5 | TQFP | 44 | 30 | C |
| LC4064C | LC4064C-25T100C | 64 | 1.8 | 2.5 | TQFP | 100 | 64 | C |
| | LC4064C-5T100C | 64 | 1.8 | 5 | TQFP | 100 | 64 | C |
| | LC4064C-75T100C | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | C |
| | LC4064C-25T48C | 64 | 1.8 | 2.5 | TQFP | 48 | 32 | C |
| | LC4064C-5T48C | 64 | 1.8 | 5 | TQFP | 48 | 32 | C |
| | LC4064C-75T48C | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | C |
| | LC4064C-25T44C | 64 | 1.8 | 2.5 | TQFP | 44 | 30 | C |
| | LC4064C-5T44C | 64 | 1.8 | 5 | TQFP | 44 | 30 | C |
| | LC4064C-75T44C | 64 | 1.8 | 7.5 | TQFP | 44 | 30 | C |

**ispMACH 4000V (3.3V) Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4128V | LC4128V-27T144C | 128 | 3.3 | 2.7 | TQFP | 144 | 96 | C |
| | LC4128V-5T144C | 128 | 3.3 | 5 | TQFP | 144 | 96 | C |
| | LC4128V-75T144C | 128 | 3.3 | 7.5 | TQFP | 144 | 96 | C |
| | LC4128V-27T128C | 128 | 3.3 | 2.7 | TQFP | 128 | 92 | C |
| | LC4128V-5T128C | 128 | 3.3 | 5 | TQFP | 128 | 92 | C |
| | LC4128V-75T128C | 128 | 3.3 | 7.5 | TQFP | 128 | 92 | C |
| | LC4128V-27T100C | 128 | 3.3 | 2.7 | TQFP | 100 | 64 | C |
| | LC4128V-5T100C | 128 | 3.3 | 5 | TQFP | 100 | 64 | C |
| | LC4128V-75T100C | 128 | 3.3 | 7.5 | TQFP | 100 | 64 | C |
| LC4256V | LC4256V-3FT256AC | 256 | 3.3 | 3 | ftBGA | 256 | 128 | C |
| | LC4256V-5FT256AC | 256 | 3.3 | 5 | ftBGA | 256 | 128 | C |
| | LC4256V-75FT256AC | 256 | 3.3 | 7.5 | ftBGA | 256 | 128 | C |
| | LC4256V-3FT256BC | 256 | 3.3 | 3 | ftBGA | 256 | 160 | C |
| | LC4256V-5FT256BC | 256 | 3.3 | 5 | ftBGA | 256 | 160 | C |
| | LC4256V-75FT256BC | 256 | 3.3 | 7.5 | ftBGA | 256 | 160 | C |
| | LC4256V-3F256AC[1] | 256 | 3.3 | 3 | fpBGA | 256 | 128 | C |
| | LC4256V-5F256AC[1] | 256 | 3.3 | 5 | fpBGA | 256 | 128 | C |
| | LC4256V-75F256AC[1] | 256 | 3.3 | 7.5 | fpBGA | 256 | 128 | C |
| | LC4256V-3F256BC[1] | 256 | 3.3 | 3 | fpBGA | 256 | 160 | C |
| | LC4256V-5F256BC[1] | 256 | 3.3 | 5 | fpBGA | 256 | 160 | C |
| | LC4256V-75F256BC[1] | 256 | 3.3 | 7.5 | fpBGA | 256 | 160 | C |
| | LC4256V-3T176C | 256 | 3.3 | 3 | TQFP | 176 | 128 | C |
| | LC4256V-5T176C | 256 | 3.3 | 5 | TQFP | 176 | 128 | C |
| | LC4256V-75T176C | 256 | 3.3 | 7.5 | TQFP | 176 | 128 | C |
| | LC4256V-3T144C | 256 | 3.3 | 3 | TQFP | 144 | 96 | C |
| | LC4256V-5T144C | 256 | 3.3 | 5 | TQFP | 144 | 96 | C |
| | LC4256V-75T144C | 256 | 3.3 | 7.5 | TQFP | 144 | 96 | C |
| | LC4256V-3T100C | 256 | 3.3 | 3 | TQFP | 100 | 64 | C |
| | LC4256V-5T100C | 256 | 3.3 | 5 | TQFP | 100 | 64 | C |
| | LC4256V-75T100C | 256 | 3.3 | 7.5 | TQFP | 100 | 64 | C |
| LC4384V | LC4384V-35FT256C | 384 | 3.3 | 3.5 | ftBGA | 256 | 192 | C |
| | LC4384V-5FT256C | 384 | 3.3 | 5 | ftBGA | 256 | 192 | C |
| | LC4384V-75FT256C | 384 | 3.3 | 7.5 | ftBGA | 256 | 192 | C |
| | LC4384V-35F256C[1] | 384 | 3.3 | 3.5 | fpBGA | 256 | 192 | C |
| | LC4384V-5F256C[1] | 384 | 3.3 | 5 | fpBGA | 256 | 192 | C |
| | LC4384V-75F256C[1] | 384 | 3.3 | 7.5 | fpBGA | 256 | 192 | C |
| | LC4384V-35T176C | 384 | 3.3 | 3.5 | TQFP | 176 | 128 | C |
| | LC4384V-5T176C | 384 | 3.3 | 5 | TQFP | 176 | 128 | C |
| | LC4384V-75T176C | 384 | 3.3 | 7.5 | TQFP | 176 | 128 | C |

**ispMACH 4000V (3.3V) Industrial Devices (Cont.)**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4256V | LC4256V-5FT256AI | 256 | 3.3 | 5 | ftBGA | 256 | 128 | I |
| | LC4256V-75FT256AI | 256 | 3.3 | 7.5 | ftBGA | 256 | 128 | I |
| | LC4256V-10FT256AI | 256 | 3.3 | 10 | ftBGA | 256 | 128 | I |
| | LC4256V-5FT256BI | 256 | 3.3 | 5 | ftBGA | 256 | 160 | I |
| | LC4256V-75FT256BI | 256 | 3.3 | 7.5 | ftBGA | 256 | 160 | I |
| | LC4256V-10FT256BI | 256 | 3.3 | 10 | ftBGA | 256 | 160 | I |
| | LC4256V-5F256AI[1] | 256 | 3.3 | 5 | fpBGA | 256 | 128 | I |
| | LC4256V-75F256AI[1] | 256 | 3.3 | 7.5 | fpBGA | 256 | 128 | I |
| | LC4256V-10F256AI[1] | 256 | 3.3 | 10 | fpBGA | 256 | 128 | I |
| | LC4256V-5F256BI[1] | 256 | 3.3 | 5 | fpBGA | 256 | 160 | I |
| | LC4256V-75F256BI[1] | 256 | 3.3 | 7.5 | fpBGA | 256 | 160 | I |
| | LC4256V-10F256BI[1] | 256 | 3.3 | 10 | fpBGA | 256 | 160 | I |
| | LC4256V-5T176I | 256 | 3.3 | 5 | TQFP | 176 | 128 | I |
| | LC4256V-75T176I | 256 | 3.3 | 7.5 | TQFP | 176 | 128 | I |
| | LC4256V-10T176I | 256 | 3.3 | 10 | TQFP | 176 | 128 | I |
| | LC4256V-5T144I | 256 | 3.3 | 5 | TQFP | 144 | 96 | I |
| | LC4256V-75T144I | 256 | 3.3 | 7.5 | TQFP | 144 | 96 | I |
| | LC4256V-10T144I | 256 | 3.3 | 10 | TQFP | 144 | 96 | I |
| | LC4256V-5T100I | 256 | 3.3 | 5 | TQFP | 100 | 64 | I |
| | LC4256V-75T100I | 256 | 3.3 | 7.5 | TQFP | 100 | 64 | I |
| | LC4256V-10T100I | 256 | 3.3 | 10 | TQFP | 100 | 64 | I |
| LC4384V | LC4384V-5FT256I | 384 | 3.3 | 5 | ftBGA | 256 | 192 | I |
| | LC4384V-75FT256I | 384 | 3.3 | 7.5 | ftBGA | 256 | 192 | I |
| | LC4384V-10FT256I | 384 | 3.3 | 10 | ftBGA | 256 | 192 | I |
| | LC4384V-5F256I[1] | 384 | 3.3 | 5 | fpBGA | 256 | 192 | I |
| | LC4384V-75F256I[1] | 384 | 3.3 | 7.5 | fpBGA | 256 | 192 | I |
| | LC4384V-10F256I[1] | 384 | 3.3 | 10 | fpBGA | 256 | 192 | I |
| | LC4384V-5T176I | 384 | 3.3 | 5 | TQFP | 176 | 128 | I |
| | LC4384V-75T176I | 384 | 3.3 | 7.5 | TQFP | 176 | 128 | I |
| | LC4384V-10T176I | 384 | 3.3 | 10 | TQFP | 176 | 128 | I |
| LC4512V | LC4512V-5FT256I | 512 | 3.3 | 5 | ftBGA | 256 | 208 | I |
| | LC4512V-75FT256I | 512 | 3.3 | 7.5 | ftBGA | 256 | 208 | I |
| | LC4512V-10FT256I | 512 | 3.3 | 10 | ftBGA | 256 | 208 | I |
| | LC4512V-5F256I[1] | 512 | 3.3 | 5 | fpBGA | 256 | 208 | I |
| | LC4512V-75F256I[1] | 512 | 3.3 | 7.5 | fpBGA | 256 | 208 | I |
| | LC4512V-10F256I[1] | 512 | 3.3 | 10 | fpBGA | 256 | 208 | I |
| | LC4512V-5T176I | 512 | 3.3 | 5 | TQFP | 176 | 128 | I |
| | LC4512V-75T176I | 512 | 3.3 | 7.5 | TQFP | 176 | 128 | I |
| | LC4512V-10T176I | 512 | 3.3 | 10 | TQFP | 176 | 128 | I |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## Revision History (Cont.)

| Date | Version | Change Summary |
|---|---|---|
| January 2004 | 20z | ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device. |
| | | Added new feature - ispMACH 4000Z supports operation down to 1.6V. |
| | | Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices. |
| April 2004 | 21z | Updated $I_{PU}$ (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150µA to -200µA. |
| November 2004 | 22z | Added User Electronic Signature section. |
| | | Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers. |
| December 2004 | 22z.1 | Updated Further Information section. |
| February 2006 | 22z.2 | Clarification to ispMACH 4000Z Input Leakage ($I_{IH}$) specification. |
| March 2007 | 22.3 | Updated ispMACH 4000 Introduction section. |
| | | Updated Signal Descriptions table. |
| June 2007 | 22.4 | Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet. |
| | | Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet. |
| | | Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices. |
| November 2007 | 23.0 | Added 256-ftBGA package Ordering Part Number information per PCN#14A-07. |
| May 2009 | 23.1 | Correction to $t_{CW}$, $t_{GW}$, $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000Z External Switching Characteristics table. |
| | | Correction to $t_{CW}$, $t_{GW}$, $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000V/B/C External Switching Characteristics table. |