



Welcome to [E-XFL.COM](http://E-XFL.COM)

## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128v-75tn100i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128v-75tn100i</a>



**Table 7. ORP Combinations for I/O Blocks with 16 I/Os**

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

**Table 8. ORP Combinations for I/O Blocks with 4 I/Os**

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

**Table 9. ORP Combinations for I/O Blocks with 10 I/Os**

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

**Table 10. ORP Combinations for I/O Blocks with 12 I/Os**

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

**ORP Bypass and Fast Output Multiplexers**

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster  $t_{CO}$ .

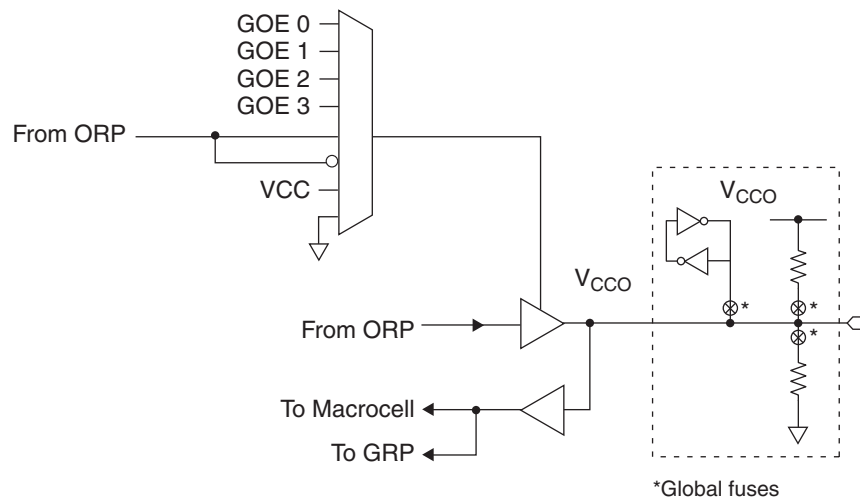
**Output Enable Routing Multiplexers**

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

**I/O Cell**

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

**Figure 8. I/O Cell**



Each output supports a variety of output standards dependent on the  $V_{CCO}$  supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the  $V_{CCO}$  supplied to its I/O bank. The I/O standards supported are:

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage ( $V_{CC}$ )	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage ( $V_{CCO}$ )	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied <sup>4, 5</sup>	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature ( $T_j$ ) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of ( $V_{IH}$  (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with  $V_{IN} > 3.6V$  is allowed.

### Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6 <sup>1, 2</sup>	1.9	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V	
	Supply Voltage for 3.3V Devices	3.0	3.6	V	
$T_j$	Junction Temperature (Commercial)	0	90	C	
	Junction Temperature (Industrial)	-40	105	C	
	Junction Temperature (Extended)	-40	130	C	

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

### Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

### Hot Socketing Characteristics<sup>1,2,3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DK}$	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$	—	±30	±200	µA

1. Insensitive to sequence of  $V_{CC}$  or  $V_{CCO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCO}$ , provided  $(V_{IN} - V_{CCO}) \leq 3.6V$ .
2.  $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}, I_{PD}$  or  $I_{BH}$ . Device defaults to pull-up until fuse circuitry is active.

## I/O Recommended Operating Conditions

Standard	$V_{CCO}$ (V) <sup>1</sup>	
	Min.	Max.
LVTTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3 <sup>2</sup>	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for  $V_{CCO}$  are the average of the min. and max. values.

2. ispMACH 4000Z only.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input Leakage Current (ispMACH 4000Z)	$0 \leq V_{IN} < V_{CCO}$	—	0.5	1	$\mu A$
$I_{IH}^1$	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \leq 5.5V$	—	—	10	$\mu A$
$I_{IL}, I_{IH}^1$	Input Leakage Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$	—	—	10	$\mu A$
		$0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$	—	—	15	$\mu A$
$I_{IH}^{1,2}$	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	20	$\mu A$
		$3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	50	$\mu A$
$I_{PU}$	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-150	$\mu A$
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-200	$\mu A$
$I_{PD}$	I/O Weak Pull-down Resistor Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$	30	—	150	$\mu A$
$I_{BHLS}$	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	$\mu A$
$I_{BHHS}$	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	$\mu A$
$I_{BHLO}$	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{BHT}$	—	—	150	$\mu A$
$I_{BHHO}$	Bus Hold High Overdrive Current	$V_{BHT} \leq V_{IN} \leq V_{CCO}$	—	—	-150	$\mu A$
$V_{BHT}$	Bus Hold Trip Points	—	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
$C_1$	I/O Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_2$	Clock Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_3$	Global Input Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where  $3.0V \leq V_{CCO} \leq 3.6V$ .

3.  $T_A = 25^\circ C, f = 1.0MHz$

4.  $I_{IH}$  excursions of up to 1.5 $\mu A$  maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

**ispMACH 4000V/B/C External Switching Characteristics (Cont.)**

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t <sub>S</sub>	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t <sub>R</sub>	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t <sub>RW</sub>	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
t <sub>G<sub>P<sub>TOE/DIS</sub></sub></sub>	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
t <sub>G<sub>OE/DIS</sub></sub>	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t <sub>CW</sub>	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	2.2	—	2.8	—	4.0	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
f <sub>MAX</sub> (Ext.)	Clock frequency with external feedback, [1/ (t <sub>S</sub> + t <sub>CO</sub> )]	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards. Timing v.3.2
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

## ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>GP</sub> TOE	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t <sub>P</sub> TOE	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2



**ispMACH 4000Z Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>P<sub>TOE</sub></sub>	Macrocell PT OE Delay	—	2.50	—	2.70	—	2.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details. Timing v.2.2

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:  
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B <sup>^</sup> 10	D4	D <sup>^</sup> 2	D10	D <sup>^</sup> 5
34	1	B11	B <sup>^</sup> 11	D6	D <sup>^</sup> 3	D8	D <sup>^</sup> 4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B <sup>^</sup> 12	D8	D <sup>^</sup> 4	D6	D <sup>^</sup> 3
39	1	B13	B <sup>^</sup> 13	D10	D <sup>^</sup> 5	D4	D <sup>^</sup> 2
40	1	B14	B <sup>^</sup> 14	D12	D <sup>^</sup> 6	D2	D <sup>^</sup> 1
41	1	B15/GOE1	B <sup>^</sup> 15	D14/GOE1	D <sup>^</sup> 7	D0/GOE1	D <sup>^</sup> 0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A <sup>^</sup> 0	A0/GOE0	A <sup>^</sup> 0	A0/GOE0	A <sup>^</sup> 0
45	0	A1	A <sup>^</sup> 1	A2	A <sup>^</sup> 1	A1	A <sup>^</sup> 1
46	0	A2	A <sup>^</sup> 2	A4	A <sup>^</sup> 2	A2	A <sup>^</sup> 2
47	0	A3	A <sup>^</sup> 3	A6	A <sup>^</sup> 3	A4	A <sup>^</sup> 3
48	0	A4	A <sup>^</sup> 4	A8	A <sup>^</sup> 4	A6	A <sup>^</sup> 4

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A <sup>^</sup> 5	A8	A <sup>^</sup> 5
C1	0	A6	A <sup>^</sup> 6	A10	A <sup>^</sup> 6
D1	0	A7	A <sup>^</sup> 7	A11	A <sup>^</sup> 7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
E1	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A <sup>^</sup> 8	B15	B <sup>^</sup> 7
G3	0	A9	A <sup>^</sup> 9	B12	B <sup>^</sup> 6
G1	0	A10	A <sup>^</sup> 10	B10	B <sup>^</sup> 5
H1	0	A11	A <sup>^</sup> 11	B8	B <sup>^</sup> 4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC <sup>1</sup>	-	I <sup>1</sup>	-
K4	0	A12	A <sup>^</sup> 12	B6	B <sup>^</sup> 3
H4	0	A13	A <sup>^</sup> 13	B4	B <sup>^</sup> 2
H5	0	A14	A <sup>^</sup> 14	B2	B <sup>^</sup> 1

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:  
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E3	0	NC	-	B8	B^6	D12	D^6
F2	0	A12	A^12	B9	B^7	D10	D^5
F1	0	A13	A^13	B10	B^8	D8	D^4
F3	0	A14	A^14	B12	B^9	D6	D^3
G1	0	A15	A^15	B13	B^10	D4	D^2
G2	0	I	-	B14	B^11	D2	D^1
G3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
H2	0	NC	-	C14	C^11	E2	E^1
H1	0	B15	B^15	C13	C^10	E4	E^2
H3	0	B14	B^14	C12	C^9	E6	E^3
J1	0	B13	B^13	C10	C^8	E8	E^4
J2	0	B12	B^12	C9	C^7	E10	E^5
J3	0	NC	-	C8	C^6	E12	E^6
K2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
K1	0	NC	-	C6	C^5	F2	F^1
K3	0	B11	B^11	C5	C^4	F4	F^2
L2	0	B10	B^10	C4	C^3	F6	F^3
L1	0	B9	B^9	C2	C^2	F8	F^4
L3	0	B8	B^8	C1	C^1	F10	F^5
M1	0	I	-	C0	C^0	F12	F^6
M2	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N1	-	TCK	-	TCK	-	TCK	-
P1	-	VCC	-	VCC	-	VCC	-
P2	-	GND	-	GND	-	GND	-
N2	0	I	-	D14	D^11	G12	G^6
P3	0	B7	B^7	D13	D^10	G10	G^5
M3	0	B6	B^6	D12	D^9	G8	G^4
N3	0	B5	B^5	D10	D^8	G6	G^3
P4	0	B4	B^4	D9	D^7	G4	G^2
M4	0	NC	-	D8	D^6	G2	G^1
N4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
P5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N5	0	NC	-	D6	D^5	H12	H^6
M5	0	B3	B^3	D5	D^4	H10	H^5
N6	0	B2	B^2	D4	D^3	H8	H^4
P6	0	B1	B^1	D2	D^2	H6	H^3
M6	0	B0	B^0	D1	D^1	H4	H^2
P7	0	NC	-	D0	D^0	H2	H^1
N7	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
M7	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
N8	-	VCC	-	VCC	-	VCC	-

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:  
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
P8	1	NC <sup>1</sup>	-	NC <sup>1</sup>	-	I <sup>1</sup>	-
M8	1	NC	-	E0	E <sup>0</sup>	I2	I <sup>1</sup>
P9	1	C0	C <sup>0</sup>	E1	E <sup>1</sup>	I4	I <sup>2</sup>
N9	1	C1	C <sup>1</sup>	E2	E <sup>2</sup>	I6	I <sup>3</sup>
M9	1	C2	C <sup>2</sup>	E4	E <sup>3</sup>	I8	I <sup>4</sup>
N10	1	C3	C <sup>3</sup>	E5	E <sup>4</sup>	I10	I <sup>5</sup>
P10	1	NC	-	E6	E <sup>5</sup>	I12	I <sup>6</sup>
M10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
N11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P11	1	NC	-	E8	E <sup>6</sup>	J2	J <sup>1</sup>
M11	1	C4	C <sup>4</sup>	E9	E <sup>7</sup>	J4	J <sup>2</sup>
P12	1	C5	C <sup>5</sup>	E10	E <sup>8</sup>	J6	J <sup>3</sup>
N12	1	C6	C <sup>6</sup>	E12	E <sup>9</sup>	J8	J <sup>4</sup>
P13	1	C7	C <sup>7</sup>	E13	E <sup>10</sup>	J10	J <sup>5</sup>
P14	1	NC	-	E14	E <sup>11</sup>	J12	J <sup>6</sup>
N14	-	GND	-	GND	-	GND	-
N13	-	TMS	-	TMS	-	TMS	-
M14	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
M12	1	NC	-	F0	F <sup>0</sup>	K12	K <sup>6</sup>
M13	1	C8	C <sup>8</sup>	F1	F <sup>1</sup>	K10	K <sup>5</sup>
L14	1	C9	C <sup>9</sup>	F2	F <sup>2</sup>	K8	K <sup>4</sup>
L12	1	C10	C <sup>10</sup>	F4	F <sup>3</sup>	K6	K <sup>3</sup>
L13	1	C11	C <sup>11</sup>	F5	F <sup>4</sup>	K4	K <sup>2</sup>
K14	1	NC	-	F6	F <sup>5</sup>	K2	K <sup>1</sup>
K13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
K12	1	NC	-	F8	F <sup>6</sup>	L12	L <sup>6</sup>
J13	1	C12	C <sup>12</sup>	F9	F <sup>7</sup>	L10	L <sup>5</sup>
J14	1	C13	C <sup>13</sup>	F10	F <sup>8</sup>	L8	L <sup>4</sup>
J12	1	C14	C <sup>14</sup>	F12	F <sup>9</sup>	L6	L <sup>3</sup>
H14	1	C15	C <sup>15</sup>	F13	F <sup>10</sup>	L4	L <sup>2</sup>
H13	1	I	-	F14	F <sup>11</sup>	L2	L <sup>1</sup>
H12	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
G13	1	NC	-	G14	G <sup>11</sup>	M2	M <sup>1</sup>
G14	1	NC	-	G13	G <sup>10</sup>	M4	M <sup>2</sup>
G12	1	D15	D <sup>15</sup>	G12	G <sup>9</sup>	M6	M <sup>3</sup>
F14	1	D14	D <sup>14</sup>	G10	G <sup>8</sup>	M8	M <sup>4</sup>
F13	1	D13	D <sup>13</sup>	G9	G <sup>7</sup>	M10	M <sup>5</sup>
F12	1	D12	D <sup>12</sup>	G8	G <sup>6</sup>	M12	M <sup>6</sup>
E13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
E14	1	NC	-	G6	G <sup>5</sup>	N2	N <sup>1</sup>
E12	1	D11	D <sup>11</sup>	G5	G <sup>4</sup>	N4	N <sup>2</sup>

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
C12	1	O0	O^0	O2	O^2	GX0	GX^0	OX0	OX^0
E10	1	NC	-	O1	O^1	CX8	CX^4	MX0	MX^0
A13	1	NC	-	O0	O^0	CX10	CX^5	MX4	MX^1
D12	1	NC	-	NC	-	NC	-	LX0	LX^0
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B12	1	NC	-	NC	-	NC	-	LX4	LX^1
A12	1	NC	-	NC	-	EX2	EX^1	LX8	LX^2
B11	1	NC	-	NC	-	EX0	EX^0	LX12	LX^3
A11	1	NC	-	P14	P^9	CX12	CX^6	MX8	MX^2
D10	1	NC	-	P12	P^8	CX14	CX^7	MX12	MX^3
C10	1	P14	P^7	P10	P^7	HX14	HX^7	PX14	PX^7
B10	1	P12	P^6	P9	P6	HX12	HX^6	PX12	PX^6
A10	1	P10	P^5	P8	P^5	HX10	HX^5	PX10	PX^5
A9	1	P8	P^4	P6	P^4	HX8	HX^4	PX8	PX^4
F9	1	P6	P^3	P4	P^3	HX6	HX^3	PX6	PX^3
B9	1	P4	P^2	P2	P^2	HX4	HX^2	PX4	PX^2
E9	1	P2/GOE1	P^1	P1/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE1	PX^1
C9	1	P0	P^0	P0	P^0	HX0	HX^0	PX0	PX^0
-	-	GND	-	GND	-	GND	-	GND	-
D9	1	CLK3/I	-	CLK3/I	-	CLK3/I	-	CLK3/I	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
B8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-	CLK0/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
D8	0	A0	A^0	A0	A^0	A0	A^0	A0	A^0
C8	0	A2/GOE0	A^1	A1/GOE0	A^1	A2/GOE0	A^1	A2/GOE0	A^1
A8	0	A4	A^2	A2	A^2	A4	A^2	A4	A^2
A7	0	A6	A^3	A4	A^3	A6	A^3	A6	A^3
B7	0	A8	A^4	A6	A^4	A8	A^4	A8	A^4
E8	0	A10	A^5	A8	A^5	A10	A^5	A10	A^5
D7	0	A12	A^6	A9	A^6	A12	A^6	A12	A^6
F8	0	A14	A^7	A10	A^7	A14	A^7	A14	A^7
C7	0	NC	-	A12	A^8	F14	F^7	D0	D^0
A6	0	NC	-	A14	A^9	F12	F^6	D4	D^1
B6	0	NC	-	NC	-	D14	D^7	E0	E^0
A5	0	NC	-	NC	-	D12	D^6	E4	E^1
B5	0	NC	-	NC	-	NC	-	E8	E^2
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
D5	0	NC	-	NC	-	NC	-	E12	E^3
A4	0	NC	-	B0	B^0	F10	F^5	D8	D^2

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B^1	F8	F^4	D12	D^3
A3	0	B0	B^0	B2	B^2	B0	B^0	B0	B^0
F7	0	B2	B^1	B4	B^3	B2	B^1	B2	B^1
B4	0	B4	B^2	B6	B^4	B4	B^2	B4	B^2
C5	0	B6	B^3	B8	B^5	B6	B^3	B6	B^3
A2	0	B8	B^4	B9	B^6	B8	B^4	B8	B^4
E6	0	B10	B^5	B10	B^7	B10	B^5	B10	B^5
B3	0	B12	B^6	B12	B^8	B12	B^6	B12	B^6
C4	0	B14	B^7	B14	B^9	B14	B^7	B14	B^7
D4	0	NC	-	NC	-	D10	D^5	F0	F^0
E5	0	NC	-	NC	-	D8	D^4	F2	F^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

## ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I <sup>1</sup>	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I <sup>1</sup>	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I <sup>1</sup>	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I <sup>1</sup>	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I <sup>1</sup>	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I <sup>1</sup>	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C

## ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-5FT256I	384	2.5	5	ftBGA	256	192	I
	LC4384B-75FT256I	384	2.5	7.5	ftBGA	256	192	I
	LC4384B-10FT256I	384	2.5	10	ftBGA	256	192	I
	LC4384B-5F256I <sup>1</sup>	384	2.5	5	fpBGA	256	192	I
	LC4384B-75F256I <sup>1</sup>	384	2.5	7.5	fpBGA	256	192	I
	LC4384B-10F256I <sup>1</sup>	384	2.5	10	fpBGA	256	192	I
	LC4384B-5T176I	384	2.5	5	TQFP	176	128	I
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128	I
	LC4384B-10T176I	384	2.5	10	TQFP	176	128	I
LC4512B	LC4512B-5FT256I	512	2.5	5	ftBGA	256	208	I
	LC4512B-75FT256I	512	2.5	7.5	ftBGA	256	208	I
	LC4512B-10FT256I	512	2.5	10	ftBGA	256	208	I
	LC4512B-5F256I <sup>1</sup>	512	2.5	5	fpBGA	256	208	I
	LC4512B-75F256I <sup>1</sup>	512	2.5	7.5	fpBGA	256	208	I
	LC4512B-10F256I <sup>1</sup>	512	2.5	10	fpBGA	256	208	I
	LC4512B-5T176I	512	2.5	5	TQFP	176	128	I
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
	LC4512B-10T176I	512	2.5	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32	C
	LC4032V-5T48C	32	3.3	5	TQFP	48	32	C
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32	C
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30	C
	LC4032V-5T44C	32	3.3	5	TQFP	44	30	C
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30	C
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64	C
	LC4064V-5T100C	64	3.3	5	TQFP	100	64	C
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64	C
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32	C
	LC4064V-5T48C	64	3.3	5	TQFP	48	32	C
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32	C
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30	C
	LC4064V-5T44C	64	3.3	5	TQFP	44	30	C
LC4064V-75T44C	64	3.3	7.5	TQFP	44	30	C	



## ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI <sup>1</sup>	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI <sup>1</sup>	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI <sup>1</sup>	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI <sup>1</sup>	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI <sup>1</sup>	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI <sup>1</sup>	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
LC4256V-10T100I	256	3.3	10	TQFP	100	64	I	
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I <sup>1</sup>	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I <sup>1</sup>	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I <sup>1</sup>	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I <sup>1</sup>	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I <sup>1</sup>	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I <sup>1</sup>	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)**

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices**

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

**ispMACH 4000C (1.8V) Lead-Free Commercial Devices**

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

## ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4512C	LC4512C-35FTN256C	512	1.8	3.5	Lead-free ftBGA	256	208	C
	LC4512C-5FTN256C	512	1.8	5	Lead-free ftBGA	256	208	C
	LC4512C-75FTN256C	512	1.8	7.5	Lead-free ftBGA	256	208	C
	LC4512C-35FN256C <sup>1</sup>	512	1.8	3.5	Lead-free fpBGA	256	208	C
	LC4512C-5FN256C <sup>1</sup>	512	1.8	5	Lead-free fpBGA	256	208	C
	LC4512C-75FN256C <sup>1</sup>	512	1.8	7.5	Lead-free fpBGA	256	208	C
	LC4512C-35TN176C	512	1.8	3.5	Lead-free TQFP	176	128	C
	LC4512C-5TN176C	512	1.8	5	Lead-free TQFP	176	128	C
LC4512C-75TN176C	512	1.8	7.5	Lead-free TQFP	176	128	C	

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000C (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032C-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I
	LC4032C-10TN48I	32	1.8	10	Lead-free TQFP	48	32	I
	LC4032C-5TN44I	32	1.8	5	Lead-free TQFP	44	30	I
	LC4032C-75TN44I	32	1.8	7.5	Lead-free TQFP	44	30	I
	LC4032C-10TN44I	32	1.8	10	Lead-free TQFP	44	30	I
LC4064C	LC4064C-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064C-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064C-10TN100I	64	1.8	10	Lead-free TQFP	100	64	I
	LC4064C-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064C-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
	LC4064C-10TN48I	64	1.8	10	Lead-free TQFP	48	32	I
	LC4064C-5TN44I	64	1.8	5	Lead-free TQFP	44	30	I
	LC4064C-75TN44I	64	1.8	5	Lead-free TQFP	44	30	I
LC4064C-10TN44I	64	1.8	10	Lead-free TQFP	44	30	I	
LC4128C	LC4128C-5TN128I	128	1.8	5	Lead-free TQFP	128	92	I
	LC4128C-75TN128I	128	1.8	7.5	Lead-free TQFP	128	92	I
	LC4128C-10TN128I	128	1.8	10	Lead-free TQFP	128	92	I
	LC4128C-5TN100I	128	1.8	5	Lead-free TQFP	100	64	I
	LC4128C-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
	LC4128C-10TN100I	128	1.8	10	Lead-free TQFP	100	64	I

## ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C <sup>1</sup>	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C <sup>1</sup>	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C <sup>1</sup>	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C <sup>1</sup>	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C <sup>1</sup>	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C <sup>1</sup>	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

## ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

## Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ( $0 \leq V_{IN} \leq 3.6V$ ).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided ( $V_{IN} - V_{CCO}$ ) $\leq$ 3.6V.
		Improved LC4064ZC t <sub>S</sub> to 2.5ns, t <sub>ST</sub> to 2.7ns and f <sub>MAX</sub> (Ext.) to 175MHz, LC4128ZC t <sub>CO</sub> to 3.5ns and f <sub>MAX</sub> (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs