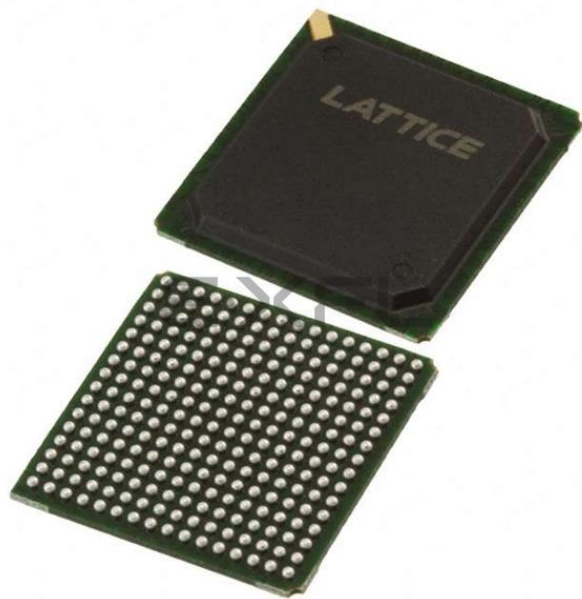




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	160
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-10f256bi

Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT n	Logic PT	Single PT for XOR/OR
PT $n+1$	Logic PT	Individual Clock (PT Clock)
PT $n+2$	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT $n+3$	Logic PT	Individual Initialization (PT Initialization)
PT $n+4$	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator $n+4$. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator

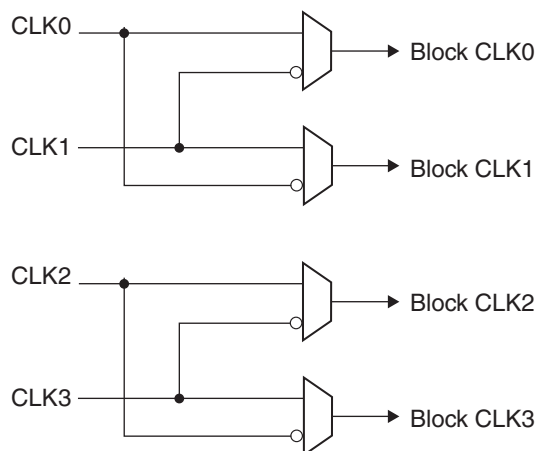


Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

- LVTTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

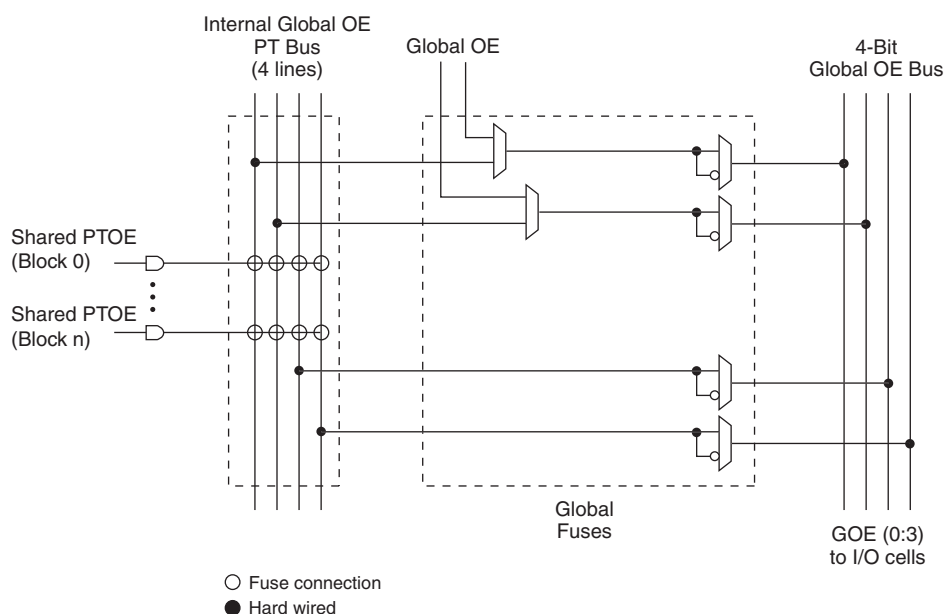
Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 device that has a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except ispMACH 4032



I/O Recommended Operating Conditions

Standard	V_{CCO} (V) ¹	
	Min.	Max.
LVTTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3 ²	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

2. ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input Leakage Current (ispMACH 4000Z)	$0 \leq V_{IN} < V_{CCO}$	—	0.5	1	μA
I_{IH}^1	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \leq 5.5V$	—	—	10	μA
I_{IL}, I_{IH}^1	Input Leakage Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$	—	—	10	μA
		$0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$	—	—	15	μA
$I_{IH}^{1,2}$	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	20	μA
		$3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	50	μA
I_{PU}	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-150	μA
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-200	μA
I_{PD}	I/O Weak Pull-down Resistor Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$	30	—	150	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{BHT}$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \leq V_{IN} \leq V_{CCO}$	—	—	-150	μA
V_{BHT}	Bus Hold Trip Points	—	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
C_1	I/O Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_2	Clock Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_3	Global Input Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \leq V_{CCO} \leq 3.6V$.

3. $T_A = 25^\circ C$, $f = 1.0MHz$

4. I_{IH} excursions of up to 1.5 μA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

ispMACH 4000Z Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.95	—	1.25	—	1.80	ns
t _{GOE}	Global OE Pin Delay	—	3.00	—	3.50	—	4.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.05	—	2.15	ns
t _{BUF}	Delay through Output Buffer	—	1.10	—	1.00	—	1.30	ns
t _{EN}	Output Enable Time	—	2.50	—	2.50	—	2.70	ns
t _{DIS}	Output Disable Time	—	2.50	—	2.50	—	2.70	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	2.25	—	2.05	—	2.50	ns
t _{MCELL}	Macrocell Delay	—	0.65	—	0.65	—	1.00	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	—	1.00	ns
t _{FBK}	Internal Feedback Delay	—	0.35	—	0.05	—	0.05	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.20	—	0.70	—	1.90	ns
t _{PDi}	Macrocell Propagation Delay	—	0.45	—	0.65	—	1.00	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	1.00	—	1.10	—	1.35	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	2.10	—	1.90	—	2.45	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.20	—	1.30	—	1.55	—	ns
t _{ST_PT}	T-register Setup Time (Product Term Clock)	2.30	—	2.10	—	2.75	—	ns
t _H	D-Register Hold Time	1.90	—	1.90	—	3.15	—	ns
t _{HT}	T-Resister Hold Time	1.90	—	1.90	—	3.15	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	1.30	—	1.10	—	0.75	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	1.30	—	1.50	—	1.95	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.00	—	1.00	—	1.18	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.75	—	1.15	—	1.05	ns
t _{CES}	Clock Enable Setup Time	2.00	—	2.00	—	2.00	—	ns
t _{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t _{SL}	Latch Setup Time (Global Clock)	1.00	—	1.00	—	1.65	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	2.10	—	1.90	—	2.15	—	ns
t _{HL}	Latch Hold Time	2.00	—	2.00	—	1.17	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t _{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.97	—	0.97	—	0.28	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.80	—	1.80	—	1.67	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.83	—	1.83	—	2.72	ns
t _{GPTOE}	Global PT OE Delay	—	4.30	—	4.20	—	3.50	ns

ispMACH 4000V/B/C Timing Adders¹ (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.00	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t _{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t _{BLA}	t _{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
K5	0	A15	A ¹⁵	B0	B ⁰
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B ⁰	C0	C ⁰
K7	1	B1	B ¹	C1	C ¹
K8	1	B2	B ²	C2	C ²
K9	1	B3	B ³	C4	C ³
K10	1	B4	B ⁴	C6	C ⁴
J10	-	TMS	-	TMS	-
H8	1	B5	B ⁵	C8	C ⁵
H10	1	B6	B ⁶	C10	C ⁶
G10	1	B7	B ⁷	C11	C ⁷
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC ¹	-	I ¹	-
F10	1	NC ¹	-	I ¹	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B ⁸	D15	D ⁷
D8	1	B9	B ⁹	D12	D ⁶
D10	1	B10	B ¹⁰	D10	D ⁵
C10	1	B11	B ¹¹	D8	D ⁴
B10	1	NC ¹	-	I ¹	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC ¹	-	I ¹	-
A7	1	B12	B ¹²	D6	D ³
C7	1	B13	B ¹³	D4	D ²
C6	1	B14	B ¹⁴	D2	D ¹
A6	1	B15/GOE1	B ¹⁵	D0/GOE1	D ⁰
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰
A4	0	A1	A ¹	A1	A ¹
A3	0	A2	A ²	A2	A ²
A2	0	A3	A ³	A4	A ³
A1	0	A4	A ⁴	A6	A ⁴

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D ³	H6	H ³	P12	P ³
85	1	D2	D ²	H4	H ²	P10	P ²
86	1	D1	D ¹	H2	H ¹	P6	P ¹
87	1	D0/GOE1	D ⁰	H0/GOE1	H ⁰	P2/OE1	P ⁰
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰	A2/GOE0	A ⁰
92	0	A1	A ¹	A2	A ¹	A6	A ¹
93	0	A2	A ²	A4	A ²	A10	A ²
94	0	A3	A ³	A6	A ³	A12	A ³
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A ⁴	A8	A ⁴	B2	B ⁰
98	0	A5	A ⁵	A10	A ⁵	B6	B ¹
99	0	A6	A ⁶	A12	A ⁶	B10	B ²
100	0	A7	A ⁷	A14	A ⁷	B12	B ³

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B ⁰
5	0	B1	B ¹
6	0	B2	B ²
7	0	B4	B ³
8	0	B5	B ⁴
9	0	B6	B ⁵
10	0	GND (Bank 0)	-
11	0	B8	B ⁶
12	0	B9	B ⁷
13	0	B10	B ⁸
14	0	B12	B ⁹
15	0	B13	B ¹⁰
16	0	B14	B ¹¹
17	0	VCCO (Bank 0)	-
18	0	C14	C ¹¹

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D [^] 7	G4	G [^] 2
44	0	D8	D [^] 6	G2	G [^] 1
45	0	NC ²	-	I ²	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D [^] 5	H12	H [^] 6
49	0	D5	D [^] 4	H10	H [^] 5
50	0	D4	D [^] 3	H8	H [^] 4
51	0	D2	D [^] 2	H6	H [^] 3
52	0	D1	D [^] 1	H4	H [^] 2
53	0	D0	D [^] 0	H2	H [^] 1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E [^] 0	I2	I [^] 1
59	1	E1	E [^] 1	I4	I [^] 2
60	1	E2	E [^] 2	I6	I [^] 3
61	1	E4	E [^] 3	I8	I [^] 4
62	1	E5	E [^] 4	I10	I [^] 5
63	1	E6	E [^] 5	I12	I [^] 6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E [^] 6	J2	J [^] 1
67	1	E9	E [^] 7	J4	J [^] 2
68	1	E10	E [^] 8	J6	J [^] 3
69	1	E12	E [^] 9	J8	J [^] 4
70	1	E13	E [^] 10	J10	J [^] 5
71	1	E14	E [^] 11	J12	J [^] 6
72	1	NC ²	-	I ²	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F [^] 0	K12	K [^] 6
77	1	F1	F [^] 1	K10	K [^] 5
78	1	F2	F [^] 2	K8	K [^] 4
79	1	F4	F [^] 3	K6	K [^] 3
80	1	F5	F [^] 4	K4	K [^] 2
81	1	F6	F [^] 5	K2	K [^] 1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F [^] 6	L14	L [^] 7
84	1	F9	F [^] 7	L12	L [^] 6
85	1	F10	F [^] 8	L10	L [^] 5

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L [^] 1
T5	0	NC	-	NC	-	I2	I [^] 1	L8	L [^] 2
R6	0	NC	-	NC	-	I0	I [^] 0	L12	L [^] 3
T6	0	NC	-	H14	H [^] 9	G12	G [^] 6	M8	M [^] 2
N7	0	NC	-	H12	H [^] 8	G14	G [^] 7	M12	M [^] 3
P7	0	H14	H [^] 7	H10	H [^] 7	L14	L [^] 7	P14	P [^] 7
R7	0	H12	H [^] 6	H9	H [^] 6	L12	L [^] 6	P12	P [^] 6
L8	0	H10	H [^] 5	H8	H [^] 5	L10	L [^] 5	P10	P [^] 5
T7	0	H8	H [^] 4	H6	H [^] 4	L8	L [^] 4	P8	P [^] 4
M8	0	H6	H [^] 3	H4	H [^] 3	L6	L [^] 3	P6	P [^] 3
N8	0	H4	H [^] 2	H2	H [^] 2	L4	L [^] 2	P4	P [^] 2
R8	0	H2	H [^] 1	H1	H [^] 1	L2	L [^] 1	P2	P [^] 1
P8	0	H0	H [^] 0	H0	H [^] 0	L0	L [^] 0	P0	P [^] 0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I [^] 0	I0	I [^] 0	M0	M [^] 0	AX0	AX [^] 0
R9	1	I2	I [^] 1	I1	I [^] 1	M2	M [^] 1	AX2	AX [^] 1
T9	1	I4	I [^] 2	I2	I [^] 2	M4	M [^] 2	AX4	AX [^] 2
T10	1	I6	I [^] 3	I4	I [^] 3	M6	M [^] 3	AX6	AX [^] 3
R10	1	I8	I [^] 4	I6	I [^] 4	M8	M [^] 4	AX8	AX [^] 4
M9	1	I10	I [^] 5	I8	I [^] 5	M10	M [^] 5	AX10	AX [^] 5
P10	1	I12	I [^] 6	I9	I [^] 6	M12	M [^] 6	AX12	AX [^] 6
L9	1	I14	I [^] 7	I10	I [^] 7	M14	M [^] 7	AX14	AX [^] 7
N10	1	NC	-	I12	I [^] 8	BX14	BX [^] 7	DX0	DX [^] 0
T11	1	NC	-	I14	I [^] 9	BX12	BX [^] 6	DX4	DX [^] 1
R11	1	NC	-	NC	-	P0	P [^] 0	EX0	EX [^] 0
T12	1	NC	-	NC	-	P2	P [^] 1	EX4	EX [^] 1
N12	1	NC	-	NC	-	NC	-	EX8	EX [^] 2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX [^] 3
T13	1	NC	-	J0	J [^] 0	BX10	BX [^] 5	DX8	DX [^] 2
P12	1	NC	-	J1	J [^] 1	BX8	BX [^] 4	DX12	DX [^] 3
M10	1	J0	J [^] 0	J2	J [^] 2	N0	N [^] 0	BX0	BX [^] 0
R13	1	J2	J [^] 1	J4	J [^] 3	N2	N [^] 1	BX2	BX [^] 1
L10	1	J4	J [^] 2	J6	J [^] 4	N4	N [^] 2	BX4	BX [^] 2
T14	1	J6	J [^] 3	J8	J [^] 5	N6	N [^] 3	BX6	BX [^] 3
M11	1	J8	J [^] 4	J9	J [^] 6	N8	N [^] 4	BX8	BX [^] 4

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J ⁵	J10	J ⁷	N10	N ⁵	BX10	BX ⁵
P13	1	J12	J ⁶	J12	J ⁸	N12	N ⁶	BX12	BX ⁶
N13	1	J14	J ⁷	J14	J ⁹	N14	N ⁷	BX14	BX ⁷
M12	1	NC	-	NC	-	P4	P ²	FX0	FX ⁰
T15	1	NC	-	NC	-	P6	P ³	FX2	FX ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX ²
R16	1	NC	-	NC	-	P8	P ⁴	FX6	FX ³
N14	1	NC	-	NC	-	P10	P ⁵	FX8	FX ⁴
P15	1	K14	K ⁷	K14	K ⁹	O14	O ⁷	CX14	CX ⁷
L11	1	K12	K ⁶	K12	K ⁸	O12	O ⁶	CX12	CX ⁶
P16	1	K10	K ⁵	K10	K ⁷	O10	O ⁵	CX10	CX ⁵
K11	1	K8	K ⁴	K9	K ⁶	O8	O ⁴	CX8	CX ⁴
M14	1	K6	K ³	K8	K ⁵	O6	O ³	CX6	CX ³
K12	1	K4	K ²	K6	K ⁴	O4	O ²	CX4	CX ²
N15	1	K2	K ¹	K4	K ³	O2	O ¹	CX2	CX ¹
N16	1	K0	K ⁰	K2	K ²	O0	O ⁰	CX0	CX ⁰
M15	1	NC	-	K1	K ¹	BX6	BX ³	HX0	HX ⁰
M13	1	NC	-	K0	K ⁰	BX4	BX ²	HX4	HX ¹
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX ⁵
L15	1	NC	-	NC	-	P12	P ⁶	FX12	FX ⁶
L16	1	NC	-	NC	-	P14	P ⁷	FX14	FX ⁷
J11	1	NC	-	L14	L ⁹	BX2	BX ¹	HX8	HX ²
K15	1	NC	-	L12	L ⁸	BX0	BX ⁰	HX12	HX ³
J12	1	L14	L ⁷	L10	L ⁷	AX14	AX ⁷	GX14	GX ⁷
K13	1	L12	L ⁶	L9	L ⁶	AX12	AX ⁶	GX12	GX ⁶
K14	1	L10	L ⁵	L8	L ⁵	AX10	AX ⁵	GX10	GX ⁵
K16	1	L8	L ⁴	L6	L ⁴	AX8	AX ⁴	GX8	GX ⁴
J16	1	L6	L ³	L4	L ³	AX6	AX ³	GX6	GX ³
J15	1	L4	L ²	L2	L ²	AX4	AX ²	GX4	GX ²
H16	1	L2	L ¹	L1	L ¹	AX2	AX ¹	GX2	GX ¹
J13	1	L0	L ⁰	L0	L ⁰	AX0	AX ⁰	GX0	GX ⁰
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M ⁰	M0	M ⁰	DX0	DX ⁰	JX0	JX ⁰

Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispMACH 4000Z devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

Conventional Packaging

ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35M56C	32	1.8	3.5	csBGA	56	32	C
	LC4032ZC-5M56C	32	1.8	5	csBGA	56	32	C
	LC4032ZC-75M56C	32	1.8	7.5	csBGA	56	32	C
	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32	C
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32	C
LC4064ZC	LC4064ZC-37M132C	64	1.8	3.7	csBGA	132	64	C
	LC4064ZC-5M132C	64	1.8	5	csBGA	132	64	C
	LC4064ZC-75M132C	64	1.8	7.5	csBGA	132	64	C
	LC4064ZC-37T100C	64	1.8	3.7	TQFP	100	64	C
	LC4064ZC-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064ZC-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064ZC-37M56C	64	1.8	3.7	csBGA	56	32	C
	LC4064ZC-5M56C	64	1.8	5	csBGA	56	32	C
	LC4064ZC-75M56C	64	1.8	7.5	csBGA	56	32	C
	LC4064ZC-37T48C	64	1.8	3.7	TQFP	48	32	C
	LC4064ZC-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064ZC-75T48C	64	1.8	7.5	TQFP	48	32	C
LC4128ZC	LC4128ZC-42M132C	128	1.8	4.2	csBGA	132	96	C
	LC4128ZC-75M132C	128	1.8	7.5	csBGA	132	96	C
	LC4128ZC-42T100C	128	1.8	4.2	TQFP	100	64	C
	LC4128ZC-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256ZC	LC4256ZC-45T176C	256	1.8	4.5	TQFP	176	128	C
	LC4256ZC-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256ZC-45M132C	256	1.8	4.5	csBGA	132	96	C
	LC4256ZC-75M132C	256	1.8	7.5	csBGA	132	96	C
	LC4256ZC-45T100C	256	1.8	4.5	TQFP	100	64	C
	LC4256ZC-75T100C	256	1.8	7.5	TQFP	100	64	C

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5M56I	32	1.8	5	csBGA	56	32	I
	LC4032ZC-75M56I	32	1.8	7.5	csBGA	56	32	I
	LC4032ZC-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032ZC-75T48I	32	1.8	7.5	TQFP	48	32	I

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI ¹	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI ¹	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI ¹	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI ¹	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI ¹	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI ¹	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC ¹	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC ¹	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC ¹	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC ¹	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC ¹	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC ¹	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C ¹	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C ¹	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C ¹	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C ¹	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C ¹	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C ¹	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

ispMACH 4000B (2.5V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128B	LC4128B-5TN128I	128	2.5	5	Lead-Free TQFP	128	92	I
	LC4128B-75TN128I	128	2.5	7.5	Lead-Free TQFP	128	92	I
	LC4128B-10TN128I	128	2.5	10	Lead-Free TQFP	128	92	I
	LC4128B-5TN100I	128	2.5	5	Lead-Free TQFP	100	64	I
	LC4128B-75TN100I	128	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4128B-10TN100I	128	2.5	10	Lead-Free TQFP	100	64	I
LC4256B	LC4256B-5FTN256AI	256	2.5	5	Lead-Free ftBGA	256	128	I
	LC4256B-75FTN256AI	256	2.5	7.5	Lead-Free ftBGA	256	128	I
	LC4256B-10FTN256AI	256	2.5	10	Lead-Free ftBGA	256	128	I
	LC4256B-5FTN256BI	256	2.5	5	Lead-Free ftBGA	256	160	I
	LC4256B-75FTN256BI	256	2.5	7.5	Lead-Free ftBGA	256	160	I
	LC4256B-10FTN256BI	256	2.5	10	Lead-Free ftBGA	256	160	I
	LC4256B-5FN256AI ¹	256	2.5	5	Lead-Free fpBGA	256	128	I
	LC4256B-75FN256AI ¹	256	2.5	7.5	Lead-Free fpBGA	256	128	I
	LC4256B-10FN256AI ¹	256	2.5	10	Lead-Free fpBGA	256	128	I
	LC4256B-5FN256BI ¹	256	2.5	5	Lead-Free fpBGA	256	160	I
	LC4256B-75FN256BI ¹	256	2.5	7.5	Lead-Free fpBGA	256	160	I
	LC4256B-10FN256BI ¹	256	2.5	10	Lead-Free fpBGA	256	160	I
	LC4256B-5TN176I	256	2.5	5	Lead-Free TQFP	176	128	I
	LC4256B-75TN176I	256	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4256B-10TN176I	256	2.5	10	Lead-Free TQFP	176	128	I
	LC4256B-5TN100I	256	2.5	5	Lead-Free TQFP	100	64	I
	LC4256B-75TN100I	256	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4256B-10TN100I	256	2.5	10	Lead-Free TQFP	100	64	I
LC4384B	LC4384B-5FTN256I	384	2.5	5	Lead-Free ftBGA	256	192	I
	LC4384B-75FTN256I	384	2.5	7.5	Lead-Free ftBGA	256	192	I
	LC4384B-10FTN256I	384	2.5	10	Lead-Free ftBGA	256	192	I
	LC4384B-5FN256I ¹	384	2.5	5	Lead-Free fpBGA	256	192	I
	LC4384B-75FN256I ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	I
	LC4384B-10FN256I ¹	384	2.5	10	Lead-Free fpBGA	256	192	I
	LC4384B-5TN176I	384	2.5	5	Lead-Free TQFP	176	128	I
	LC4384B-75TN176I	384	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4384B-10TN176I	384	2.5	10	Lead-Free TQFP	176	128	I
LC4512B	LC4512B-5FTN256I	512	2.5	5	Lead-Free ftBGA	256	208	I
	LC4512B-75FTN256I	512	2.5	7.5	Lead-Free ftBGA	256	208	I
	LC4512B-10FTN256I	512	2.5	10	Lead-Free ftBGA	256	208	I
	LC4512B-5FN256I ¹	512	2.5	5	Lead-Free fpBGA	256	208	I
	LC4512B-75FN256I ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	I
	LC4512B-10FN256I ¹	512	2.5	10	Lead-Free fpBGA	256	208	I
	LC4512B-5TN176I	512	2.5	5	Lead-Free TQFP	176	128	I
	LC4512B-75TN176I	512	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4512B-10TN176I	512	2.5	10	Lead-Free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-3FTN256AC	256	3.3	3	Lead-free ftBGA	256	128	C
	LC4256V-5FTN256AC	256	3.3	5	Lead-free ftBGA	256	128	C
	LC4256V-75FTN256AC	256	3.3	7.5	Lead-free ftBGA	256	128	C
	LC4256V-3FTN256BC	256	3.3	3	Lead-free ftBGA	256	160	C
	LC4256V-5FTN256BC	256	3.3	5	Lead-free ftBGA	256	160	C
	LC4256V-75FTN256BC	256	3.3	7.5	Lead-free ftBGA	256	160	C
	LC4256V-3FN256AC ¹	256	3.3	3	Lead-free fpBGA	256	128	C
	LC4256V-5FN256AC ¹	256	3.3	5	Lead-free fpBGA	256	128	C
	LC4256V-75FN256AC ¹	256	3.3	7.5	Lead-free fpBGA	256	128	C
	LC4256V-3FN256BC ¹	256	3.3	3	Lead-free fpBGA	256	160	C
	LC4256V-5FN256BC ¹	256	3.3	5	Lead-free fpBGA	256	160	C
	LC4256V-75FN256BC ¹	256	3.3	7.5	Lead-free fpBGA	256	160	C
	LC4256V-3TN176C	256	3.3	3	Lead-free TQFP	176	128	C
	LC4256V-5TN176C	256	3.3	5	Lead-free TQFP	176	128	C
	LC4256V-75TN176C	256	3.3	7.5	Lead-free TQFP	176	128	C
	LC4256V-3TN144C	256	3.3	3	Lead-free TQFP	144	96	C
	LC4256V-5TN144C	256	3.3	5	Lead-free TQFP	144	96	C
	LC4256V-75TN144C	256	3.3	7.5	Lead-free TQFP	144	96	C
	LC4256V-3TN100C	256	3.3	3	Lead-free TQFP	100	64	C
	LC4256V-5TN100C	256	3.3	5	Lead-free TQFP	100	64	C
	LC4256V-75TN100C	256	3.3	7.5	Lead-free TQFP	100	64	C
LC4384V	LC4384V-35FTN256C	384	3.3	3.5	Lead-free ftBGA	256	192	C
	LC4384V-5FTN256C	384	3.3	5	Lead-free ftBGA	256	192	C
	LC4384V-75FTN256C	384	3.3	7.5	Lead-free ftBGA	256	192	C
	LC4384V-35FN256C ¹	384	3.3	3.5	Lead-free fpBGA	256	192	C
	LC4384V-5FN256C ¹	384	3.3	5	Lead-free fpBGA	256	192	C
	LC4384V-75FN256C ¹	384	3.3	7.5	Lead-free fpBGA	256	192	C
	LC4384V-35TN176C	384	3.3	3.5	Lead-free TQFP	176	128	C
	LC4384V-5TN176C	384	3.3	5	Lead-free TQFP	176	128	C
	LC4384V-75TN176C	384	3.3	7.5	Lead-free TQFP	176	128	C
LC4512V	LC4512V-35FTN256C	512	3.3	3.5	Lead-free ftBGA	256	208	C
	LC4512V-5FTN256C	512	3.3	5	Lead-free ftBGA	256	208	C
	LC4512V-75FTN256C	512	3.3	7.5	Lead-free ftBGA	256	208	C
	LC4512V-35FN256C ¹	512	3.3	3.5	Lead-free fpBGA	256	208	C
	LC4512V-5FN256C ¹	512	3.3	5	Lead-free fpBGA	256	208	C
	LC4512V-75FN256C ¹	512	3.3	7.5	Lead-free fpBGA	256	208	C
	LC4512V-35TN176C	512	3.3	3.5	Lead-free TQFP	176	128	C
	LC4512V-5TN176C	512	3.3	5	Lead-free TQFP	176	128	C
	LC4512V-75TN176C	512	3.3	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ($0 \leq V_{IN} \leq 3.6V$).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
		Improved LC4064ZC t _S to 2.5ns, t _{ST} to 2.7ns and f _{MAX} (Ext.) to 175MHz, LC4128ZC t _{CO} to 3.5ns and f _{MAX} (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs