



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	128
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-10ftn256ai

Table 2. ispMACH 4000Z Family Selection Guide

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t _{PD} (ns)	3.5	3.7	4.2	4.5
t _S (ns)	2.2	2.5	2.7	2.9
t _{CO} (ns)	3.0	3.2	3.5	3.8
f _{MAX} (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I _{CC} (μA)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram

The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CC0} of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

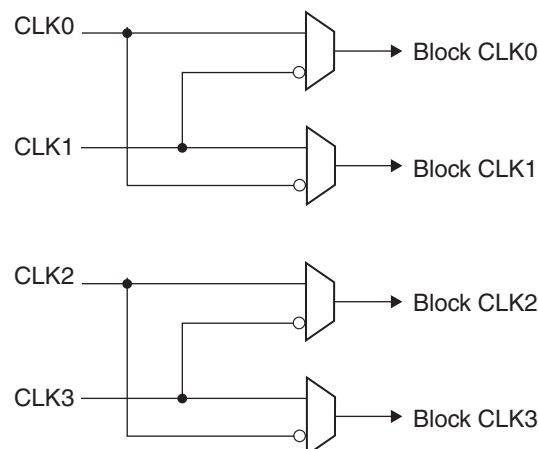
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



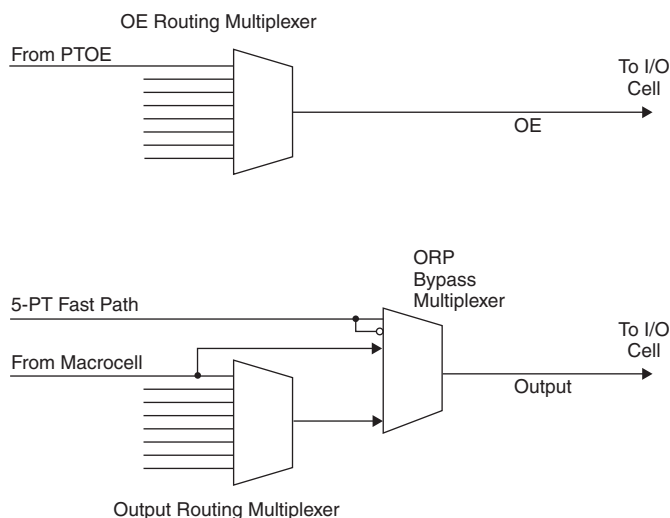
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	341	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	361	—	μA
		V _{CC} = 1.9V, T _A = 85°C	—	372	—	μA
		V _{CC} = 1.9V, T _A = 125°C	—	468	—	μA
ICC ^{4, 5}	Standby Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	13	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	32	55	μA
		V _{CC} = 1.9V, T _A = 85°C	—	43	90	μA
		V _{CC} = 1.9V, T _A = 125°C	—	135	—	μA

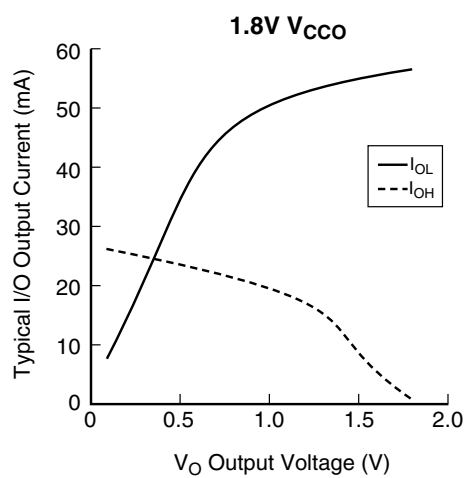
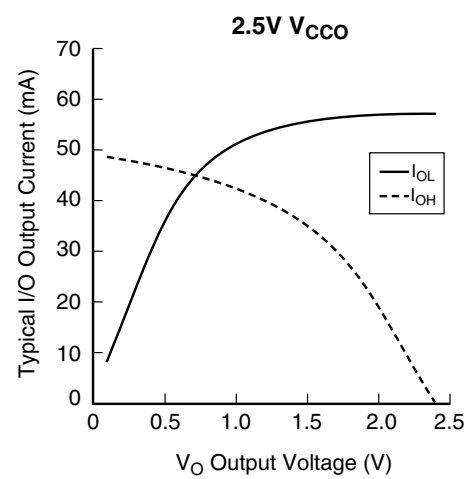
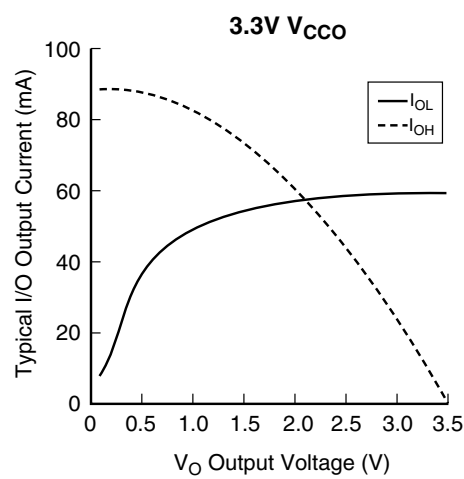
1. T_A = 25°C, frequency = 1.0 MHz.

2. Device configured with 16-bit counters.

3. I_{CC} varies with specific device configuration and operating frequency.

4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.

5. Includes V_{CCO} current without output loading.



ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
t _S	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
t _{ST}	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
t _{SIR}	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
t _R	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
t _{RW}	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
t _{CW}	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
t _{WIR}	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
f _{MAX} (Ext.)	clock frequency with external feedback, [1 / (t _S + t _{CO})]	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

ispMACH 4000Z External Switching Characteristics (Cont.)**Over Recommended Operating Conditions**

Parameter	Description ^{1, 2, 3}	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t _S	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t _{ST}	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t _{SIR}	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t _R	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t _{RW}	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t _{CW}	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t _{WIR}	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f _{MAX} (Ext.)	clock frequency with external feedback, [1 / (t _S + t _{CO})]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

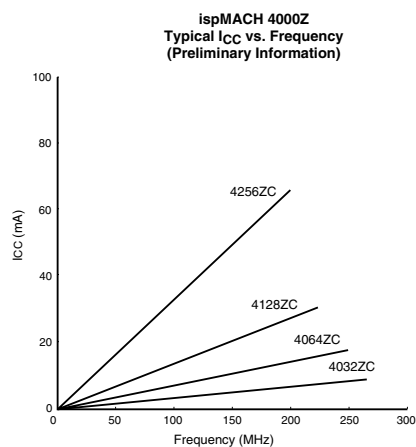
Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

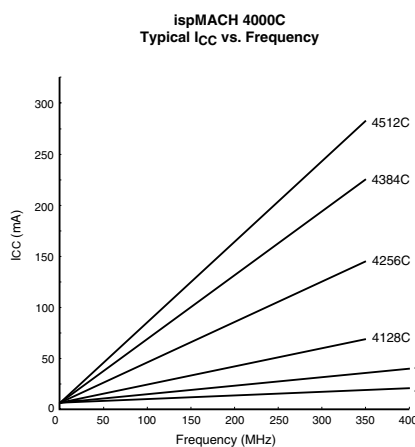
3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

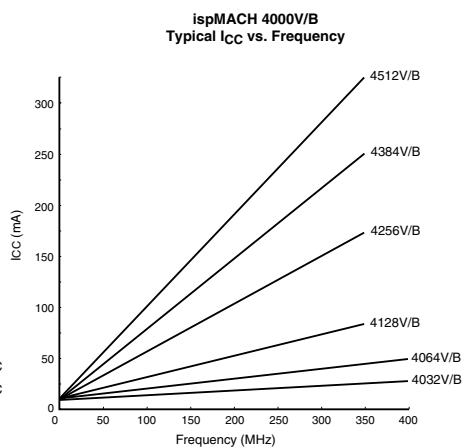
Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

Power Estimation Coefficients¹

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A ⁸	B0	B ⁰	C12	C ³
4	0	A9	A ⁹	B2	B ¹	C10	C ²
5	0	A10	A ¹⁰	B4	B ²	C6	C ¹
6	0	A11	A ¹¹	B6	B ³	C2	C ⁰
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A ¹²	B8	B ⁴	D12	D ³
9	0	A13	A ¹³	B10	B ⁵	D10	D ²
10	0	A14	A ¹⁴	B12	B ⁶	D6	D ¹
11	0	A15	A ¹⁵	B13	B ⁷	D4	D ⁰
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B ¹⁵	C14	C ⁷	E4	E ⁰
15	0	B14	B ¹⁴	C12	C ⁶	E6	E ¹
16	0	B13	B ¹³	C10	C ⁵	E10	E ²
17	0	B12	B ¹²	C8	C ⁴	E12	E ³
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B ¹¹	C6	C ³	F2	F ⁰
20	0	B10	B ¹⁰	C5	C ²	F6	F ¹
21	0	B9	B ⁹	C4	C ¹	F10	F ²
22	0	B8	B ⁸	C2	C ⁰	F12	F ³
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B ⁷	D13	D ⁷	G12	G ³
29	0	B6	B ⁶	D12	D ⁶	G10	G ²
30	0	B5	B ⁵	D10	D ⁵	G6	G ¹
31	0	B4	B ⁴	D8	D ⁴	G2	G ⁰
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B ³	D6	D ³	H12	H ³
35	0	B2	B ²	D4	D ²	H10	H ²
36	0	B1	B ¹	D2	D ¹	H6	H ¹
37	0	B0	B ⁰	D0	D ⁰	H2	H ⁰
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C ⁰	E0	E ⁰	I2	I ⁰

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C ¹	E2	E ¹	I6	I ¹
43	1	C2	C ²	E4	E ²	I10	I ²
44	1	C3	C ³	E6	E ³	I12	I ³
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C ⁴	E8	E ⁴	J2	J ⁰
48	1	C5	C ⁵	E10	E ⁵	J6	J ¹
49	1	C6	C ⁶	E12	E ⁶	J10	J ²
50	1	C7	C ⁷	E14	E ⁷	J12	J ³
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C ⁸	F0	F ⁰	K12	K ³
54	1	C9	C ⁹	F2	F ¹	K10	K ²
55	1	C10	C ¹⁰	F4	F ²	K6	K ¹
56	1	C11	C ¹¹	F6	F ³	K2	K ⁰
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C ¹²	F8	F ⁴	L12	L ³
59	1	C13	C ¹³	F10	F ⁵	L10	L ²
60	1	C14	C ¹⁴	F12	F ⁶	L6	L ¹
61	1	C15	C ¹⁵	F13	F ⁷	L4	L ⁰
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D ¹⁵	G14	G ⁷	M4	M ⁰
65	1	D14	D ¹⁴	G12	G ⁶	M6	M ¹
66	1	D13	D ¹³	G10	G ⁵	M10	M ²
67	1	D12	D ¹²	G8	G ⁴	M12	M ³
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D ¹¹	G6	G ³	N2	N ⁰
70	1	D10	D ¹⁰	G5	G ²	N6	N ¹
71	1	D9	D ⁹	G4	G ¹	N10	N ²
72	1	D8	D ⁸	G2	G ⁰	N12	N ³
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D ⁷	H13	H ⁷	O12	O ³
79	1	D6	D ⁶	H12	H ⁶	O10	O ²
80	1	D5	D ⁵	H10	H ⁵	O6	O ¹
81	1	D4	D ⁴	H8	H ⁴	O2	O ⁰
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C ¹⁰
20	0	C12	C ⁹
21	0	C10	C ⁸
22	0	C9	C ⁷
23	0	C8	C ⁶
24	0	GND (Bank 0)	-
25	0	C6	C ⁵
26	0	C5	C ⁴
27	0	C4	C ³
28	0	C2	C ²
29	0	C0	C ⁰
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D ¹¹
35	0	D13	D ¹⁰
36	0	D12	D ⁹
37	0	D10	D ⁸
38	0	D9	D ⁷
39	0	D8	D ⁶
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D ⁵
43	0	D5	D ⁴
44	0	D4	D ³
45	0	D2	D ²
46	0	D1	D ¹
47	0	D0	D ⁰
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E ⁰
53	1	E1	E ¹
54	1	E2	E ²
55	1	E4	E ³
56	1	E5	E ⁴
57	1	E6	E ⁵
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E ⁶
61	1	E9	E ⁷

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
60	0	H8	H ⁴	L8	L ⁴	P8	P ⁴
61	0	H6	H ³	L6	L ³	P6	P ³
62	0	H4	H ²	L4	L ²	P4	P ²
63	0	H2	H ¹	L2	L ¹	P2	P ¹
64	0	H0	H ⁰	L0	L ⁰	P0	P ⁰
65	-	GND	-	GND	-	GND	-
66	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
67	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
68	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
69	-	VCC	-	VCC	-	VCC	-
70	1	I0	I ⁰	M0	M ⁰	AX0	AX ⁰
71	1	I2	I ¹	M2	M ¹	AX2	AX ¹
72	1	I4	I ²	M4	M ²	AX4	AX ²
73	1	I6	I ³	M6	M ³	AX6	AX ³
74	1	I8	I ⁴	M8	M ⁴	AX8	AX ⁴
75	1	I10	I ⁵	M10	M ⁵	AX10	AX ⁵
76	1	I12	I ⁶	M12	M ⁶	AX12	AX ⁶
77	1	I14	I ⁷	M14	M ⁷	AX14	AX ⁷
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
79	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
80	1	J0	J ⁰	N0	N ⁰	BX0	BX ⁰
81	1	J2	J ¹	N2	N ¹	BX2	BX ¹
82	1	J4	J ²	N4	N ²	BX4	BX ²
83	1	J6	J ³	N6	N ³	BX6	BX ³
84	1	J8	J ⁴	N8	N ⁴	BX8	BX ⁴
85	1	J10	J ⁵	N10	N ⁵	BX10	BX ⁵
86	1	J12	J ⁶	N12	N ⁶	BX12	BX ⁶
87	1	J14	J ⁷	N14	N ⁷	BX14	BX ⁷
88	-	VCC	-	VCC	-	VCC	-
89	-	NC	-	NC	-	NC	-
90	-	GND	-	GND	-	GND	-
91	-	TMS	-	TMS	-	TMS	-
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
93	1	K14	K ⁷	O14	O ⁷	CX14	CX ⁷
94	1	K12	K ⁶	O12	O ⁶	CX12	CX ⁶
95	1	K10	K ⁵	O10	O ⁵	CX10	CX ⁵
96	1	K8	K ⁴	O8	O ⁴	CX8	CX ⁴
97	1	K6	K ³	O6	O ³	CX6	CX ³
98	1	K4	K ²	O4	O ²	CX4	CX ²
99	1	K2	K ¹	O2	O ¹	CX2	CX ¹
100	1	K0	K ⁰	O0	O ⁰	CX0	CX ⁰

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E ⁷	E10	E ⁷	H14	H ⁷	J14	J ⁷
K3	0	NC	-	E12	E ⁸	G0	G ⁰	I0	I ⁰
K4	0	NC	-	E14	E ⁹	G2	G ¹	I4	I ¹
L1	0	NC	-	NC	-	I14	I ⁷	K0	K ⁰
L2	0	NC	-	NC	-	I12	I ⁶	K2	K ¹
M1	0	NC	-	NC	-	NC	-	K4	K ²
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K ³
N1	0	NC	-	NC	-	I10	I ⁵	K8	K ⁴
M3	0	NC	-	NC	-	I8	I ⁴	K10	K ⁵
M4	0	NC	-	F0	F ⁰	G4	G ²	I8	I ²
N2	0	NC	-	F1	F ¹	G6	G ³	I12	I ³
K5	0	F0	F ⁰	F2	F ²	J0	J ⁰	N0	N ⁰
P1	0	F2	F ¹	F4	F ³	J2	J ¹	N2	N ¹
K6	0	F4	F ²	F6	F ⁴	J4	J ²	N4	N ²
N3	0	F6	F ³	F8	F ⁵	J6	J ³	N6	N ³
L5	0	F8	F ⁴	F9	F ⁶	J8	J ⁴	N8	N ⁴
P2	0	F10	F ⁵	F10	F ⁷	J10	J ⁵	N10	N ⁵
L6	0	F12	F ⁶	F12	F ⁸	J12	J ⁶	N12	N ⁶
R1	0	F14	F ⁷	F14	F ⁹	J14	J ⁷	N14	N ⁷
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G ⁹	I6	I ³	K12	K ⁶
M5	0	NC	-	G12	G ⁸	I4	I ²	K14	K ⁷
N4	0	G14	G ⁷	G10	G ⁷	K14	K ⁷	O14	O ⁷
T3	0	G12	G ⁶	G9	G ⁶	K12	K ⁶	O12	O ⁶
R3	0	G10	G ⁵	G8	G ⁵	K10	K ⁵	O10	O ⁵
M6	0	G8	G ⁴	G6	G ⁴	K8	K ⁴	O8	O ⁴
P4	0	G6	G ³	G4	G ³	K6	K ³	O6	O ³
L7	0	G4	G ²	G2	G ²	K4	K ²	O4	O ²
N5	0	G2	G ¹	G1	G ¹	K2	K ¹	O2	O ¹
M7	0	G0	G ⁰	G0	G ⁰	K0	K ⁰	O0	O ⁰
P5	0	NC	-	NC	-	G8	G ⁴	M0	M ⁰
R4	0	NC	-	NC	-	G10	G ⁵	M4	M ¹
T4	0	NC	-	NC	-	NC	-	L0	L ⁰
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC ¹	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC ¹	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC ¹	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC ¹	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC ¹	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC ¹	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C ¹	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C ¹	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C ¹	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI ¹	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI ¹	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI ¹	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI ¹	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI ¹	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI ¹	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I ¹	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I ¹	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I ¹	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I ¹	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I ¹	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I ¹	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
	LC4064B-75TN44C	64	2.5	7.5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC ¹	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC ¹	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC ¹	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC ¹	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC ¹	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC ¹	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
	LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C
	LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C

ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FTN256AI	256	3.3	5	Lead-free ftBGA	256	128	I
	LC4256V-75FTN256AI	256	3.3	7.5	Lead-free ftBGA	256	128	I
	LC4256V-10FTN256AI	256	3.3	10	Lead-free ftBGA	256	128	I
	LC4256V-5FTN256BI	256	3.3	5	Lead-free ftBGA	256	160	I
	LC4256V-75FTN256BI	256	3.3	7.5	Lead-free ftBGA	256	160	I
	LC4256V-10FTN256BI	256	3.3	10	Lead-free ftBGA	256	160	I
	LC4256V-5FN256AI ¹	256	3.3	5	Lead-free fpBGA	256	128	I
	LC4256V-75FN256AI ¹	256	3.3	7.5	Lead-free fpBGA	256	128	I
	LC4256V-10FN256AI ¹	256	3.3	10	Lead-free fpBGA	256	128	I
	LC4256V-5FN256BI ¹	256	3.3	5	Lead-free fpBGA	256	160	I
	LC4256V-75FN256BI ¹	256	3.3	7.5	Lead-free fpBGA	256	160	I
	LC4256V-10FN256BI ¹	256	3.3	10	Lead-free fpBGA	256	160	I
	LC4256V-5TN176I	256	3.3	5	Lead-free TQFP	176	128	I
	LC4256V-75TN176I	256	3.3	7.5	Lead-free TQFP	176	128	I
	LC4256V-10TN176I	256	3.3	10	Lead-free TQFP	176	128	I
	LC4256V-5TN144I	256	3.3	5	Lead-free TQFP	144	96	I
	LC4256V-75TN144I	256	3.3	7.5	Lead-free TQFP	144	96	I
	LC4256V-10TN144I	256	3.3	10	Lead-free TQFP	144	96	I
	LC4256V-5TN100I	256	3.3	5	Lead-free TQFP	100	64	I
	LC4256V-75TN100I	256	3.3	7.5	Lead-free TQFP	100	64	I
	LC4256V-10TN100I	256	3.3	10	Lead-free TQFP	100	64	I
LC4384V	LC4384V-5FTN256I	384	3.3	5	Lead-free ftBGA	256	192	I
	LC4384V-75FTN256I	384	3.3	7.5	Lead-free ftBGA	256	192	I
	LC4384V-10FTN256I	384	3.3	10	Lead-free ftBGA	256	192	I
	LC4384V-5FN256I ¹	384	3.3	5	Lead-free fpBGA	256	192	I
	LC4384V-75FN256I ¹	384	3.3	7.5	Lead-free fpBGA	256	192	I
	LC4384V-10FN256I ¹	384	3.3	10	Lead-free fpBGA	256	192	I
	LC4384V-5TN176I	384	3.3	5	Lead-free TQFP	176	128	I
	LC4384V-75TN176I	384	3.3	7.5	Lead-free TQFP	176	128	I
	LC4384V-10TN176I	384	3.3	10	Lead-free TQFP	176	128	I
LC4512V	LC4512V-5FTN256I	512	3.3	5	Lead-free ftBGA	256	208	I
	LC4512V-75FTN256I	512	3.3	7.5	Lead-free ftBGA	256	208	I
	LC4512V-10FTN256I	512	3.3	10	Lead-free ftBGA	256	208	I
	LC4512V-5FN256I ¹	512	3.3	5	Lead-free fpBGA	256	208	I
	LC4512V-75FN256I ¹	512	3.3	7.5	Lead-free fpBGA	256	208	I
	LC4512V-10FN256I ¹	512	3.3	10	Lead-free fpBGA	256	208	I
	LC4512V-5TN176I	512	3.3	5	Lead-free TQFP	176	128	I
	LC4512V-75TN176I	512	3.3	7.5	Lead-free TQFP	176	128	I
	LC4512V-10TN176I	512	3.3	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.