# Lattice Semiconductor Corporation - LC4256B-10TN176I Datasheet

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 2.3V ~ 2.7V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 128 |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-TQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-10tn176i |

*Table 2. ispMACH 4000Z Family Selection Guide*

| | ispMACH 4032ZC | ispMACH 4064ZC | ispMACH 4128ZC | ispMACH 4256ZC |
|---|---|---|---|---|
| Macrocells | 32 | 64 | 128 | 256 |
| I/O + Dedicated Inputs | 32+4/32+4 | 32+4/32+12/ 64+10/64+10 | 64+10/96+4 | 64+10/96+6/ 128+4 |
| $t_{PD}$ (ns) | 3.5 | 3.7 | 4.2 | 4.5 |
| $t_S$ (ns) | 2.2 | 2.5 | 2.7 | 2.9 |
| $t_{CO}$ (ns) | 3.0 | 3.2 | 3.5 | 3.8 |
| $f_{MAX}$ (MHz) | 267 | 250 | 220 | 200 |
| Supply Voltage (V) | 1.8 | 1.8 | 1.8 | 1.8 |
| Max. Standby Icc (µA) | 20 | 25 | 35 | 55 |
| Pins/Package | 48 TQFP<br>56 csBGA | 48 TQFP<br>56 csBGA<br>100 TQFP<br>132 csBGA | 100 TQFP<br>132csBGA | 100 TQFP<br>132 csBGA<br>176 TQFP |

## ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

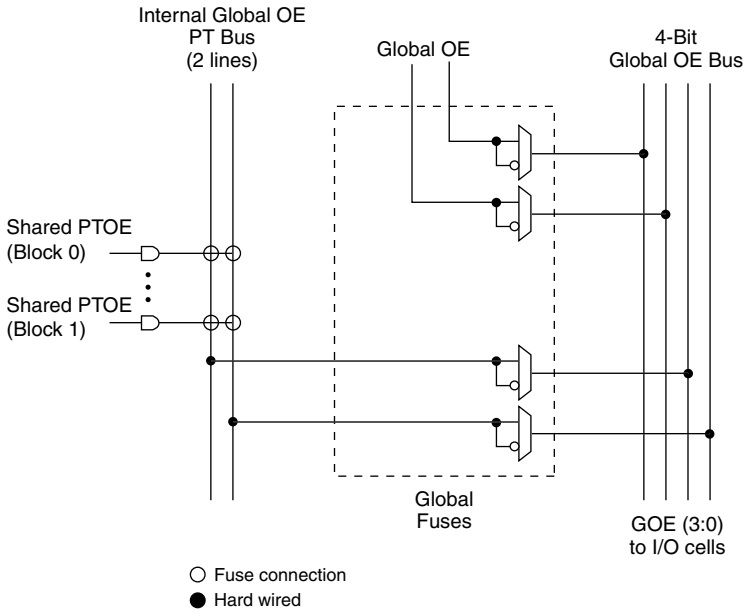
The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to $V_{CC}$ (logic core).

## Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

***Figure 10. Global OE Generation for ispMACH 4032***




## Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced $E^2$ low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

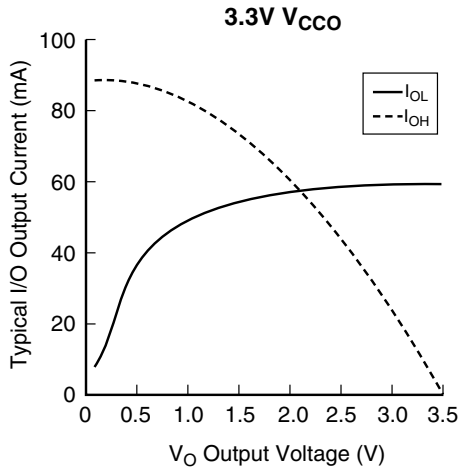
The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

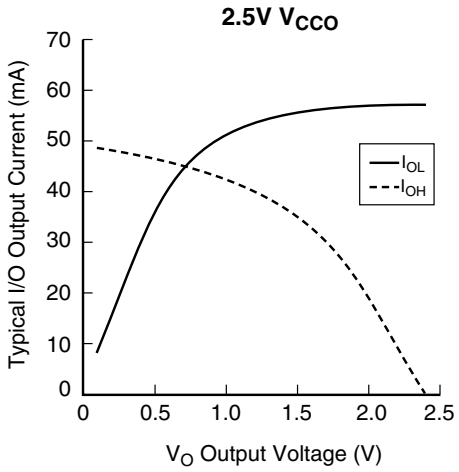
## IEEE 1149.1-Compliant Boundary Scan Testability

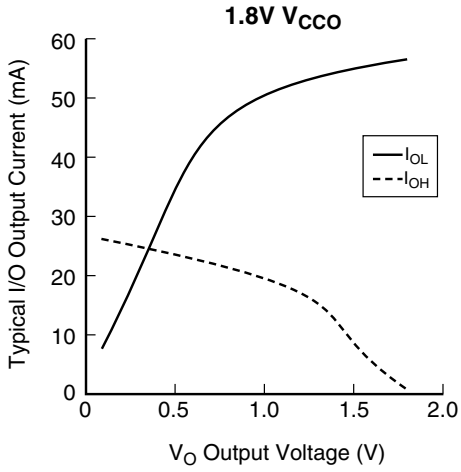
All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

## I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.


3.3V $V_{CCO}$
Typical I/O Output Current (mA)
100
80
60
40
20
0
0 0.5 1.0 1.5 2.0 2.5 3.0 3.5
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$


2.5V $V_{CCO}$
Typical I/O Output Current (mA)
70
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0 2.5
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$


1.8V $V_{CCO}$
Typical I/O Output Current (mA)
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$

# ispMACH 4000V/B/C External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -25 | | -27 | | -3 | | -35 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 2.5 | — | 2.7 | — | 3.0 | — | 3.5 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 3.2 | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| $t_S$ | GLB register setup time before clock | 1.8 | — | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 2.0 | — | 2.0 | — | 2.2 | — | 2.2 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 0.7 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 1.7 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 0.9 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 2.2 | — | 2.7 | — | 2.7 | — | 2.7 | ns |
| $t_R$ | External reset pin to output delay | — | 3.5 | — | 4.0 | — | 4.4 | — | 4.5 | ns |
| $t_{RW}$ | External reset pulse duration | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | - | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 4.0 | — | 4.5 | — | 5.0 | — | 5.5 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 5.0 | — | 6.5 | — | 8.0 | — | 8.0 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 3.0 | — | 3.5 | — | 4.0 | — | 4.5 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.1 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.1 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.1 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 400 | — | 333 | — | 322 | — | 322 | MHz |
| $f_{MAX}$ (Ext.) | Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$ | — | 250 | — | 222 | — | 212 | — | 212 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

# ispMACH 4000V/B/C External Switching Characteristics (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -5 | | -75 | | -10 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 5.0 | — | 7.5 | — | 10.0 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 5.5 | — | 8.0 | — | 10.5 | ns |
| $t_S$ | GLB register setup time before clock | 3.0 | — | 4.5 | — | 5.5 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 3.2 | — | 4.7 | — | 5.5 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.2 | — | 1.7 | — | 1.7 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.2 | — | 2.7 | — | 2.7 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.0 | — | 1.0 | — | 1.0 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.4 | — | 4.5 | — | 6.0 | ns |
| $t_R$ | External reset pin to output delay | — | 6.3 | — | 9.0 | — | 10.5 | ns |
| $t_{RW}$ | External reset pulse duration | 2.0 | — | 4.0 | — | 4.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 7.0 | — | 9.0 | — | 10.5 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 9.0 | — | 10.3 | — | 12.0 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 5.0 | — | 7.0 | — | 8.0 | ns |
| $t_{CW}$ | Global clock width, high or low | 2.2 | — | 2.8 | — | 4.0 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 2.2 | — | 2.8 | — | 4.0 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 2.2 | — | 2.8 | — | 4.0 | | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 227 | — | 168 | — | 125 | MHz |
| $f_{MAX}$ (Ext.) | Clock frequency with external feedback, [1/ ($t_S$ + $t_{CO}$)] | — | 156 | — | 111 | — | 86 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

# ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -75 | | -10 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{GPTOE}$ | Global PT OE Delay | — | 5.58 | — | 5.58 | — | 5.78 | ns |
| $t_{PTOE}$ | Macrocell PT OE Delay | — | 3.58 | — | 4.28 | — | 4.28 | ns |

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

# ispMACH 4000Z Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{GPTOE}$ | Global PT OE Delay | — | 1.9 | — | 2.35 | — | 2.60 | ns |
| $t_{PTOE}$ | Macrocell PT OE Delay | — | 2.4 | — | 3.35 | — | 2.60 | ns |

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

# ispMACH 4000Z Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -45 | | -5 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 0.95 | — | 1.25 | — | 1.80 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 3.00 | — | 3.50 | — | 4.30 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 1.95 | — | 2.05 | — | 2.15 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 1.10 | — | 1.00 | — | 1.30 | ns |
| $t_{EN}$ | Output Enable Time | — | 2.50 | — | 2.50 | — | 2.70 | ns |
| $t_{DIS}$ | Output Disable Time | — | 2.50 | — | 2.50 | — | 2.70 | ns |
| **Routing/GLB Delays** | | | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 2.25 | — | 2.05 | — | 2.50 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 0.65 | — | 0.65 | — | 1.00 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 1.00 | — | 1.00 | — | 1.00 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.35 | — | 0.05 | — | 0.05 | ns |
| $t_{PDb}$ | 5-PT Bypass Propagation Delay | — | 0.20 | — | 0.70 | — | 1.90 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.45 | — | 0.65 | — | 1.00 | ns |
| **Register/Latch Delays** | | | | | | | | |
| $t_{S}$ | D-Register Setup Time (Global Clock) | 1.00 | — | 1.10 | — | 1.35 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 2.10 | — | 1.90 | — | 2.45 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.20 | — | 1.30 | — | 1.55 | — | ns |
| $t_{ST\_PT}$ | T-register Setup Time (Product Term Clock) | 2.30 | — | 2.10 | — | 2.75 | — | ns |
| $t_{H}$ | D-Register Hold Time | 1.90 | — | 1.90 | — | 3.15 | — | ns |
| $t_{HT}$ | T-Resister Hold Time | 1.90 | — | 1.90 | — | 3.15 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 1.30 | — | 1.10 | — | 0.75 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 1.30 | — | 1.50 | — | 1.95 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 1.00 | — | 1.00 | — | 1.18 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.75 | — | 1.15 | — | 1.05 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 1.00 | — | 1.00 | — | 1.65 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 2.10 | — | 1.90 | — | 2.15 | — | ns |
| $t_{HL}$ | Latch Hold Time | 2.00 | — | 2.00 | — | 1.17 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.33 | — | 0.33 | — | 0.33 | ns |
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.97 | — | 0.97 | — | 0.28 | ns |
| $t_{SRR}$ | Asynchronous Reset or Set Recovery Delay | — | 1.80 | — | 1.80 | — | 1.67 | ns |
| **Control Delays** | | | | | | | | |
| $t_{BCLK}$ | GLB PT Clock Delay | — | 1.55 | — | 1.55 | — | 1.25 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | — | 1.55 | — | 1.55 | — | 1.25 | ns |
| $t_{BSR}$ | GLB PT Set/Reset Delay | — | 1.83 | — | 1.83 | — | 1.83 | ns |
| $t_{PTSR}$ | Macrocell PT Set/Reset Delay | — | 1.83 | — | 1.83 | — | 2.72 | ns |
| $t_{GPTOE}$ | Global PT OE Delay | — | 4.30 | — | 4.20 | — | 3.50 | ns |

# ispMACH 4000Z Timing Adders [1]

| Adder Type | Base Parameter | Description | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 1.00 | — | 1.00 | — | 1.30 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.40 | — | 0.40 | — | 0.45 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.40 | — | 0.40 | — | 0.40 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.04 | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding the use of these adders.

## Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

***Figure 12. Output Test Load, LVTTL and LVCMOS Standards***

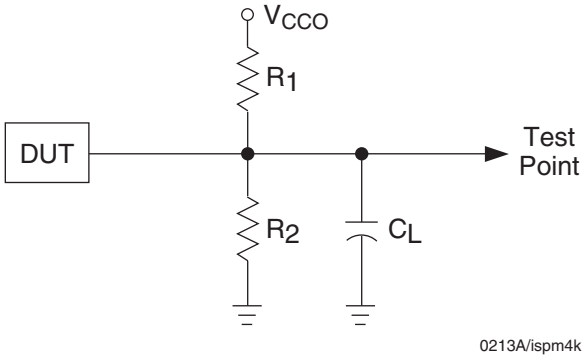



***Table 11. Test Fixture Required Components***

| Test Condition | $R_1$ | $R_2$ | $C_L$[1] | Timing Ref. | $V_{CCO}$ |
|---|---|---|---|---|---|
| LVCMOS I/O, (L -> H, H -> L) | 106Ω | 106Ω | 35pF | LVCMOS 3.3 = 1.5V | LVCMOS 3.3 = 3.0V |
| | | | | LVCMOS 2.5 = $V_{CCO}$/2 | LVCMOS 2.5 = 2.3V |
| | | | | LVCMOS 1.8 = $V_{CCO}$/2 | LVCMOS 1.8 = 1.65V |
| LVCMOS I/O (Z -> H) | ∞ | 106Ω | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (Z -> L) | 106Ω | ∞ | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (H -> Z) | ∞ | 106Ω | 5pF | $V_{OH}$ - 0.3 | 3.0V |
| LVCMOS I/O (L -> Z) | 106Ω | ∞ | 5pF | $V_{OL}$ + 0.3 | 3.0V |

1. $C_L$ includes test fixtures and probe capacitance.

## ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V | | ispMACH 4256V | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 43 | 0 | D9 | D^7 | G4 | G^2 |
| 44 | 0 | D8 | D^6 | G2 | G^1 |
| 45 | 0 | NC[2] | - | I[2] | - |
| 46 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 47 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 48 | 0 | D6 | D^5 | H12 | H^6 |
| 49 | 0 | D5 | D^4 | H10 | H^5 |
| 50 | 0 | D4 | D^3 | H8 | H^4 |
| 51 | 0 | D2 | D^2 | H6 | H^3 |
| 52 | 0 | D1 | D^1 | H4 | H^2 |
| 53 | 0 | D0 | D^0 | H2 | H^1 |
| 54 | 0 | CLK1/I | - | CLK1/I | - |
| 55 | 1 | GND (Bank 1) | - | GND (Bank 1) | - |
| 56 | 1 | CLK2/I | - | CLK2/I | - |
| 57 | - | VCC | - | VCC | - |
| 58 | 1 | E0 | E^0 | I2 | I^1 |
| 59 | 1 | E1 | E^1 | I4 | I^2 |
| 60 | 1 | E2 | E^2 | I6 | I^3 |
| 61 | 1 | E4 | E^3 | I8 | I^4 |
| 62 | 1 | E5 | E^4 | I10 | I^5 |
| 63 | 1 | E6 | E^5 | I12 | I^6 |
| 64 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 65 | 1 | GND (Bank 1) | - | GND (Bank 1) | - |
| 66 | 1 | E8 | E^6 | J2 | J^1 |
| 67 | 1 | E9 | E^7 | J4 | J^2 |
| 68 | 1 | E10 | E^8 | J6 | J^3 |
| 69 | 1 | E12 | E^9 | J8 | J^4 |
| 70 | 1 | E13 | E^10 | J10 | J^5 |
| 71 | 1 | E14 | E^11 | J12 | J^6 |
| 72 | 1 | NC[2] | - | I[2] | - |
| 73 | - | GND | - | GND | - |
| 74 | - | TMS | - | TMS | - |
| 75 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 76 | 1 | F0 | F^0 | K12 | K^6 |
| 77 | 1 | F1 | F^1 | K10 | K^5 |
| 78 | 1 | F2 | F^2 | K8 | K^4 |
| 79 | 1 | F4 | F^3 | K6 | K^3 |
| 80 | 1 | F5 | F^4 | K4 | K^2 |
| 81 | 1 | F6 | F^5 | K2 | K^1 |
| 82 | 1 | GND (Bank 1) | - | GND (Bank 1) | - |
| 83 | 1 | F8 | F^6 | L14 | L^7 |
| 84 | 1 | F9 | F^7 | L12 | L^6 |
| 85 | 1 | F10 | F^8 | L10 | L^5 |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| J6 | 0 | E14 | E^7 | E10 | E^7 | H14 | H^7 | J14 | J^7 |
| K3 | 0 | NC | - | E12 | E^8 | G0 | G^0 | I0 | I^0 |
| K4 | 0 | NC | - | E14 | E^9 | G2 | G^1 | I4 | I^1 |
| L1 | 0 | NC | - | NC | - | I14 | I^7 | K0 | K^0 |
| L2 | 0 | NC | - | NC | - | I12 | I^6 | K2 | K^1 |
| M1 | 0 | NC | - | NC | - | NC | - | K4 | K^2 |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| - | 0 | - | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| M2 | 0 | NC | - | NC | - | NC | - | K6 | K^3 |
| N1 | 0 | NC | - | NC | - | I10 | I^5 | K8 | K^4 |
| M3 | 0 | NC | - | NC | - | I8 | I^4 | K10 | K^5 |
| M4 | 0 | NC | - | F0 | F^0 | G4 | G^2 | I8 | I^2 |
| N2 | 0 | NC | - | F1 | F^1 | G6 | G^3 | I12 | I^3 |
| K5 | 0 | F0 | F^0 | F2 | F^2 | J0 | J^0 | N0 | N^0 |
| P1 | 0 | F2 | F^1 | F4 | F^3 | J2 | J^1 | N2 | N^1 |
| K6 | 0 | F4 | F^2 | F6 | F^4 | J4 | J^2 | N4 | N^2 |
| N3 | 0 | F6 | F^3 | F8 | F^5 | J6 | J^3 | N6 | N^3 |
| L5 | 0 | F8 | F^4 | F9 | F^6 | J8 | J^4 | N8 | N^4 |
| P2 | 0 | F10 | F^5 | F10 | F^7 | J10 | J^5 | N10 | N^5 |
| L6 | 0 | F12 | F^6 | F12 | F^8 | J12 | J^6 | N12 | N^6 |
| R1 | 0 | F14 | F^7 | F14 | F^9 | J14 | J^7 | N14 | N^7 |
| - | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| P3 | - | TCK | - | TCK | - | TCK | - | TCK | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| - | - | GND | - | GND | - | GND | - | GND | - |
| - | 0 | - | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| T2 | 0 | NC | - | G14 | G^9 | I6 | I^3 | K12 | K^6 |
| M5 | 0 | NC | - | G12 | G^8 | I4 | I^2 | K14 | K^7 |
| N4 | 0 | G14 | G^7 | G10 | G^7 | K14 | K^7 | O14 | O^7 |
| T3 | 0 | G12 | G^6 | G9 | G^6 | K12 | K^6 | O12 | O^6 |
| R3 | 0 | G10 | G^5 | G8 | G^5 | K10 | K^5 | O10 | O^5 |
| M6 | 0 | G8 | G^4 | G6 | G^4 | K8 | K^4 | O8 | O^4 |
| P4 | 0 | G6 | G^3 | G4 | G^3 | K6 | K^3 | O6 | O^3 |
| L7 | 0 | G4 | G^2 | G2 | G^2 | K4 | K^2 | O4 | O^2 |
| N5 | 0 | G2 | G^1 | G1 | G^1 | K2 | K^1 | O2 | O^1 |
| M7 | 0 | G0 | G^0 | G0 | G^0 | K0 | K^0 | O0 | O^0 |
| P5 | 0 | NC | - | NC | - | G8 | G^4 | M0 | M^0 |
| R4 | 0 | NC | - | NC | - | G10 | G^5 | M4 | M^1 |
| T4 | 0 | NC | - | NC | - | NC | - | L0 | L^0 |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| - | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| R5 | 0 | NC | - | NC | - | NC | - | L4 | L^1 |
| T5 | 0 | NC | - | NC | - | I2 | I^1 | L8 | L^2 |
| R6 | 0 | NC | - | NC | - | I0 | I^0 | L12 | L^3 |
| T6 | 0 | NC | - | H14 | H^9 | G12 | G^6 | M8 | M^2 |
| N7 | 0 | NC | - | H12 | H^8 | G14 | G^7 | M12 | M^3 |
| P7 | 0 | H14 | H^7 | H10 | H^7 | L14 | L^7 | P14 | P^7 |
| R7 | 0 | H12 | H^6 | H9 | H^6 | L12 | L^6 | P12 | P^6 |
| L8 | 0 | H10 | H^5 | H8 | H^5 | L10 | L^5 | P10 | P^5 |
| T7 | 0 | H8 | H^4 | H6 | H^4 | L8 | L^4 | P8 | P^4 |
| M8 | 0 | H6 | H^3 | H4 | H^3 | L6 | L^3 | P6 | P^3 |
| N8 | 0 | H4 | H^2 | H2 | H^2 | L4 | L^2 | P4 | P^2 |
| R8 | 0 | H2 | H^1 | H1 | H^1 | L2 | L^1 | P2 | P^1 |
| P8 | 0 | H0 | H^0 | H0 | H^0 | L0 | L^0 | P0 | P^0 |
| - | - | GND | - | GND | - | GND | - | GND | - |
| T8 | 0 | CLK1/I | - | CLK1/I | - | CLK1/I | - | CLK1/I | - |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| N9 | 1 | CLK2/I | - | CLK2/I | - | CLK2/I | - | CLK2/I | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| P9 | 1 | I0 | I^0 | I0 | I^0 | M0 | M^0 | AX0 | AX^0 |
| R9 | 1 | I2 | I^1 | I1 | I^1 | M2 | M^1 | AX2 | AX^1 |
| T9 | 1 | I4 | I^2 | I2 | I^2 | M4 | M^2 | AX4 | AX^2 |
| T10 | 1 | I6 | I^3 | I4 | I^3 | M6 | M^3 | AX6 | AX^3 |
| R10 | 1 | I8 | I^4 | I6 | I^4 | M8 | M^4 | AX8 | AX^4 |
| M9 | 1 | I10 | I^5 | I8 | I^5 | M10 | M^5 | AX10 | AX^5 |
| P10 | 1 | I12 | I^6 | I9 | I^6 | M12 | M^6 | AX12 | AX^6 |
| L9 | 1 | I14 | I^7 | I10 | I^7 | M14 | M^7 | AX14 | AX^7 |
| N10 | 1 | NC | - | I12 | I^8 | BX14 | BX^7 | DX0 | DX^0 |
| T11 | 1 | NC | - | I14 | I^9 | BX12 | BX^6 | DX4 | DX^1 |
| R11 | 1 | NC | - | NC | - | P0 | P^0 | EX0 | EX^0 |
| T12 | 1 | NC | - | NC | - | P2 | P^1 | EX4 | EX^1 |
| N12 | 1 | NC | - | NC | - | NC | - | EX8 | EX^2 |
| - | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| R12 | 1 | NC | - | NC | - | NC | - | EX12 | EX^3 |
| T13 | 1 | NC | - | J0 | J^0 | BX10 | BX^5 | DX8 | DX^2 |
| P12 | 1 | NC | - | J1 | J^1 | BX8 | BX^4 | DX12 | DX^3 |
| M10 | 1 | J0 | J^0 | J2 | J^2 | N0 | N^0 | BX0 | BX^0 |
| R13 | 1 | J2 | J^1 | J4 | J^3 | N2 | N^1 | BX2 | BX^1 |
| L10 | 1 | J4 | J^2 | J6 | J^4 | N4 | N^2 | BX4 | BX^2 |
| T14 | 1 | J6 | J^3 | J8 | J^5 | N6 | N^3 | BX6 | BX^3 |
| M11 | 1 | J8 | J^4 | J9 | J^6 | N8 | N^4 | BX8 | BX^4 |

**ispMACH 4000C (1.8V) Industrial Devices (Cont.)**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4384C | LC4384C-5FT256I | 384 | 1.8 | 5 | ftBGA | 256 | 192 | I |
| | LC4384C-75FT256I | 384 | 1.8 | 7.5 | ftBGA | 256 | 192 | I |
| | LC4384C-10FT256I | 384 | 1.8 | 10 | ftBGA | 256 | 192 | I |
| | LC4384C-5F256I[1] | 384 | 1.8 | 5 | fpBGA | 256 | 192 | I |
| | LC4384C-75F256I[1] | 384 | 1.8 | 7.5 | fpBGA | 256 | 192 | I |
| | LC4384C-10F256I[1] | 384 | 1.8 | 10 | fpBGA | 256 | 192 | I |
| | LC4384C-5T176I | 384 | 1.8 | 5 | TQFP | 176 | 128 | I |
| | LC4384C-75T176I | 384 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4384C-10T176I | 384 | 1.8 | 10 | TQFP | 176 | 128 | I |
| LC4512C | LC4512C-5FT256I | 512 | 1.8 | 5 | ftBGA | 256 | 208 | I |
| | LC4512C-75FT256I | 512 | 1.8 | 7.5 | ftBGA | 256 | 208 | I |
| | LC4512C-10FT256I | 512 | 1.8 | 10 | ftBGA | 256 | 208 | I |
| | LC4512C-5F256I[1] | 512 | 1.8 | 5 | fpBGA | 256 | 208 | I |
| | LC4512C-75F256I[1] | 512 | 1.8 | 7.5 | fpBGA | 256 | 208 | I |
| | LC4512C-10F256I[1] | 512 | 1.8 | 10 | fpBGA | 256 | 208 | I |
| | LC4512C-5T176I | 512 | 1.8 | 5 | TQFP | 176 | 128 | I |
| | LC4512C-75T176I | 512 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4512C-10T176I | 512 | 1.8 | 10 | TQFP | 176 | 128 | I |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000B (2.5V) Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032B | LC4032B-25T48C | 32 | 2.5 | 2.5 | TQFP | 48 | 32 | C |
| | LC4032B-5T48C | 32 | 2.5 | 5 | TQFP | 48 | 32 | C |
| | LC4032B-75T48C | 32 | 2.5 | 7.5 | TQFP | 48 | 32 | C |
| | LC4032B-25T44C | 32 | 2.5 | 2.5 | TQFP | 44 | 30 | C |
| | LC4032B-5T44C | 32 | 2.5 | 5 | TQFP | 44 | 30 | C |
| | LC4032B-75T44C | 32 | 2.5 | 7.5 | TQFP | 44 | 30 | C |
| LC4064B | LC4064B-25T100C | 64 | 2.5 | 2.5 | TQFP | 100 | 64 | C |
| | LC4064B-5T100C | 64 | 2.5 | 5 | TQFP | 100 | 64 | C |
| | LC4064B-75T100C | 64 | 2.5 | 7.5 | TQFP | 100 | 64 | C |
| | LC4064B-25T48C | 64 | 2.5 | 2.5 | TQFP | 48 | 32 | C |
| | LC4064B-5T48C | 64 | 2.5 | 5 | TQFP | 48 | 32 | C |
| | LC4064B-75T48C | 64 | 2.5 | 7.5 | TQFP | 48 | 32 | C |
| | LC4064B-25T44C | 64 | 2.5 | 2.5 | TQFP | 44 | 30 | C |
| | LC4064B-5T44C | 64 | 2.5 | 5 | TQFP | 44 | 30 | C |
| | LC4064B-75T44C | 64 | 2.5 | 7.5 | TQFP | 44 | 30 | C |
| LC4128B | LC4128B-27T128C | 128 | 2.5 | 2.7 | TQFP | 128 | 92 | C |
| | LC4128B-5T128C | 128 | 2.5 | 5 | TQFP | 128 | 92 | C |
| | LC4128B-75T128C | 128 | 2.5 | 7.5 | TQFP | 128 | 92 | C |
| | LC4128B-27T100C | 128 | 2.5 | 2.7 | TQFP | 100 | 64 | C |
| | LC4128B-5T100C | 128 | 2.5 | 5 | TQFP | 100 | 64 | C |
| | LC4128B-75T100C | 128 | 2.5 | 7.5 | TQFP | 100 | 64 | C |

**ispMACH 4000B (2.5V) Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4256B | LC4256B-3FT256AC | 256 | 2.5 | 3 | ftBGA | 256 | 128 | C |
| | LC4256B-5FT256AC | 256 | 2.5 | 5 | ftBGA | 256 | 128 | C |
| | LC4256B-75FT256AC | 256 | 2.5 | 7.5 | ftBGA | 256 | 128 | C |
| | LC4256B-3FT256BC | 256 | 2.5 | 3 | ftBGA | 256 | 160 | C |
| | LC4256B-5FT256BC | 256 | 2.5 | 5 | ftBGA | 256 | 160 | C |
| | LC4256B-75FT256BC | 256 | 2.5 | 7.5 | ftBGA | 256 | 160 | C |
| | LC4256B-3F256AC[1] | 256 | 2.5 | 3 | fpBGA | 256 | 128 | C |
| | LC4256B-5F256AC[1] | 256 | 2.5 | 5 | fpBGA | 256 | 128 | C |
| | LC4256B-75F256AC[1] | 256 | 2.5 | 7.5 | fpBGA | 256 | 128 | C |
| | LC4256B-3F256BC[1] | 256 | 2.5 | 3 | fpBGA | 256 | 160 | C |
| | LC4256B-5F256BC[1] | 256 | 2.5 | 5 | fpBGA | 256 | 160 | C |
| | LC4256B-75F256BC[1] | 256 | 2.5 | 7.5 | fpBGA | 256 | 160 | C |
| | LC4256B-3T176C | 256 | 2.5 | 3 | TQFP | 176 | 128 | C |
| | LC4256B-5T176C | 256 | 2.5 | 5 | TQFP | 176 | 128 | C |
| | LC4256B-75T176C | 256 | 2.5 | 7.5 | TQFP | 176 | 128 | C |
| | LC4256B-3T100C | 256 | 2.5 | 3 | TQFP | 100 | 64 | C |
| | LC4256B-5T100C | 256 | 2.5 | 5 | TQFP | 100 | 64 | C |
| | LC4256B-75T100C | 256 | 2.5 | 7.5 | TQFP | 100 | 64 | C |
| LC4384B | LC4384B-35FT256C | 384 | 2.5 | 3.5 | ftBGA | 256 | 192 | C |
| | LC4384B-5FT256C | 384 | 2.5 | 5 | ftBGA | 256 | 192 | C |
| | LC4384B-75FT256C | 384 | 2.5 | 7.5 | ftBGA | 256 | 192 | C |
| | LC4384B-35F256C[1] | 384 | 2.5 | 3.5 | fpBGA | 256 | 192 | C |
| | LC4384B-5F256C[1] | 384 | 2.5 | 5 | fpBGA | 256 | 192 | C |
| | LC4384B-75F256C[1] | 384 | 2.5 | 7.5 | fpBGA | 256 | 192 | C |
| | LC4384B-35T176C | 384 | 2.5 | 3.5 | TQFP | 176 | 128 | C |
| | LC4384B-5T176C | 384 | 2.5 | 5 | TQFP | 176 | 128 | C |
| | LC4384B-75T176C | 384 | 2.5 | 7.5 | TQFP | 176 | 128 | C |
| LC4512B | LC4512B-35FT256C | 512 | 2.5 | 3.5 | ftBGA | 256 | 208 | C |
| | LC4512B-5FT256C | 512 | 2.5 | 5 | ftBGA | 256 | 208 | C |
| | LC4512B-75FT256C | 512 | 2.5 | 7.5 | ftBGA | 256 | 208 | C |
| | LC4512B-35F256C[1] | 512 | 2.5 | 3.5 | fpBGA | 256 | 208 | C |
| | LC4512B-5F256C[1] | 512 | 2.5 | 5 | fpBGA | 256 | 208 | C |
| | LC4512B-75F256C[1] | 512 | 2.5 | 7.5 | fpBGA | 256 | 208 | C |
| | LC4512B-35T176C | 512 | 2.5 | 3.5 | TQFP | 176 | 128 | C |
| | LC4512B-5T176C | 512 | 2.5 | 5 | TQFP | 176 | 128 | C |
| | LC4512B-75T176C | 512 | 2.5 | 7.5 | TQFP | 176 | 128 | C |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000V (3.3V) Extended Temperature Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032V | LC4032V-75T48E | 32 | 3.3 | 7.5 | TQFP | 48 | 32 | E |
| | LC4032V-75T44E | 32 | 3.3 | 7.5 | TQFP | 44 | 30 | E |
| LC4064V | LC4064V-75T100E | 64 | 3.3 | 7.5 | TQFP | 100 | 64 | E |
| | LC4064V-75T48E | 64 | 3.3 | 7.5 | TQFP | 48 | 32 | E |
| | LC4064V-75T44E | 64 | 3.3 | 7.5 | TQFP | 44 | 30 | E |
| LC4128V | LC4128V-75T144E | 128 | 3.3 | 7.5 | TQFP | 144 | 96 | E |
| | LC4128V-75T128E | 128 | 3.3 | 7.5 | TQFP | 128 | 92 | E |
| | LC4128V-75T100E | 128 | 3.3 | 7.5 | TQFP | 100 | 64 | E |
| LC4256V | LC4256V-75T176E | 256 | 3.3 | 7.5 | TQFP | 176 | 128 | E |
| | LC4256V-75T144E | 256 | 3.3 | 7.5 | TQFP | 144 | 96 | E |
| | LC4256V-75T100E | 256 | 3.3 | 7.5 | TQFP | 100 | 64 | E |

**ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4256C | LC4256C-5FTN256AI | 256 | 1.8 | 5 | Lead-free ftBGA | 256 | 128 | I |
| | LC4256C-75FTN256AI | 256 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 128 | I |
| | LC4256C-10FTN256AI | 256 | 1.8 | 10 | Lead-free ftBGA | 256 | 128 | I |
| | LC4256C-5FTN256BI | 256 | 1.8 | 5 | Lead-free ftBGA | 256 | 160 | I |
| | LC4256C-75FTN256BI | 256 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 160 | I |
| | LC4256C-10FTN256BI | 256 | 1.8 | 10 | Lead-free ftBGA | 256 | 160 | I |
| | LC4256C-5FN256AI[1] | 256 | 1.8 | 5 | Lead-free fpBGA | 256 | 128 | I |
| | LC4256C-75FN256AI[1] | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 128 | I |
| | LC4256C-10FN256AI[1] | 256 | 1.8 | 10 | Lead-free fpBGA | 256 | 128 | I |
| | LC4256C-5FN256BI[1] | 256 | 1.8 | 5 | Lead-free fpBGA | 256 | 160 | I |
| | LC4256C-75FN256BI[1] | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 160 | I |
| | LC4256C-10FN256BI[1] | 256 | 1.8 | 10 | Lead-free fpBGA | 256 | 160 | I |
| | LC4256C-5TN176I | 256 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | I |
| | LC4256C-75TN176I | 256 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | I |
| | LC4256C-10TN176I | 256 | 1.8 | 10 | Lead-free TQFP | 176 | 128 | I |
| | LC4256C-5TN100I | 256 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | I |
| | LC4256C-75TN100I | 256 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | I |
| | LC4256C-10TN100I | 256 | 1.8 | 10 | Lead-free TQFP | 100 | 64 | I |
| LC4384C | LC4384C-5FTN256I | 384 | 1.8 | 5 | Lead-free ftBGA | 256 | 192 | I |
| | LC4384C-75FTN256I | 384 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 192 | I |
| | LC4384C-10FTN256I | 384 | 1.8 | 10 | Lead-free ftBGA | 256 | 192 | I |
| | LC4384C-5FN256I[1] | 384 | 1.8 | 5 | Lead-free fpBGA | 256 | 192 | I |
| | LC4384C-75FN256I[1] | 384 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 192 | I |
| | LC4384C-10FN256I[1] | 384 | 1.8 | 10 | Lead-free fpBGA | 256 | 192 | I |
| | LC4384C-5TN176I | 384 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | I |
| | LC4384C-75TN176I | 384 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | I |
| | LC4384C-10TN176I | 384 | 1.8 | 10 | Lead-free TQFP | 176 | 128 | I |
| LC4512C | LC4512C-5FTN256I | 512 | 1.8 | 5 | Lead-free ftBGA | 256 | 208 | I |
| | LC4512C-75FTN256I | 512 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 208 | I |
| | LC4512C-10FTN256I | 512 | 1.8 | 10 | Lead-free ftBGA | 256 | 208 | I |
| | LC4512C-5FN256I[1] | 512 | 1.8 | 5 | Lead-free fpBGA | 256 | 208 | I |
| | LC4512C-75FN256I[1] | 512 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 208 | I |
| | LC4512C-10FN256I[1] | 512 | 1.8 | 10 | Lead-free fpBGA | 256 | 208 | I |
| | LC4512C-5TN176I | 512 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | I |
| | LC4512C-75TN176I | 512 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | I |
| | LC4512C-10TN176I | 512 | 1.8 | 10 | Lead-free TQFP | 176 | 128 | I |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000V (3.3V) Lead-Free Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032V | LC4032V-25TN48C | 32 | 3.3 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032V-5TN48C | 32 | 3.3 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032V-75TN48C | 32 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032V-25TN44C | 32 | 3.3 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4032V-5TN44C | 32 | 3.3 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4032V-75TN44C | 32 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | C |
| LC4064V | LC4064V-25TN100C | 64 | 3.3 | 2.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064V-5TN100C | 64 | 3.3 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064V-75TN100C | 64 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064V-25TN48C | 64 | 3.3 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064V-5TN48C | 64 | 3.3 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064V-75TN48C | 64 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064V-25TN44C | 64 | 3.3 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064V-5TN44C | 64 | 3.3 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064V-75TN44C | 64 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | C |
| LC4128V | LC4128V-27TN144C | 128 | 3.3 | 2.7 | Lead-free TQFP | 144 | 96 | C |
| | LC4128V-5TN144C | 128 | 3.3 | 5 | Lead-free TQFP | 144 | 96 | C |
| | LC4128V-75TN144C | 128 | 3.3 | 7.5 | Lead-free TQFP | 144 | 96 | C |
| | LC4128V-27TN128C | 128 | 3.3 | 2.7 | Lead-free TQFP | 128 | 92 | C |
| | LC4128V-5TN128C | 128 | 3.3 | 5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128V-75TN128C | 128 | 3.3 | 7.5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128V-27TN100C | 128 | 3.3 | 2.7 | Lead-free TQFP | 100 | 64 | C |
| | LC4128V-5TN100C | 128 | 3.3 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4128V-75TN100C | 128 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | C |

**ispMACH 4000V (3.3V) Lead-Free Industrial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032V | LC4032V-5TN48I | 32 | 3.3 | 5 | Lead-free TQFP | 48 | 32 | I |
| | LC4032V-75TN48I | 32 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | I |
| | LC4032V-10TN48I | 32 | 3.3 | 10 | Lead-free TQFP | 48 | 32 | I |
| | LC4032V-5TN44I | 32 | 3.3 | 5 | Lead-free TQFP | 44 | 30 | I |
| | LC4032V-75TN44I | 32 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | I |
| | LC4032V-10TN44I | 32 | 3.3 | 10 | Lead-free TQFP | 44 | 30 | I |
| LC4064V | LC4064V-5TN100I | 64 | 3.3 | 5 | Lead-free TQFP | 100 | 64 | I |
| | LC4064V-75TN100I | 64 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | I |
| | LC4064V-10TN100I | 64 | 3.3 | 10 | Lead-free TQFP | 100 | 64 | I |
| | LC4064V-5TN48I | 64 | 3.3 | 5 | Lead-free TQFP | 48 | 32 | I |
| | LC4064V-75TN48I | 64 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | I |
| | LC4064V-10TN48I | 64 | 3.3 | 10 | Lead-free TQFP | 48 | 32 | I |
| | LC4064V-5TN44I | 64 | 3.3 | 5 | Lead-free TQFP | 44 | 30 | I |
| | LC4064V-75TN44I | 64 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | I |
| | LC4064V-10TN44I | 64 | 3.3 | 10 | Lead-free TQFP | 44 | 30 | I |
| LC4128V | LC4128V-5TN144I | 128 | 3.3 | 5 | Lead-free TQFP | 144 | 96 | I |
| | LC4128V-75TN144I | 128 | 3.3 | 7.5 | Lead-free TQFP | 144 | 96 | I |
| | LC4128V-10TN144I | 128 | 3.3 | 10 | Lead-free TQFP | 144 | 96 | I |
| | LC4128V-5TN128I | 128 | 3.3 | 5 | Lead-free TQFP | 128 | 92 | I |
| | LC4128V-75TN128I | 128 | 3.3 | 7.5 | Lead-free TQFP | 128 | 92 | I |
| | LC4128V-10TN128I | 128 | 3.3 | 10 | Lead-free TQFP | 128 | 92 | I |
| | LC4128V-5TN100I | 128 | 3.3 | 5 | Lead-free TQFP | 100 | 64 | I |
| | LC4128V-75TN100I | 128 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | I |
| | LC4128V-10TN100I | 128 | 3.3 | 10 | Lead-free TQFP | 100 | 64 | I |

**ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032V | LC4032V-75TN48E | 32 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | E |
| | LC4032V-75TN44E | 32 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | E |
| LC4064V | LC4064V-75TN100E | 64 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | E |
| | LC4064V-75TN48E | 64 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | E |
| | LC4064V-75TN44E | 64 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | E |
| LC4128V | LC4128V-75TN144E | 128 | 3.3 | 7.5 | Lead-free TQFP | 144 | 96 | E |
| | LC4128V-75TN128E | 128 | 3.3 | 7.5 | Lead-free TQFP | 128 | 92 | E |
| | LC4128V-75TN100E | 128 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | E |
| LC4256V | LC4256V-75TN176E | 256 | 3.3 | 7.5 | Lead-free TQFP | 176 | 128 | E |
| | LC4256V-75TN144E | 256 | 3.3 | 7.5 | Lead-free TQFP | 144 | 96 | E |
| | LC4256V-75TN100E | 256 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | E |

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| — | — | Previous Lattice releases. |
| July 2003 | 17z | Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices. |
| | | Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points (0 ≤ VIN ≤ 3.6V). |
| | | Added 132-ball chip scale BGA power supply and NC connections. |
| | | Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices. |
| | | Added lead-free package designators. |
| October 2003 | 18z | Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided (VIN - VCCO) ≤ 3.6V. |
| | | Improved LC4064ZC $t_S$ to 2.5ns, $t_{ST}$ to 2.7ns and $f_{MAX}$ (Ext.) to 175MHz, LC4128ZC $t_{CO}$ to 3.5ns and $f_{MAX}$ (Ext.) to 161MHz (version v.2.1). |
| | | Improved associated internal timing numbers and timing adders (version v.2.1). |
| | | Added ispMACH 4000V/B/C/Z ORP Reference Tables. |
| | | Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11). |
| | | Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version. |
| | | Added the ispMACH 4000 Family Speed Grade Offering table. |
| | | Added the ispMACH 4128ZC Industrial and Automotive Device OPNs |
| December 2003 | 19z | Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs |