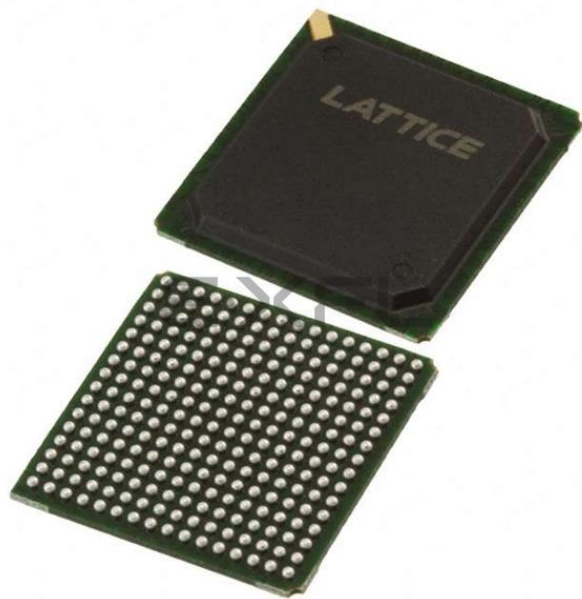




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	3 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	128
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-3fn256ac

Table 2. ispMACH 4000Z Family Selection Guide

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t _{PD} (ns)	3.5	3.7	4.2	4.5
t _S (ns)	2.2	2.5	2.7	2.9
t _{CO} (ns)	3.0	3.2	3.5	3.8
f _{MAX} (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I _{CC} (μA)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

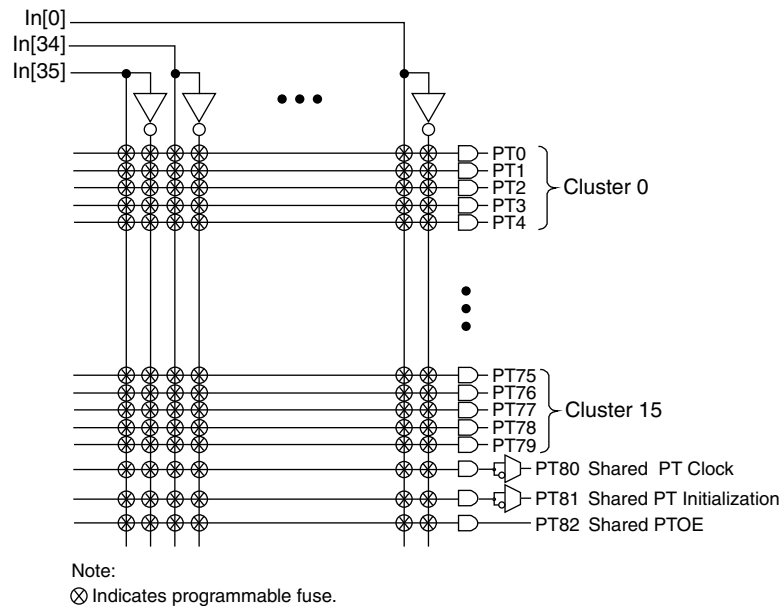
The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 3. AND Array

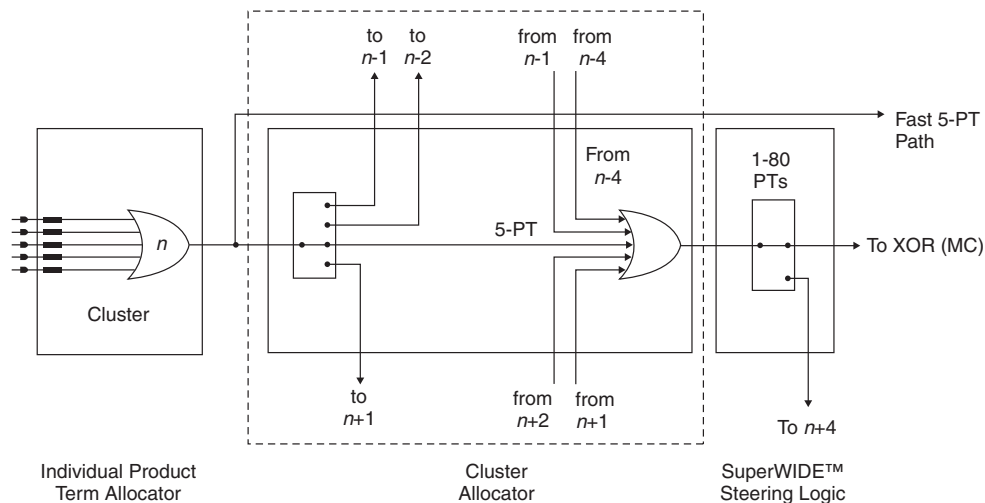
Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator

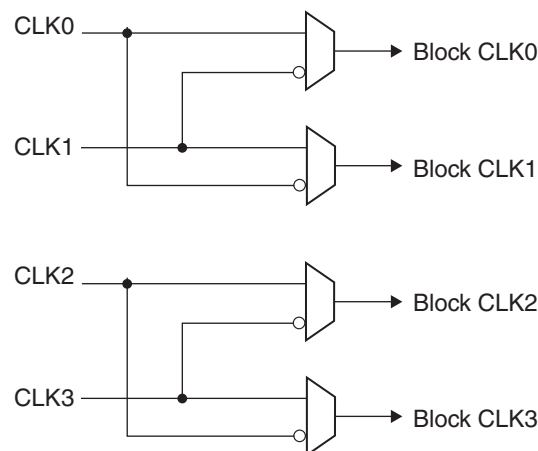


Table 10. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO} .

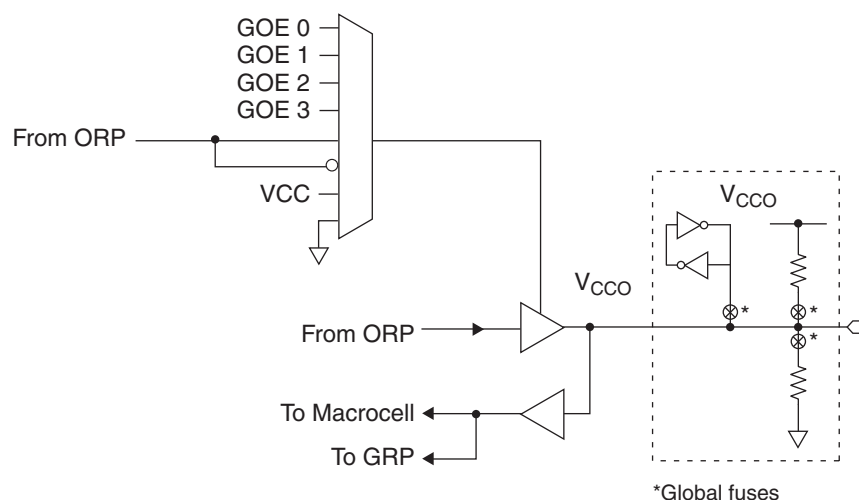
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

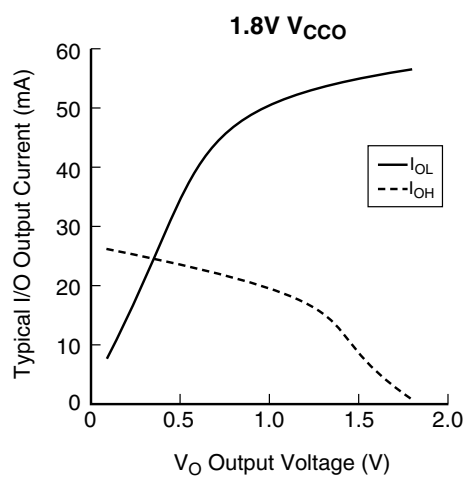
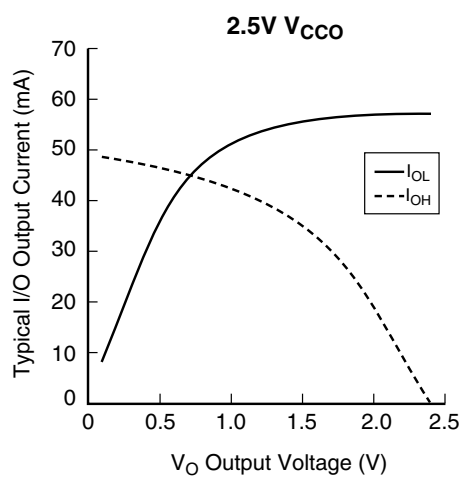
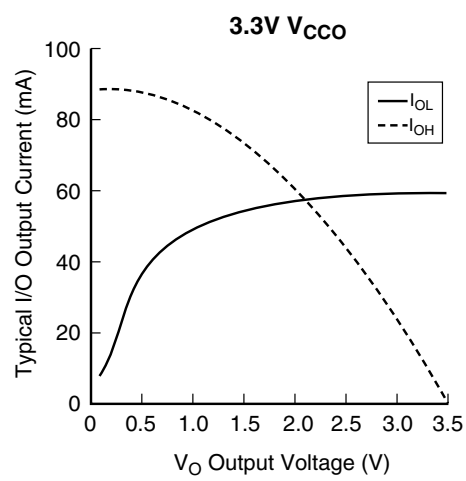
I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:



ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{GPTOE}	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t _{PPTOE}	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4000V/B/C Timing Adders¹

Adder Type	Base Parameter	Description	-25		-27		-3		-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders											
t _{INDIO}	t _{INREG}	Input register delay	—	0.95	—	1.00	—	1.00	—	1.00	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	—	0.33	ns
t _{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	—	0.05	ns
t _{BLA}	t _{ROUTE}	Additional block loading adder	—	0.03	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters											
LVTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters											
LVTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
P8	1	NC ¹	-	NC ¹	-	I ¹	-
M8	1	NC	-	E0	E ⁰	I2	I ¹
P9	1	C0	C ⁰	E1	E ¹	I4	I ²
N9	1	C1	C ¹	E2	E ²	I6	I ³
M9	1	C2	C ²	E4	E ³	I8	I ⁴
N10	1	C3	C ³	E5	E ⁴	I10	I ⁵
P10	1	NC	-	E6	E ⁵	I12	I ⁶
M10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
N11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P11	1	NC	-	E8	E ⁶	J2	J ¹
M11	1	C4	C ⁴	E9	E ⁷	J4	J ²
P12	1	C5	C ⁵	E10	E ⁸	J6	J ³
N12	1	C6	C ⁶	E12	E ⁹	J8	J ⁴
P13	1	C7	C ⁷	E13	E ¹⁰	J10	J ⁵
P14	1	NC	-	E14	E ¹¹	J12	J ⁶
N14	-	GND	-	GND	-	GND	-
N13	-	TMS	-	TMS	-	TMS	-
M14	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
M12	1	NC	-	F0	F ⁰	K12	K ⁶
M13	1	C8	C ⁸	F1	F ¹	K10	K ⁵
L14	1	C9	C ⁹	F2	F ²	K8	K ⁴
L12	1	C10	C ¹⁰	F4	F ³	K6	K ³
L13	1	C11	C ¹¹	F5	F ⁴	K4	K ²
K14	1	NC	-	F6	F ⁵	K2	K ¹
K13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
K12	1	NC	-	F8	F ⁶	L12	L ⁶
J13	1	C12	C ¹²	F9	F ⁷	L10	L ⁵
J14	1	C13	C ¹³	F10	F ⁸	L8	L ⁴
J12	1	C14	C ¹⁴	F12	F ⁹	L6	L ³
H14	1	C15	C ¹⁵	F13	F ¹⁰	L4	L ²
H13	1	I	-	F14	F ¹¹	L2	L ¹
H12	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
G13	1	NC	-	G14	G ¹¹	M2	M ¹
G14	1	NC	-	G13	G ¹⁰	M4	M ²
G12	1	D15	D ¹⁵	G12	G ⁹	M6	M ³
F14	1	D14	D ¹⁴	G10	G ⁸	M8	M ⁴
F13	1	D13	D ¹³	G9	G ⁷	M10	M ⁵
F12	1	D12	D ¹²	G8	G ⁶	M12	M ⁶
E13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
E14	1	NC	-	G6	G ⁵	N2	N ¹
E12	1	D11	D ¹¹	G5	G ⁴	N4	N ²

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D [^] 7	G4	G [^] 2
44	0	D8	D [^] 6	G2	G [^] 1
45	0	NC ²	-	I ²	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D [^] 5	H12	H [^] 6
49	0	D5	D [^] 4	H10	H [^] 5
50	0	D4	D [^] 3	H8	H [^] 4
51	0	D2	D [^] 2	H6	H [^] 3
52	0	D1	D [^] 1	H4	H [^] 2
53	0	D0	D [^] 0	H2	H [^] 1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E [^] 0	I2	I [^] 1
59	1	E1	E [^] 1	I4	I [^] 2
60	1	E2	E [^] 2	I6	I [^] 3
61	1	E4	E [^] 3	I8	I [^] 4
62	1	E5	E [^] 4	I10	I [^] 5
63	1	E6	E [^] 5	I12	I [^] 6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E [^] 6	J2	J [^] 1
67	1	E9	E [^] 7	J4	J [^] 2
68	1	E10	E [^] 8	J6	J [^] 3
69	1	E12	E [^] 9	J8	J [^] 4
70	1	E13	E [^] 10	J10	J [^] 5
71	1	E14	E [^] 11	J12	J [^] 6
72	1	NC ²	-	I ²	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F [^] 0	K12	K [^] 6
77	1	F1	F [^] 1	K10	K [^] 5
78	1	F2	F [^] 2	K8	K [^] 4
79	1	F4	F [^] 3	K6	K [^] 3
80	1	F5	F [^] 4	K4	K [^] 2
81	1	F6	F [^] 5	K2	K [^] 1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F [^] 6	L14	L [^] 7
84	1	F9	F [^] 7	L12	L [^] 6
85	1	F10	F [^] 8	L10	L [^] 5

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C ⁷	C14	C ⁹	C14	C ⁷	C14	C ⁷
F5	0	C12	C ⁶	C12	C ⁸	C12	C ⁶	C12	C ⁶
D3	0	C10	C ⁵	C10	C ⁷	C10	C ⁵	C10	C ⁵
C1	0	C8	C ⁴	C9	C ⁶	C8	C ⁴	C8	C ⁴
C2	0	C6	C ³	C8	C ⁵	C6	C ³	C6	C ³
E3	0	C4	C ²	C6	C ⁴	C4	C ²	C4	C ²
D2	0	C2	C ¹	C4	C ³	C2	C ¹	C2	C ¹
F6	0	C0	C ⁰	C2	C ²	C0	C ⁰	C0	C ⁰
D1	0	NC	-	C1	C ¹	F6	F ³	H0	H ⁰
E2	0	NC	-	C0	C ⁰	F4	F ²	H4	H ¹
E4	0	NC	-	NC	-	D6	D ³	F4	F ²
G5	0	NC	-	NC	-	D4	D ²	F6	F ³
E1	0	NC	-	NC	-	NC	-	F8	F ⁴
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F ⁵
F1	0	NC	-	NC	-	D2	D ¹	F12	F ⁶
G1	0	NC	-	NC	-	D0	D ⁰	F14	F ⁷
G6	0	NC	-	D14	D ⁹	F2	F ¹	H8	H ²
G4	0	NC	-	D12	D ⁸	F0	F ⁰	H12	H ³
H6	0	D14	D ⁷	D10	D ⁷	E14	E ⁷	G14	G ⁷
G3	0	D12	D ⁶	D9	D ⁶	E12	E ⁶	G12	G ⁶
H5	0	D10	D ⁵	D8	D ⁵	E10	E ⁵	G10	G ⁵
G2	0	D8	D ⁴	D6	D ⁴	E8	E ⁴	G8	G ⁴
H1	0	D6	D ³	D4	D ³	E6	E ³	G6	G ³
H2	0	D4	D ²	D2	D ²	E4	E ²	G4	G ²
H3	0	D2	D ¹	D1	D ¹	E2	E ¹	G2	G ¹
H4	0	D0	D ⁰	D0	D ⁰	E0	E ⁰	G0	G ⁰
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E ⁰	E0	E ⁰	H0	H ⁰	J0	J ⁰
J3	0	E2	E ¹	E1	E ¹	H2	H ¹	J2	J ¹
J2	0	E4	E ²	E2	E ²	H4	H ²	J4	J ²
J1	0	E6	E ³	E4	E ³	H6	H ³	J6	J ³
K1	0	E8	E ⁴	E6	E ⁴	H8	H ⁴	J8	J ⁴
J5	0	E10	E ⁵	E8	E ⁵	H10	H ⁵	J10	J ⁵
K2	0	E12	E ⁶	E9	E ⁶	H12	H ⁶	J12	J ⁶

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E ⁷	E10	E ⁷	H14	H ⁷	J14	J ⁷
K3	0	NC	-	E12	E ⁸	G0	G ⁰	I0	I ⁰
K4	0	NC	-	E14	E ⁹	G2	G ¹	I4	I ¹
L1	0	NC	-	NC	-	I14	I ⁷	K0	K ⁰
L2	0	NC	-	NC	-	I12	I ⁶	K2	K ¹
M1	0	NC	-	NC	-	NC	-	K4	K ²
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K ³
N1	0	NC	-	NC	-	I10	I ⁵	K8	K ⁴
M3	0	NC	-	NC	-	I8	I ⁴	K10	K ⁵
M4	0	NC	-	F0	F ⁰	G4	G ²	I8	I ²
N2	0	NC	-	F1	F ¹	G6	G ³	I12	I ³
K5	0	F0	F ⁰	F2	F ²	J0	J ⁰	N0	N ⁰
P1	0	F2	F ¹	F4	F ³	J2	J ¹	N2	N ¹
K6	0	F4	F ²	F6	F ⁴	J4	J ²	N4	N ²
N3	0	F6	F ³	F8	F ⁵	J6	J ³	N6	N ³
L5	0	F8	F ⁴	F9	F ⁶	J8	J ⁴	N8	N ⁴
P2	0	F10	F ⁵	F10	F ⁷	J10	J ⁵	N10	N ⁵
L6	0	F12	F ⁶	F12	F ⁸	J12	J ⁶	N12	N ⁶
R1	0	F14	F ⁷	F14	F ⁹	J14	J ⁷	N14	N ⁷
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G ⁹	I6	I ³	K12	K ⁶
M5	0	NC	-	G12	G ⁸	I4	I ²	K14	K ⁷
N4	0	G14	G ⁷	G10	G ⁷	K14	K ⁷	O14	O ⁷
T3	0	G12	G ⁶	G9	G ⁶	K12	K ⁶	O12	O ⁶
R3	0	G10	G ⁵	G8	G ⁵	K10	K ⁵	O10	O ⁵
M6	0	G8	G ⁴	G6	G ⁴	K8	K ⁴	O8	O ⁴
P4	0	G6	G ³	G4	G ³	K6	K ³	O6	O ³
L7	0	G4	G ²	G2	G ²	K4	K ²	O4	O ²
N5	0	G2	G ¹	G1	G ¹	K2	K ¹	O2	O ¹
M7	0	G0	G ⁰	G0	G ⁰	K0	K ⁰	O0	O ⁰
P5	0	NC	-	NC	-	G8	G ⁴	M0	M ⁰
R4	0	NC	-	NC	-	G10	G ⁵	M4	M ¹
T4	0	NC	-	NC	-	NC	-	L0	L ⁰
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

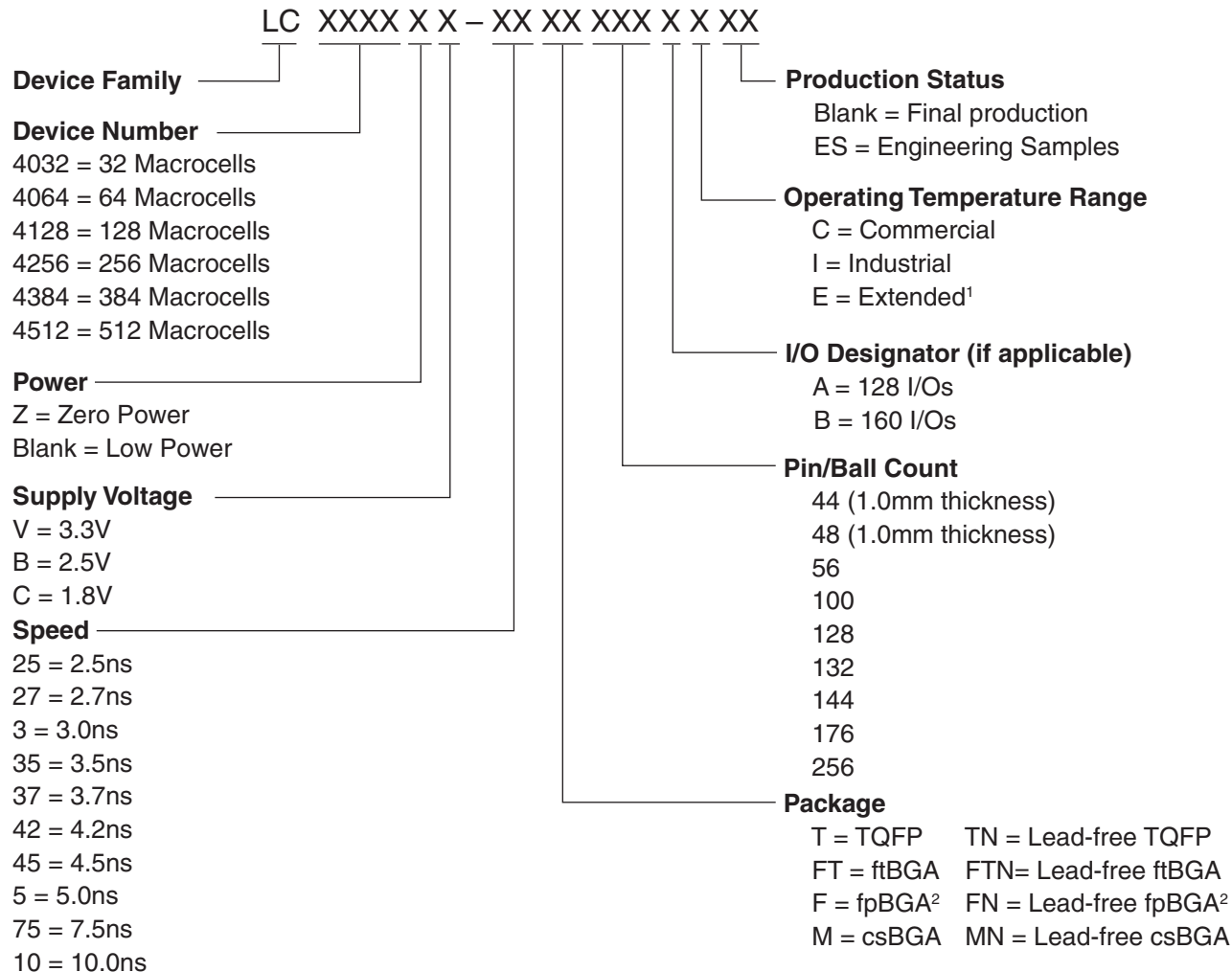
Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M ¹	M1	M ¹	DX2	DX ¹	JX2	JX ¹
H14	1	M4	M ²	M2	M ²	DX4	DX ²	JX4	JX ²
H13	1	M6	M ³	M4	M ³	DX6	DX ³	JX6	JX ³
G16	1	M8	M ⁴	M6	M ⁴	DX8	DX ⁴	JX8	JX ⁴
H12	1	M10	M ⁵	M8	M ⁵	DX10	DX ⁵	JX10	JX ⁵
G15	1	M12	M ⁶	M9	M ⁶	DX12	DX ⁶	JX12	JX ⁶
H11	1	M14	M ⁷	M10	M ⁷	DX14	DX ⁷	JX14	JX ⁷
F16	1	NC	-	M12	M ⁸	CX0	CX ⁰	IX0	IX ⁰
G13	1	NC	-	M14	M ⁹	CX2	CX ¹	IX4	IX ¹
G14	1	NC	-	NC	-	EX14	EX ⁷	KX0	KX ⁰
F15	1	NC	-	NC	-	EX12	EX ⁶	KX2	KX ¹
E16	1	NC	-	NC	-	NC	-	KX4	KX ²
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX ³
G12	1	NC	-	NC	-	EX10	EX ⁵	KX8	KX ⁴
E13	1	NC	-	NC	-	EX8	EX ⁴	KX10	KX ⁵
D16	1	NC	-	N0	N ⁰	CX4	CX ²	IX8	IX ²
E14	1	NC	-	N1	N ¹	CX6	CX ³	IX12	IX ³
G11	1	N0	N ⁰	N2	N ²	FX0	FX ⁰	NX0	NX ⁰
D15	1	N2	N ¹	N4	N ³	FX2	FX ¹	NX2	NX ¹
F11	1	N4	N ²	N6	N ⁴	FX4	FX ²	NX4	NX ²
C16	1	N6	N ³	N8	N ⁵	FX6	FX ³	NX6	NX ³
F12	1	N8	N ⁴	N9	N ⁶	FX8	FX ⁴	NX8	NX ⁴
D14	1	N10	N ⁵	N10	N ⁷	FX10	FX ⁵	NX10	NX ⁵
C15	1	N12	N ⁶	N12	N ⁸	FX12	FX ⁶	NX12	NX ⁶
B16	1	N14	N ⁷	N14	N ⁹	FX14	FX ⁷	NX14	NX ⁷
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX ³	KX12	KX ⁶
B14	1	NC	-	NC	-	EX4	EX ²	KX14	KX ⁷
E12	1	O14	O ⁷	O14	O ⁹	GX14	GX ⁷	OX14	OX ⁷
A14	1	O12	O ⁶	O12	O ⁸	GX12	GX ⁶	OX12	OX ⁶
C13	1	O10	O ⁵	O10	O ⁷	GX10	GX ⁵	OX10	OX ⁵
D13	1	O8	O ⁴	O9	O ⁶	GX8	GX ⁴	OX8	OX ⁴
E11	1	O6	O ³	O8	O ⁵	GX6	GX ³	OX6	OX ³
B13	1	O4	O ²	O6	O ⁴	GX4	GX ²	OX4	OX ²
F10	1	O2	O ¹	O4	O ³	GX2	GX ¹	OX2	OX ¹

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B ¹	F8	F ⁴	D12	D ³
A3	0	B0	B ⁰	B2	B ²	B0	B ⁰	B0	B ⁰
F7	0	B2	B ¹	B4	B ³	B2	B ¹	B2	B ¹
B4	0	B4	B ²	B6	B ⁴	B4	B ²	B4	B ²
C5	0	B6	B ³	B8	B ⁵	B6	B ³	B6	B ³
A2	0	B8	B ⁴	B9	B ⁶	B8	B ⁴	B8	B ⁴
E6	0	B10	B ⁵	B10	B ⁷	B10	B ⁵	B10	B ⁵
B3	0	B12	B ⁶	B12	B ⁸	B12	B ⁶	B12	B ⁶
C4	0	B14	B ⁷	B14	B ⁹	B14	B ⁷	B14	B ⁷
D4	0	NC	-	NC	-	D10	D ⁵	F0	F ⁰
E5	0	NC	-	NC	-	D8	D ⁴	F2	F ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispMACH 4000Z devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

Conventional Packaging

ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35M56C	32	1.8	3.5	csBGA	56	32	C
	LC4032ZC-5M56C	32	1.8	5	csBGA	56	32	C
	LC4032ZC-75M56C	32	1.8	7.5	csBGA	56	32	C
	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32	C
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32	C
LC4064ZC	LC4064ZC-37M132C	64	1.8	3.7	csBGA	132	64	C
	LC4064ZC-5M132C	64	1.8	5	csBGA	132	64	C
	LC4064ZC-75M132C	64	1.8	7.5	csBGA	132	64	C
	LC4064ZC-37T100C	64	1.8	3.7	TQFP	100	64	C
	LC4064ZC-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064ZC-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064ZC-37M56C	64	1.8	3.7	csBGA	56	32	C
	LC4064ZC-5M56C	64	1.8	5	csBGA	56	32	C
	LC4064ZC-75M56C	64	1.8	7.5	csBGA	56	32	C
	LC4064ZC-37T48C	64	1.8	3.7	TQFP	48	32	C
	LC4064ZC-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064ZC-75T48C	64	1.8	7.5	TQFP	48	32	C
LC4128ZC	LC4128ZC-42M132C	128	1.8	4.2	csBGA	132	96	C
	LC4128ZC-75M132C	128	1.8	7.5	csBGA	132	96	C
	LC4128ZC-42T100C	128	1.8	4.2	TQFP	100	64	C
	LC4128ZC-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256ZC	LC4256ZC-45T176C	256	1.8	4.5	TQFP	176	128	C
	LC4256ZC-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256ZC-45M132C	256	1.8	4.5	csBGA	132	96	C
	LC4256ZC-75M132C	256	1.8	7.5	csBGA	132	96	C
	LC4256ZC-45T100C	256	1.8	4.5	TQFP	100	64	C
	LC4256ZC-75T100C	256	1.8	7.5	TQFP	100	64	C

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5M56I	32	1.8	5	csBGA	56	32	I
	LC4032ZC-75M56I	32	1.8	7.5	csBGA	56	32	I
	LC4032ZC-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032ZC-75T48I	32	1.8	7.5	TQFP	48	32	I

ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-5FT256I	384	2.5	5	ftBGA	256	192	I
	LC4384B-75FT256I	384	2.5	7.5	ftBGA	256	192	I
	LC4384B-10FT256I	384	2.5	10	ftBGA	256	192	I
	LC4384B-5F256I ¹	384	2.5	5	fpBGA	256	192	I
	LC4384B-75F256I ¹	384	2.5	7.5	fpBGA	256	192	I
	LC4384B-10F256I ¹	384	2.5	10	fpBGA	256	192	I
	LC4384B-5T176I	384	2.5	5	TQFP	176	128	I
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128	I
	LC4384B-10T176I	384	2.5	10	TQFP	176	128	I
LC4512B	LC4512B-5FT256I	512	2.5	5	ftBGA	256	208	I
	LC4512B-75FT256I	512	2.5	7.5	ftBGA	256	208	I
	LC4512B-10FT256I	512	2.5	10	ftBGA	256	208	I
	LC4512B-5F256I ¹	512	2.5	5	fpBGA	256	208	I
	LC4512B-75F256I ¹	512	2.5	7.5	fpBGA	256	208	I
	LC4512B-10F256I ¹	512	2.5	10	fpBGA	256	208	I
	LC4512B-5T176I	512	2.5	5	TQFP	176	128	I
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
	LC4512B-10T176I	512	2.5	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32	C
	LC4032V-5T48C	32	3.3	5	TQFP	48	32	C
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32	C
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30	C
	LC4032V-5T44C	32	3.3	5	TQFP	44	30	C
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30	C
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64	C
	LC4064V-5T100C	64	3.3	5	TQFP	100	64	C
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64	C
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32	C
	LC4064V-5T48C	64	3.3	5	TQFP	48	32	C
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32	C
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30	C
	LC4064V-5T44C	64	3.3	5	TQFP	44	30	C
	LC4064V-75T44C	64	3.3	7.5	TQFP	44	30	C

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C ¹	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C ¹	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C ¹	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI ¹	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI ¹	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI ¹	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI ¹	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI ¹	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI ¹	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
	LC4256V-10T100I	256	3.3	10	TQFP	100	64	I
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I ¹	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I ¹	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I ¹	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I ¹	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I ¹	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I ¹	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.