Lattice Semiconductor Corporation - LC4256B-5FT256BC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-5ft256bc

Table 10. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

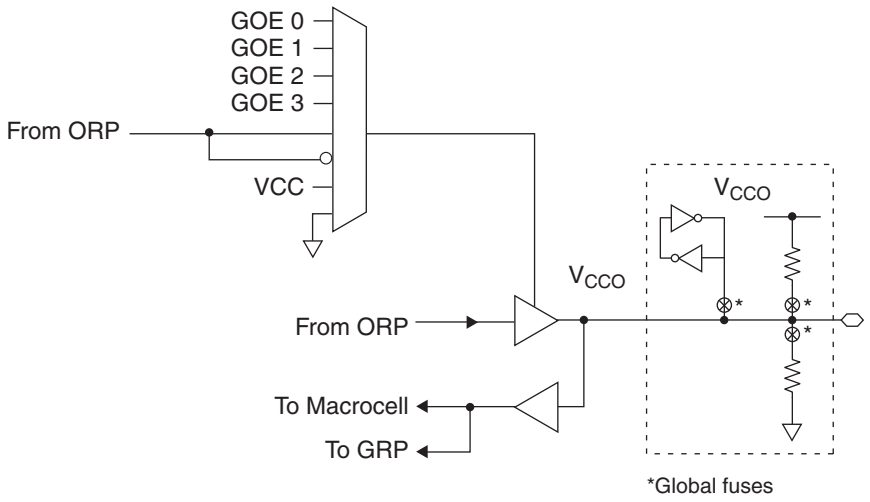
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

Supply Current, ispMACH 4000V/B/C

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032V/B/C						
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	11.8	—	mA
		Vcc = 2.5V	—	11.8	—	mA
		Vcc = 1.8V	—	1.8	—	mA
ICC^{4}	Standby Power Supply Current	Vcc = 3.3V	—	11.3	—	mA
		Vcc = 2.5V	—	11.3	—	mA
		Vcc = 1.8V	—	1.3	—	mA
ispMACH 4064V/B/C						
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
		Vcc = 2.5V	—	12	—	mA
		Vcc = 1.8V	—	2	—	mA
ICC^{5}	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
		Vcc = 2.5V	—	11.5	—	mA
		Vcc = 1.8V	—	1.5	—	mA
ispMACH 4128V/B/C						
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
		Vcc = 2.5V	—	12	—	mA
		Vcc = 1.8V	—	2	—	mA
ICC^{4}	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
		Vcc = 2.5V	—	11.5	—	mA
		Vcc = 1.8V	—	1.5	—	mA
ispMACH 4256V/B/C						
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12.5	—	mA
		Vcc = 2.5V	—	12.5	—	mA
		Vcc = 1.8V	—	2.5	—	mA
I_{CC}^{4}	Standby Power Supply Current	Vcc = 3.3V	—	12	—	mA
		Vcc = 2.5V	—	12	—	mA
		Vcc = 1.8V	—	2	—	mA
ispMACH 4384V/B/C						
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	13.5	—	mA
		Vcc = 2.5V	—	13.5	—	mA
		Vcc = 1.8V	—	3.5	—	mA
I_{CC}^{4}	Standby Power Supply Current	Vcc = 3.3V	—	12.5	—	mA
		Vcc = 2.5V	—	12.5	—	mA
		Vcc = 1.8V	—	2.5	—	mA
ispMACH 4512V/B/C						
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	14	—	mA
		Vcc = 2.5V	—	14	—	mA
		Vcc = 1.8V	—	4	—	mA

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	341	—	µA
		Vcc = 1.9V, T_A = 70°C	—	361	—	µA
		Vcc = 1.9V, T_A = 85°C	—	372	—	µA
		Vcc = 1.9V, T_A = 125°C	—	468	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	13	—	µA
		Vcc = 1.9V, T_A = 70°C	—	32	55	µA
		Vcc = 1.9V, T_A = 85°C	—	43	90	µA
		Vcc = 1.9V, T_A = 125°C	—	135	—	µA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t_S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t_{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t_R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t_{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t_{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$	—	250	—	222	—	212	—	212	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PTOE}	Macrocell PT OE Delay	—	2.50	—	2.70	—	2.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4000Z Timing Adders [1]

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.00	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t_{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding the use of these adders.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank.	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032	y: A-B
	ispMACH 4064	y: A-D
	ispMACH 4128	y: A-H
	ispMACH 4256	y: A-P
	ispMACH 4384	y: A-P, AX-HX
	ispMACH 4512	y: A-P, AX-PX

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

ispMACH 4000V/B/C ORP Reference Table

	4032V/B/C		4064V/B/C			4128V/B/C			4256V/B/C				4384V/B/C		4512V/B/C	
Number of I/Os	30[1]	32	30[2]	32	64	64	92[3]	96	64	96[4]	128	160	128	192	128	208
Number of GLBs	2	2	4	4	4	8	8	8	16	16	16	16	16	16	16	16
Number of I/Os / GLB	16	16	8	8	16	8	12	12	4	8	8	10	8	8	8	Mixture of 8 & 4[5]
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB		4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	10 I/Os / GLB	8 I/Os / GLB		8 I/Os / GLB	8 I/Os / GLB 4 I/Os / GLB

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.
2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.
3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os
4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per
5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

ispMACH 4000Z ORP Reference Table

	4032Z	4064Z		4128Z		4256Z		
Number of I/Os	32	32	64	64	96	64	96[1]	128
Number of GLBs	2	4	4	8	8	16	16	16
Number of I/Os / GLB	16	8	16	8	12	4	8	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

ispMACH 4000V/B/C/Z Power Supply and NC Connections[1]

Signal	44-pin TQFP[2]	48-pin TQFP[2]	56-ball csBGA[3]	100-pin TQFP[2]	128-pin TQFP[2]
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	**4032Z**: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispMACH 4000V/B/C/Z Power Supply and NC Connections[1] (Cont.)

Signal	132-ball csBGA[7]	144-pin TQFP[4]	176-pin TQFP[4]	256-ball ftBGA/fpBGA[2, 3, 7, 9]
VCC	P1, A14, B7, N8	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
VCCO0 VCCO (Bank 0)	G3, P5, C1[8], M2[8], C5	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1 VCCO (Bank 1)	M10, M14[8], H12, A10, C13[8]	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	B1, P2, N14, A13	1, 37, 73, 109	2, 46[5], 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank 0)	E2, K2, N4, B4	10, 18[6], 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	N11, K13, E13, B11	55, 65, 82, 90[6], 99, 118	67, 79, 101, 119, 143	
NC	**4064Z:** C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1 **4128Z:** P8, A7	**4128V**: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 **4256V**: 18, 90	1, 43, 44, 45, 89, 131, 132, 133	**4256V/B/C, 128 I/O:** A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15 **4256V/B/C, 160 I/O:** A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15 **4384V/B/C:** B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4 **4512V/B/C:** None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. V_{CCO} balls connect to two power planes within the package, one for V_{CCO0} and one for V_{CCO1}.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
4	0	B0	B^0	C12	C^6
5	0	B1	B^1	C10	C^5
6	0	B2	B^2	C8	C^4
7	0	B4	B^3	C6	C^3
8	0	B5	B^4	C4	C^2
9	0	B6	B^5	C2	C^1
10	0	GND (Bank 0)	-	GND (Bank 0)	-
11	0	B8	B^6	D14	D^7
12	0	B9	B^7	D12	D^6
13	0	B10	B^8	D10	D^5
14	0	B12	B^9	D8	D^4
15	0	B13	B^10	D6	D^3
16	0	B14	B^11	D4	D^2
17	-	NC[2]	-	I[2]	-
18	0	GND (Bank 0)[1]	-	NC[1]	-
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
20	0	NC[2]	-	I[2]	-
21	0	C14	C^11	E2	E^1
22	0	C13	C^10	E4	E^2
23	0	C12	C^9	E6	E^3
24	0	C10	C^8	E8	E^4
25	0	C9	C^7	E10	E^5
26	0	C8	C^6	E12	E^6
27	0	GND (Bank 0)	-	GND (Bank 0)	-
28	0	C6	C^5	F2	F^1
29	0	C5	C^4	F4	F^2
30	0	C4	C^3	F6	F^3
31	0	C2	C^2	F8	F^4
32	0	C1	C^1	F10	F^5
33	0	C0	C^0	F12	F^6
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
35	-	TCK	-	TCK	-
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	0	NC[2]	-	I[2]	-
39	0	D14	D^11	G12	G^6
40	0	D13	D^10	G10	G^5
41	0	D12	D^9	G8	G^4
42	0	D10	D^8	G6	G^3

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC[2]	-	I[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C^7	C14	C^9	C14	C^7	C14	C^7
F5	0	C12	C^6	C12	C^8	C12	C^6	C12	C^6
D3	0	C10	C^5	C10	C^7	C10	C^5	C10	C^5
C1	0	C8	C^4	C9	C^6	C8	C^4	C8	C^4
C2	0	C6	C^3	C8	C^5	C6	C^3	C6	C^3
E3	0	C4	C^2	C6	C^4	C4	C^2	C4	C^2
D2	0	C2	C^1	C4	C^3	C2	C^1	C2	C^1
F6	0	C0	C^0	C2	C^2	C0	C^0	C0	C^0
D1	0	NC	-	C1	C^1	F6	F^3	H0	H^0
E2	0	NC	-	C0	C^0	F4	F^2	H4	H^1
E4	0	NC	-	NC	-	D6	D^3	F4	F^2
G5	0	NC	-	NC	-	D4	D^2	F6	F^3
E1	0	NC	-	NC	-	NC	-	F8	F^4
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F^5
F1	0	NC	-	NC	-	D2	D^1	F12	F^6
G1	0	NC	-	NC	-	D0	D^0	F14	F^7
G6	0	NC	-	D14	D^9	F2	F^1	H8	H^2
G4	0	NC	-	D12	D^8	F0	F^0	H12	H^3
H6	0	D14	D^7	D10	D^7	E14	E^7	G14	G^7
G3	0	D12	D^6	D9	D^6	E12	E^6	G12	G^6
H5	0	D10	D^5	D8	D^5	E10	E^5	G10	G^5
G2	0	D8	D^4	D6	D^4	E8	E^4	G8	G^4
H1	0	D6	D^3	D4	D^3	E6	E^3	G6	G^3
H2	0	D4	D^2	D2	D^2	E4	E^2	G4	G^2
H3	0	D2	D^1	D1	D^1	E2	E^1	G2	G^1
H4	0	D0	D^0	D0	D^0	E0	E^0	G0	G^0
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E^0	E0	E^0	H0	H^0	J0	J^0
J3	0	E2	E^1	E1	E^1	H2	H^1	J2	J^1
J2	0	E4	E^2	E2	E^2	H4	H^2	J4	J^2
J1	0	E6	E^3	E4	E^3	H6	H^3	J6	J^3
K1	0	E8	E^4	E6	E^4	H8	H^4	J8	J^4
J5	0	E10	E^5	E8	E^5	H10	H^5	J10	J^5
K2	0	E12	E^6	E9	E^6	H12	H^6	J12	J^6

ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I[1]	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I[1]	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I[1]	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I[1]	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I[1]	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I[1]	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC[1]	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC[1]	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC[1]	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC[1]	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC[1]	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC[1]	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C[1]	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C[1]	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C[1]	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C[1]	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C[1]	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C[1]	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064C	LC4064C-25TN100C	64	1.8	2.5	Lead-free TQFP	100	64	C
	LC4064C-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064C-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064C-25TN48C	64	1.8	2.5	Lead-free TQFP	48	32	C
	LC4064C-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064C-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
	LC4064C-25TN44C	64	1.8	2.5	Lead-free TQFP	44	30	C
	LC4064C-5TN44C	64	1.8	5	Lead-free TQFP	44	30	C
	LC4064C-75TN44C	64	1.8	7.5	Lead-free TQFP	44	30	C
LC4128C	LC4128C-27TN128C	128	1.8	2.7	Lead-free TQFP	128	92	C
	LC4128C-5TN128C	128	1.8	5	Lead-free TQFP	128	92	C
	LC4128C-75TN128C	128	1.8	7.5	Lead-free TQFP	128	92	C
	LC4128C-27TN100C	128	1.8	2.7	Lead-free TQFP	100	64	C
	LC4128C-5TN100C	128	1.8	5	Lead-free TQFP	100	64	C
	LC4128C-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256C	LC4256C-3FTN256AC	256	1.8	3	Lead-free ftBGA	256	128	C
	LC4256C-5FTN256AC	256	1.8	5	Lead-free ftBGA	256	128	C
	LC4256C-75FTN256AC	256	1.8	7.5	Lead-free ftBGA	256	128	C
	LC4256C-3FTN256BC	256	1.8	3	Lead-free ftBGA	256	160	C
	LC4256C-5FTN256BC	256	1.8	5	Lead-free ftBGA	256	160	C
	LC4256C-75FTN256BC	256	1.8	7.5	Lead-free ftBGA	256	160	C
	LC4256C-3FN256AC[1]	256	1.8	3	Lead-free fpBGA	256	128	C
	LC4256C-5FN256AC[1]	256	1.8	5	Lead-free fpBGA	256	128	C
	LC4256C-75FN256AC[1]	256	1.8	7.5	Lead-free fpBGA	256	128	C
	LC4256C-3FN256BC[1]	256	1.8	3	Lead-free fpBGA	256	160	C
	LC4256C-5FN256BC[1]	256	1.8	5	Lead-free fpBGA	256	160	C
	LC4256C-75FN256BC[1]	256	1.8	7.5	Lead-free fpBGA	256	160	C
	LC4256C-3TN176C	256	1.8	3	Lead-free TQFP	176	128	C
	LC4256C-5TN176C	256	1.8	5	Lead-free TQFP	176	128	C
	LC4256C-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256C-3TN100C	256	1.8	3	Lead-free TQFP	100	64	C
	LC4256C-5TN100C	256	1.8	5	Lead-free TQFP	100	64	C
	LC4256C-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C
LC4384C	LC4384C-35FTN256C	384	1.8	3.5	Lead-free ftBGA	256	192	C
	LC4384C-5FTN256C	384	1.8	5	Lead-free ftBGA	256	192	C
	LC4384C-75FTN256C	384	1.8	7.5	Lead-free ftBGA	256	192	C
	LC4384C-35FN256C[1]	384	1.8	3.5	Lead-free fpBGA	256	192	C
	LC4384C-5FN256C[1]	384	1.8	5	Lead-free fpBGA	256	192	C
	LC4384C-75FN256C[1]	384	1.8	7.5	Lead-free fpBGA	256	192	C
	LC4384C-35TN176C	384	1.8	3.5	Lead-free TQFP	176	128	C
	LC4384C-5TN176C	384	1.8	5	Lead-free TQFP	176	128	C
	LC4384C-75TN176C	384	1.8	7.5	Lead-free TQFP	176	128	C

ispMACH 4000V (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25TN48C	32	3.3	2.5	Lead-free TQFP	48	32	C
	LC4032V-5TN48C	32	3.3	5	Lead-free TQFP	48	32	C
	LC4032V-75TN48C	32	3.3	7.5	Lead-free TQFP	48	32	C
	LC4032V-25TN44C	32	3.3	2.5	Lead-free TQFP	44	30	C
	LC4032V-5TN44C	32	3.3	5	Lead-free TQFP	44	30	C
	LC4032V-75TN44C	32	3.3	7.5	Lead-free TQFP	44	30	C
LC4064V	LC4064V-25TN100C	64	3.3	2.5	Lead-free TQFP	100	64	C
	LC4064V-5TN100C	64	3.3	5	Lead-free TQFP	100	64	C
	LC4064V-75TN100C	64	3.3	7.5	Lead-free TQFP	100	64	C
	LC4064V-25TN48C	64	3.3	2.5	Lead-free TQFP	48	32	C
	LC4064V-5TN48C	64	3.3	5	Lead-free TQFP	48	32	C
	LC4064V-75TN48C	64	3.3	7.5	Lead-free TQFP	48	32	C
	LC4064V-25TN44C	64	3.3	2.5	Lead-free TQFP	44	30	C
	LC4064V-5TN44C	64	3.3	5	Lead-free TQFP	44	30	C
	LC4064V-75TN44C	64	3.3	7.5	Lead-free TQFP	44	30	C
LC4128V	LC4128V-27TN144C	128	3.3	2.7	Lead-free TQFP	144	96	C
	LC4128V-5TN144C	128	3.3	5	Lead-free TQFP	144	96	C
	LC4128V-75TN144C	128	3.3	7.5	Lead-free TQFP	144	96	C
	LC4128V-27TN128C	128	3.3	2.7	Lead-free TQFP	128	92	C
	LC4128V-5TN128C	128	3.3	5	Lead-free TQFP	128	92	C
	LC4128V-75TN128C	128	3.3	7.5	Lead-free TQFP	128	92	C
	LC4128V-27TN100C	128	3.3	2.7	Lead-free TQFP	100	64	C
	LC4128V-5TN100C	128	3.3	5	Lead-free TQFP	100	64	C
	LC4128V-75TN100C	128	3.3	7.5	Lead-free TQFP	100	64	C

ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points (0 ≤ VIN ≤ 3.6V).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided (VIN - VCCO) ≤ 3.6V.
		Improved LC4064ZC t_S to 2.5ns, t_{ST} to 2.7ns and f_{MAX} (Ext.) to 175MHz, LC4128ZC t_{CO} to 3.5ns and f_{MAX} (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs