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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	128
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-5ftn256ai">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-5ftn256ai</a>

**Table 2. ispMACH 4000Z Family Selection Guide**

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t <sub>PD</sub> (ns)	3.5	3.7	4.2	4.5
t <sub>S</sub> (ns)	2.2	2.5	2.7	2.9
t <sub>CO</sub> (ns)	3.0	3.2	3.5	3.8
f <sub>MAX</sub> (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I <sub>cc</sub> ( $\mu$ A)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

## ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

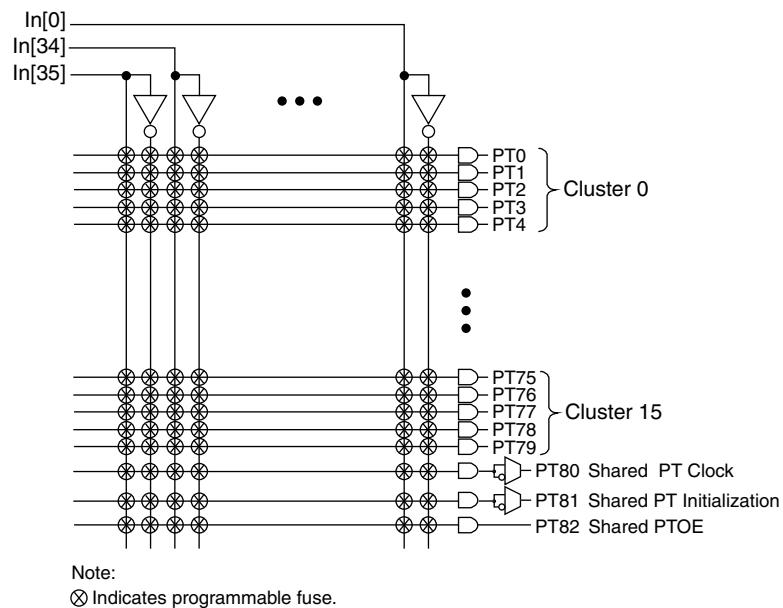
The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V<sub>CC</sub> (logic core).

## Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

**Figure 3. AND Array**

Note:  
⊗ Indicates programmable fuse.

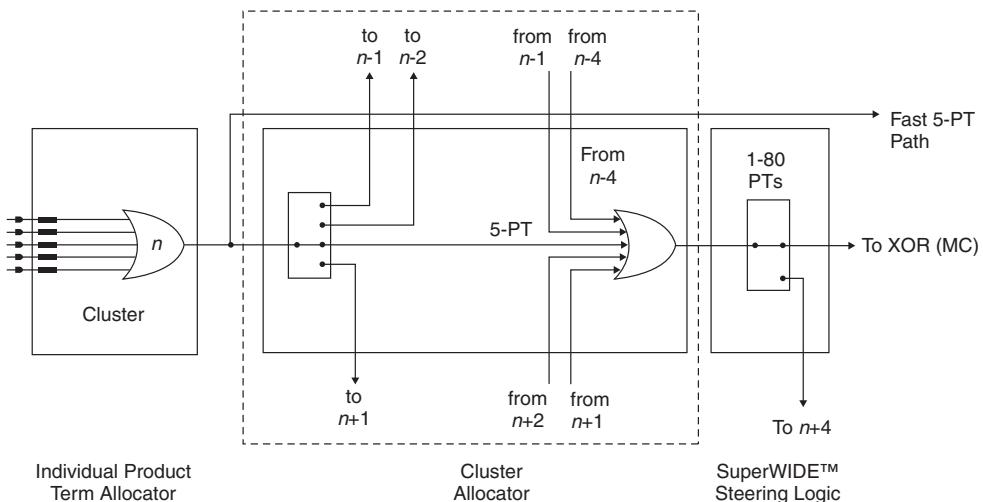
## Enhanced Logic Allocator

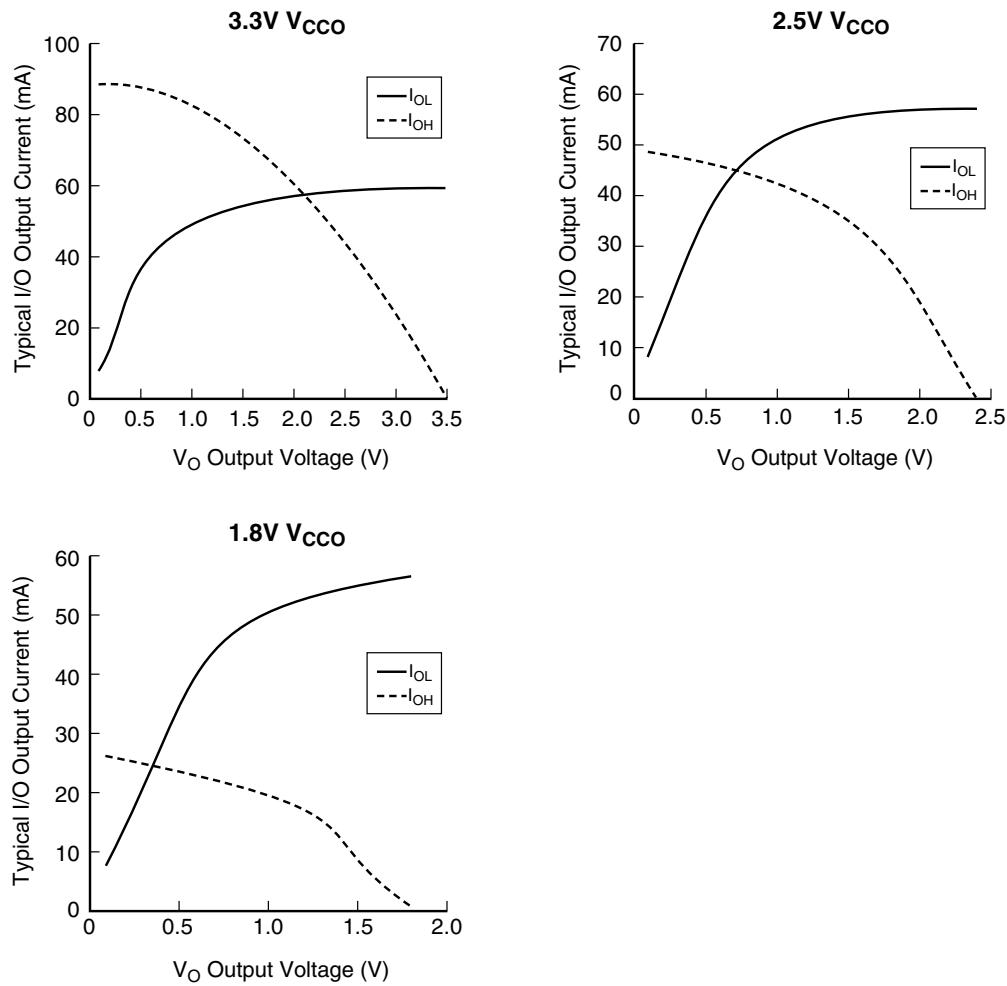
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

**Figure 4. Macrocell Slice**



**ispMACH 4000Z External Switching Characteristics****Over Recommended Operating Conditions**

Parameter	Description <sup>1, 2, 3</sup>	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PD}$	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
$t_{PD\_MC}$	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
$t_S$	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
$t_{ST}$	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
$t_{SIR}$	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
$t_{SIRZ}$	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
$t_H$	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
$t_{HT}$	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
$t_{HIR}$	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
$t_{HIRZ}$	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
$t_{CO}$	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
$t_R$	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
$t_{RW}$	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
$t_{CW}$	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
$t_{GW}$	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
$t_{WIR}$	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
$f_{MAX}^4$	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
$f_{MAX}$ (Ext.)	clock frequency with external feedback, $[1 / (t_S + t_{CO})]$	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVC MOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

**ispMACH 4000V/B/C Internal Timing Parameters (Cont.)****Over Recommended Operating Conditions**

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{GPTOE}$	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
$t_{PTOE}$	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

**ispMACH 4000Z Internal Timing Parameters**

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>								
$t_{IN}$	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
$t_{GOE}$	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
$t_{GCLK\_IN}$	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
$t_{BUF}$	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
$t_{EN}$	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
$t_{DIS}$	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
<b>Routing/GLB Delays</b>								
$t_{ROUTE}$	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
$t_{MCELL}$	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
$t_{INREG}$	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
$t_{FBK}$	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
$t_{PDb}$	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
$t_{PDi}$	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
<b>Register/Latch Delays</b>								
$t_S$	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
$t_{S\_PT}$	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
$t_{ST}$	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
$t_{ST\_PT}$	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
$t_H$	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
$t_{HT}$	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
$t_{SIR}$	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
$t_{SIR\_PT}$	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
$t_{HIR}$	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
$t_{HIR\_PT}$	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
$t_{COi}$	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
$t_{CES}$	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
$t_{CEH}$	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
$t_{SL}$	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
$t_{SL\_PT}$	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
$t_{HL}$	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
$t_{GOi}$	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
$t_{PDLi}$	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
$t_{SRi}$	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
$t_{SRR}$	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
<b>Control Delays</b>								
$t_{BCLK}$	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
$t_{PTCLK}$	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
$t_{BSR}$	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
$t_{PTSR}$	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

**ispMACH 4000Z Timing Adders<sup>1</sup>**

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.00	—	1.00	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

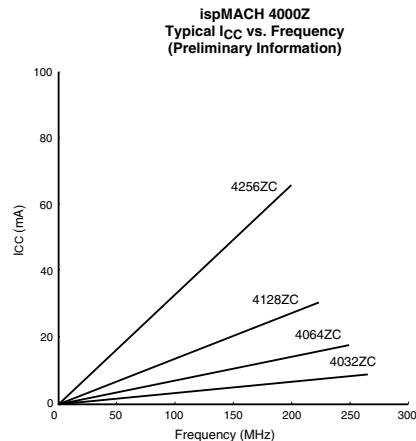
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

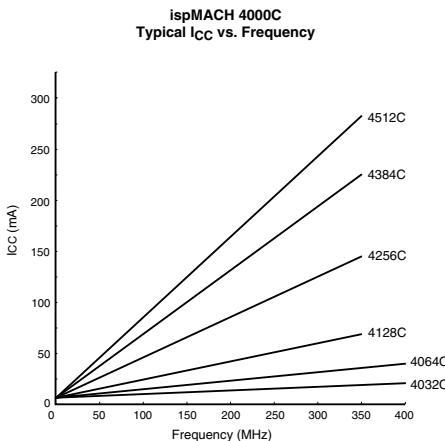
## Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
$t_{BTCP}$	TCK [BSCAN test] clock cycle	40	—	ns
$t_{BTCH}$	TCK [BSCAN test] pulse width high	20	—	ns
$t_{BTCL}$	TCK [BSCAN test] pulse width low	20	—	ns
$t_{BTSU}$	TCK [BSCAN test] setup time	8	—	ns
$t_{BTH}$	TCK [BSCAN test] hold time	10	—	ns
$t_{BRF}$	TCK [BSCAN test] rise and fall time	50	—	mV/ns
$t_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTOZ}$	TAP controller falling edge of clock to data output disable	—	10	ns
$t_{BTVO}$	TAP controller falling edge of clock to data output enable	—	10	ns
$t_{BTCPSU}$	BSCAN test Capture register setup time	8	—	ns
$t_{TCPH}$	BSCAN test Capture register hold time	10	—	ns
$t_{BTUCO}$	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
$t_{BTUOZ}$	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
$t_{BTUOV}$	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

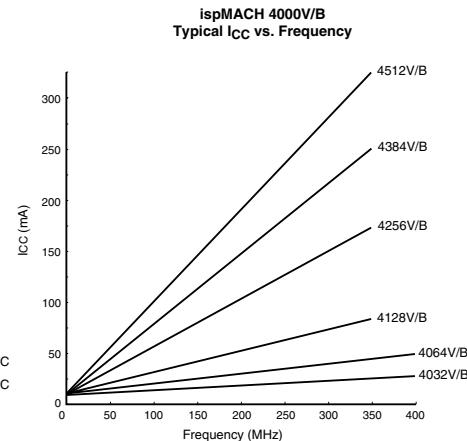
## Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

## Power Estimation Coefficients<sup>1</sup>

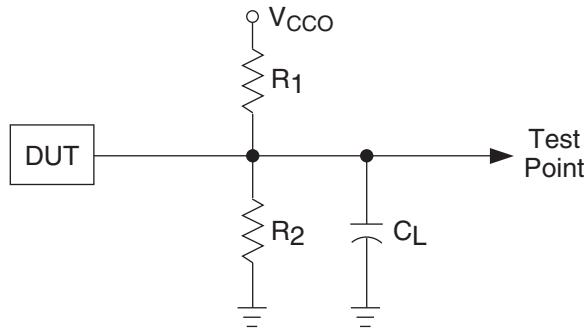
Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

- For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

## Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

**Figure 12. Output Test Load, LVTTL and LVC MOS Standards**



0213A/ispm4k

**Table 11. Test Fixture Required Components**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub> <sup>1</sup>	Timing Ref.	V <sub>CCO</sub>
LVC MOS I/O, (L → H, H → L)	106Ω	106Ω	35pF	LVC MOS 3.3 = 1.5V	LVC MOS 3.3 = 3.0V
				LVC MOS 2.5 = V <sub>CCO</sub> /2	LVC MOS 2.5 = 2.3V
				LVC MOS 1.8 = V <sub>CCO</sub> /2	LVC MOS 1.8 = 1.65V
LVC MOS I/O (Z → H)	∞	106Ω	35pF	1.5V	3.0V
LVC MOS I/O (Z → L)	106Ω	∞	35pF	1.5V	3.0V
LVC MOS I/O (H → Z)	∞	106Ω	5pF	V <sub>OH</sub> - 0.3	3.0V
LVC MOS I/O (L → Z)	106Ω	∞	5pF	V <sub>OL</sub> + 0.3	3.0V

1. C<sub>L</sub> includes test fixtures and probe capacitance.

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:  
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B^10	D4	D^2	D10	D^5
34	1	B11	B^11	D6	D^3	D8	D^4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B^12	D8	D^4	D6	D^3
39	1	B13	B^13	D10	D^5	D4	D^2
40	1	B14	B^14	D12	D^6	D2	D^1
41	1	B15/GOE1	B^15	D14/GOE1	D^7	D0/GOE1	D^0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A^0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1	A1	A^1
46	0	A2	A^2	A4	A^2	A2	A^2
47	0	A3	A^3	A6	A^3	A4	A^3
48	0	A4	A^4	A8	A^4	A6	A^4

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A^5	A8	A^5
C1	0	A6	A^6	A10	A^6
D1	0	A7	A^7	A11	A^7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
E1	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A^8	B15	B^7
G3	0	A9	A^9	B12	B^6
G1	0	A10	A^10	B10	B^5
H1	0	A11	A^11	B8	B^4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC <sup>1</sup>	-	I <sup>1</sup>	-
K4	0	A12	A^12	B6	B^3
H4	0	A13	A^13	B4	B^2
H5	0	A14	A^14	B2	B^1

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
K5	0	A15	A^15	B0	B^0
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B^0	C0	C^0
K7	1	B1	B^1	C1	C^1
K8	1	B2	B^2	C2	C^2
K9	1	B3	B^3	C4	C^3
K10	1	B4	B^4	C6	C^4
J10	-	TMS	-	TMS	-
H8	1	B5	B^5	C8	C^5
H10	1	B6	B^6	C10	C^6
G10	1	B7	B^7	C11	C^7
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
F10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B^8	D15	D^7
D8	1	B9	B^9	D12	D^6
D10	1	B10	B^10	D10	D^5
C10	1	B11	B^11	D8	D^4
B10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A7	1	B12	B^12	D6	D^3
C7	1	B13	B^13	D4	D^2
C6	1	B14	B^14	D2	D^1
A6	1	B15/GOE1	B^15	D0/GOE1	D^0
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A^0	A0/GOE0	A^0
A4	0	A1	A^1	A1	A^1
A3	0	A2	A^2	A2	A^2
A2	0	A3	A^3	A4	A^3
A1	0	A4	A^4	A6	A^4

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3	P12	P^3
85	1	D2	D^2	H4	H^2	P10	P^2
86	1	D1	D^1	H2	H^1	P6	P^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	P^0
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^0
92	0	A1	A^1	A2	A^1	A6	A^1
93	0	A2	A^2	A4	A^2	A10	A^2
94	0	A3	A^3	A6	A^3	A12	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4	B2	B^0
98	0	A5	A^5	A10	A^5	B6	B^1
99	0	A6	A^6	A12	A^6	B10	B^2
100	0	A7	A^7	A14	A^7	B12	B^3

\*This pin is input only.

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

## ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C <sup>1</sup>	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C <sup>1</sup>	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C <sup>1</sup>	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

## ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4064C	LC4064C-25TN100C	64	1.8	2.5	Lead-free TQFP	100	64	C
	LC4064C-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064C-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064C-25TN48C	64	1.8	2.5	Lead-free TQFP	48	32	C
	LC4064C-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064C-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
	LC4064C-25TN44C	64	1.8	2.5	Lead-free TQFP	44	30	C
	LC4064C-5TN44C	64	1.8	5	Lead-free TQFP	44	30	C
	LC4064C-75TN44C	64	1.8	7.5	Lead-free TQFP	44	30	C
LC4128C	LC4128C-27TN128C	128	1.8	2.7	Lead-free TQFP	128	92	C
	LC4128C-5TN128C	128	1.8	5	Lead-free TQFP	128	92	C
	LC4128C-75TN128C	128	1.8	7.5	Lead-free TQFP	128	92	C
	LC4128C-27TN100C	128	1.8	2.7	Lead-free TQFP	100	64	C
	LC4128C-5TN100C	128	1.8	5	Lead-free TQFP	100	64	C
	LC4128C-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256C	LC4256C-3FTN256AC	256	1.8	3	Lead-free ftBGA	256	128	C
	LC4256C-5FTN256AC	256	1.8	5	Lead-free ftBGA	256	128	C
	LC4256C-75FTN256AC	256	1.8	7.5	Lead-free ftBGA	256	128	C
	LC4256C-3FTN256BC	256	1.8	3	Lead-free ftBGA	256	160	C
	LC4256C-5FTN256BC	256	1.8	5	Lead-free ftBGA	256	160	C
	LC4256C-75FTN256BC	256	1.8	7.5	Lead-free ftBGA	256	160	C
	LC4256C-3FN256AC <sup>1</sup>	256	1.8	3	Lead-free fpBGA	256	128	C
	LC4256C-5FN256AC <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	128	C
	LC4256C-75FN256AC <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	128	C
	LC4256C-3FN256BC <sup>1</sup>	256	1.8	3	Lead-free fpBGA	256	160	C
	LC4256C-5FN256BC <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	160	C
	LC4256C-75FN256BC <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	160	C
	LC4256C-3TN176C	256	1.8	3	Lead-free TQFP	176	128	C
	LC4256C-5TN176C	256	1.8	5	Lead-free TQFP	176	128	C
	LC4256C-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256C-3TN100C	256	1.8	3	Lead-free TQFP	100	64	C
	LC4256C-5TN100C	256	1.8	5	Lead-free TQFP	100	64	C
	LC4256C-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C
LC4384C	LC4384C-35FTN256C	384	1.8	3.5	Lead-free ftBGA	256	192	C
	LC4384C-5FTN256C	384	1.8	5	Lead-free ftBGA	256	192	C
	LC4384C-75FTN256C	384	1.8	7.5	Lead-free ftBGA	256	192	C
	LC4384C-35FN256C <sup>1</sup>	384	1.8	3.5	Lead-free fpBGA	256	192	C
	LC4384C-5FN256C <sup>1</sup>	384	1.8	5	Lead-free fpBGA	256	192	C
	LC4384C-75FN256C <sup>1</sup>	384	1.8	7.5	Lead-free fpBGA	256	192	C
	LC4384C-35TN176C	384	1.8	3.5	Lead-free TQFP	176	128	C
	LC4384C-5TN176C	384	1.8	5	Lead-free TQFP	176	128	C
	LC4384C-75TN176C	384	1.8	7.5	Lead-free TQFP	176	128	C

## ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI <sup>1</sup>	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI <sup>1</sup>	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I <sup>1</sup>	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I <sup>1</sup>	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I <sup>1</sup>	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I <sup>1</sup>	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I <sup>1</sup>	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I <sup>1</sup>	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
	LC4064B-75TN44C	64	2.5	7.5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC <sup>1</sup>	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC <sup>1</sup>	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
	LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C
	LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I