# Lattice Semiconductor Corporation - LC4256B-75FT256BI Datasheet



**Welcome to E-XFL.COM**

## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 2.3V ~ 2.7V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 160 |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-75ft256bi |

*Table 2. ispMACH 4000Z Family Selection Guide*

| | ispMACH 4032ZC | ispMACH 4064ZC | ispMACH 4128ZC | ispMACH 4256ZC |
|---|---|---|---|---|
| Macrocells | 32 | 64 | 128 | 256 |
| I/O + Dedicated Inputs | 32+4/32+4 | 32+4/32+12/ 64+10/64+10 | 64+10/96+4 | 64+10/96+6/ 128+4 |
| $t_{PD}$ (ns) | 3.5 | 3.7 | 4.2 | 4.5 |
| $t_S$ (ns) | 2.2 | 2.5 | 2.7 | 2.9 |
| $t_{CO}$ (ns) | 3.0 | 3.2 | 3.5 | 3.8 |
| $f_{MAX}$ (MHz) | 267 | 250 | 220 | 200 |
| Supply Voltage (V) | 1.8 | 1.8 | 1.8 | 1.8 |
| Max. Standby Icc (µA) | 20 | 25 | 35 | 55 |
| Pins/Package | 48 TQFP<br>56 csBGA | 48 TQFP<br>56 csBGA<br>100 TQFP<br>132 csBGA | 100 TQFP<br>132csBGA | 100 TQFP<br>132 csBGA<br>176 TQFP |

## ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

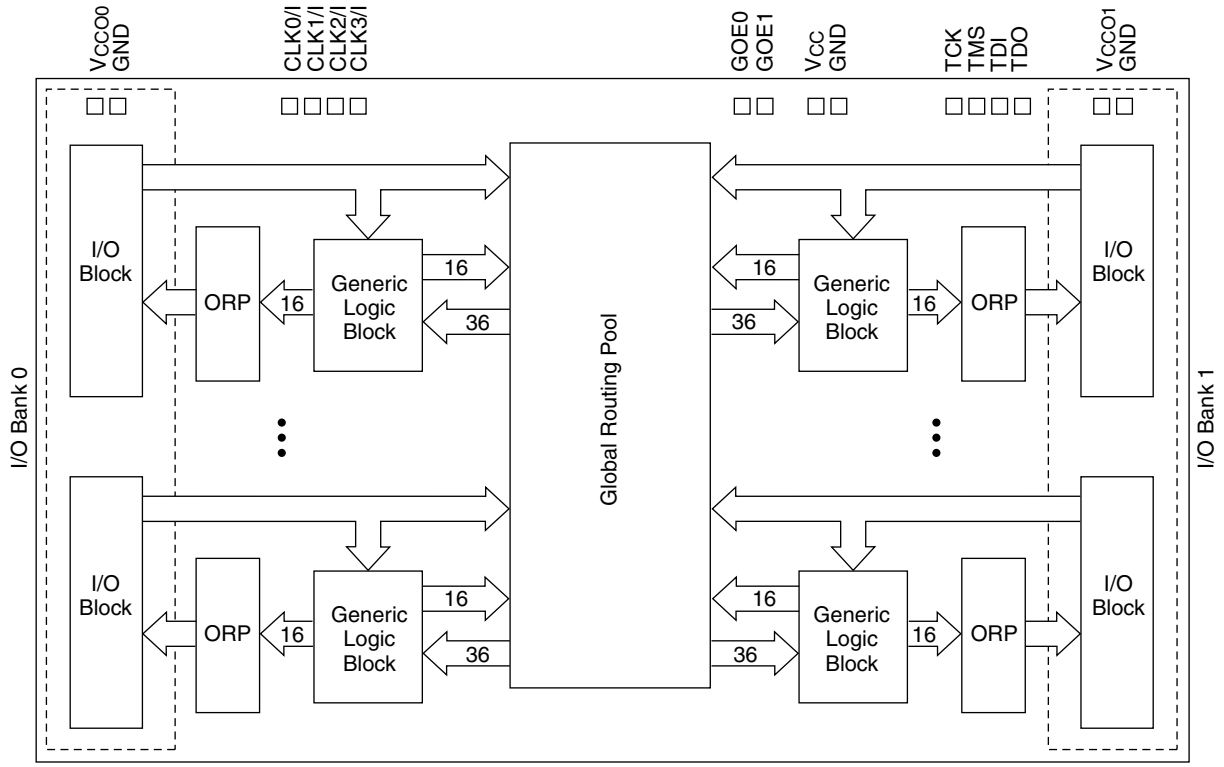
The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to $V_{CC}$ (logic core).

## Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

***Figure 1. Functional Block Diagram***




The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to $V_{CCO}$ of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

## ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

### Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

*Table 5. Product Term Expansion Capability*

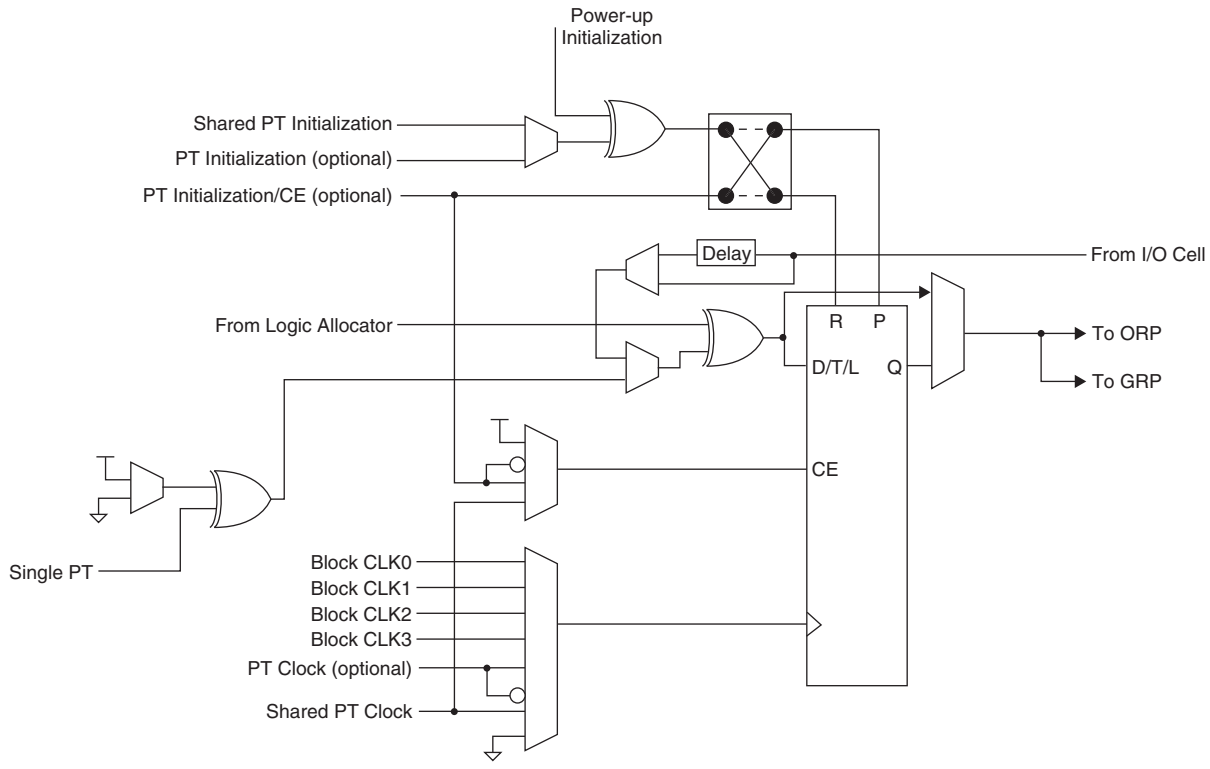
| Expansion Chains | Macrocells Associated with Expansion Chain (with Wrap Around) | Max PT/ Macrocell |
|---|---|---|
| Chain-0 | M0 M4 M8 M12 M0 | 75 |
| Chain-1 | M1 M5 M9 M13 M1 | 80 |
| Chain-2 | M2 M6 M10 M14 M2 | 75 |
| Chain-3 | M3 M7 M11 M15 M3 | 70 |

Every time the super cluster allocator is used, there is an incremental delay of $t_{EXP}$. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

## Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

*Figure 5. Macrocell*




## Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

## Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

## Initialization Control

The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the $V_{CC}$ rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

## GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

***Figure 6. GLB Clock Generator***

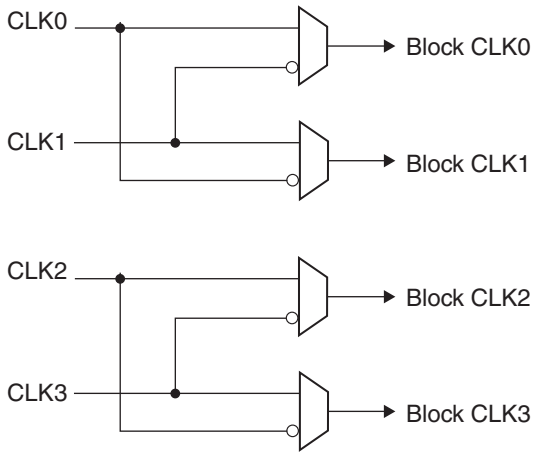


*Table 7. ORP Combinations for I/O Blocks with 16 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M1, M2, M3, M4, M5, M6, M7, M8 |
| I/O 2 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 3 | M3, M4, M5, M6, M7, M8, M9, M10 |
| I/O 4 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 5 | M5, M6, M7, M8, M9, M10, M11, M12 |
| I/O 6 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 7 | M7, M8, M9, M10, M11, M12, M13, M14 |
| I/O 8 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 9 | M9, M10, M11, M12, M13, M14, M15, M0 |
| I/O 10 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 11 | M11, M12, M13, M14, M15, M0, M1, M2 |
| I/O 12 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 13 | M13, M14, M15, M0, M1, M2, M3, M4 |
| I/O 14 | M14, M15, M0, M1, M2, M3, M4, M5 |
| I/O 15 | M15, M0, M1, M2, M3, M4, M5, M6 |

*Table 8. ORP Combinations for I/O Blocks with 4 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 2 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 3 | M12, M13, M14, M15, M0, M1, M2, M3 |

*Table 9. ORP Combinations for I/O Blocks with 10 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 2 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 3 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 4 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 5 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 6 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 7 | M14, M15, M0, M1, M2, M3, M4, M5 |
| I/O 8 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 9 | M10, M11, M12, M13, M14, M15, M0, M1 |

*Table 10. ORP Combinations for I/O Blocks with 12 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M1, M2, M3, M4, M5, M6, M7, M8 |
| I/O 2 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 3 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 4 | M5, M6, M7, M8, M9, M10, M11, M12 |
| I/O 5 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 6 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 7 | M9, M10, M11, M12, M13, M14, M15, M0 |
| I/O 8 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 9 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 10 | M13, M14, M15, M0, M1, M2, M3, M4 |
| I/O 11 | M14, M15, M0, M1, M2, M3, M4, M5 |

### ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster $t_{CO}$.

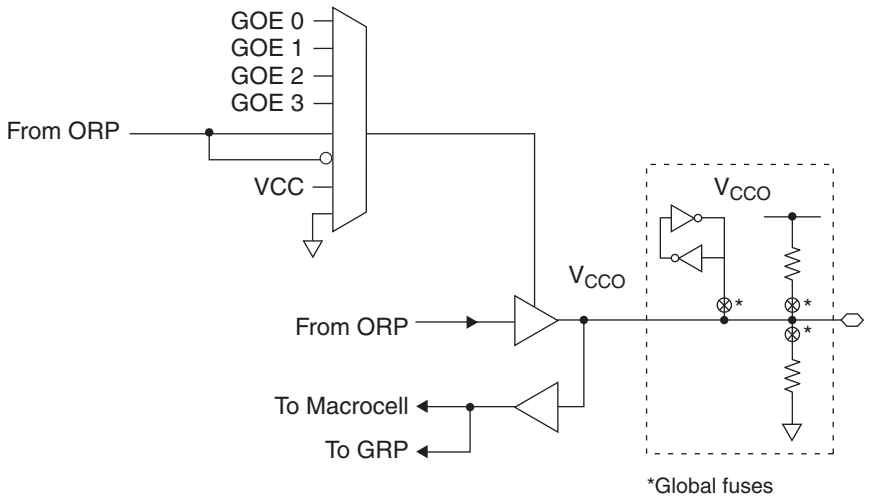
### Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

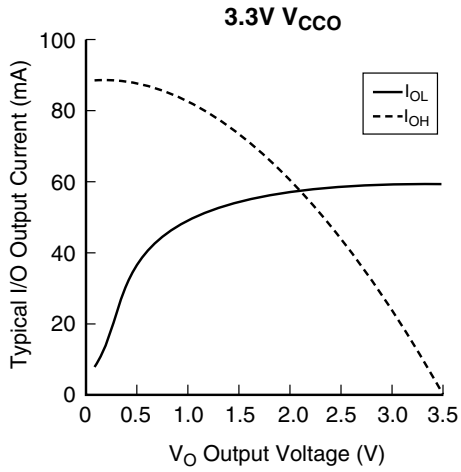
## I/O Cell

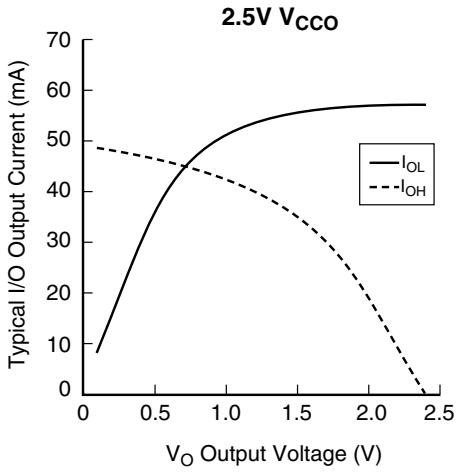
The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

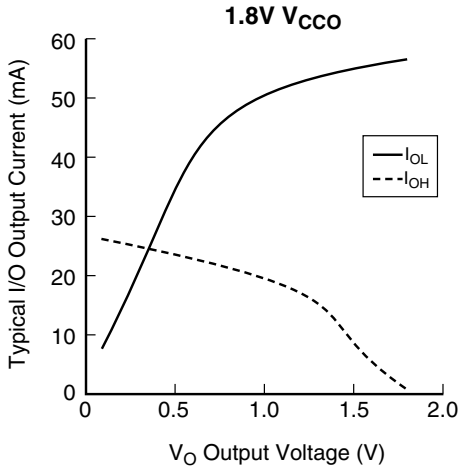
*Figure 8. I/O Cell*




Each output supports a variety of output standards dependent on the $V_{CCO}$ supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the $V_{CCO}$ supplied to its I/O bank. The I/O standards supported are:


3.3V $V_{CCO}$
Typical I/O Output Current (mA)
100
80
60
40
20
0
0 0.5 1.0 1.5 2.0 2.5 3.0 3.5
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$


2.5V $V_{CCO}$
Typical I/O Output Current (mA)
70
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0 2.5
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$


1.8V $V_{CCO}$
Typical I/O Output Current (mA)
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$

# ispMACH 4000Z External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 3.5 | — | 3.7 | — | 4.2 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 4.4 | — | 4.7 | — | 5.7 | ns |
| $t_S$ | GLB register setup time before clock | 2.2 | — | 2.5 | — | 2.7 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 2.4 | — | 2.7 | — | 2.9 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.0 | — | 1.1 | — | 1.3 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.0 | — | 2.1 | — | 2.6 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.0 | — | 1.0 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.0 | — | 3.2 | — | 3.5 | ns |
| $t_R$ | External reset pin to output delay | — | 5.0 | — | 6.0 | — | 7.3 | ns |
| $t_{RW}$ | External reset pulse duration | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 7.0 | — | 8.0 | — | 8.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 6.5 | — | 7.0 | — | 8.0 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 4.5 | — | 4.5 | — | 4.8 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 267 | — | 250 | — | 220 | MHz |
| $f_{MAX}$ (Ext.) | clock frequency with external feedback, $[1 / (t_S + t_{CO})]$ | — | 192 | — | 175 | — | 161 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

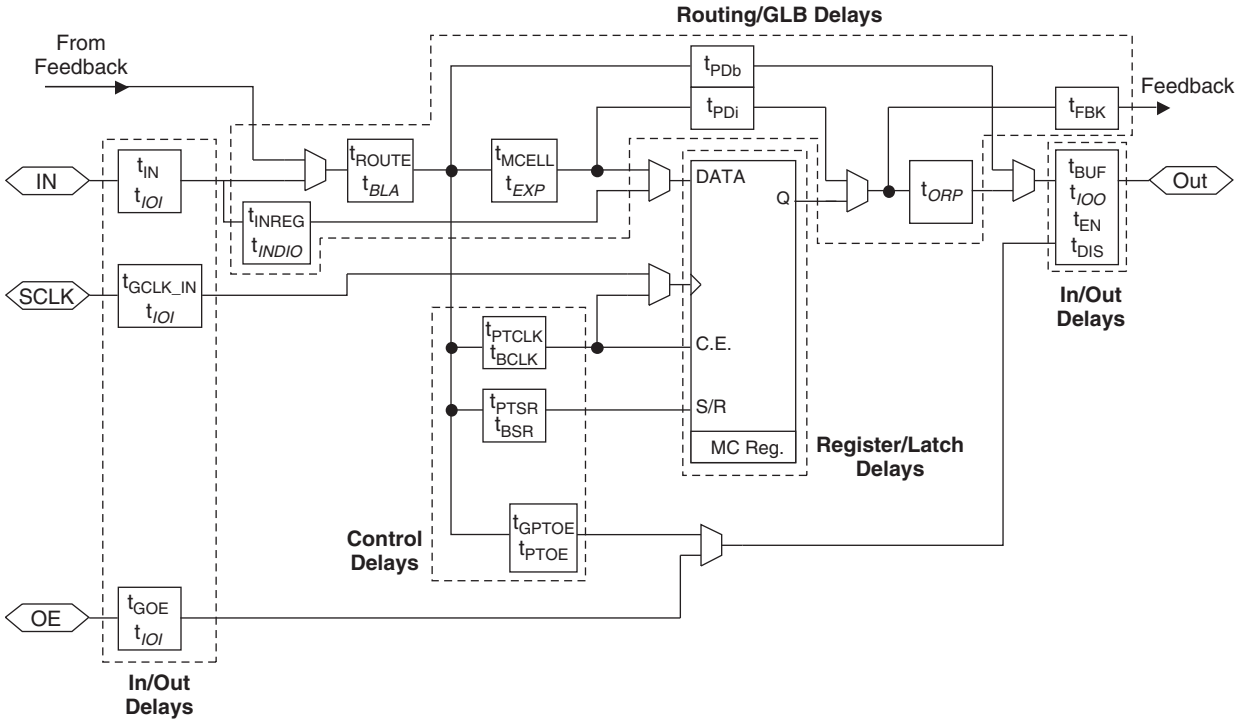
Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

## Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

***Figure 11. ispMACH 4000 Timing Model***




Note: Italicized items are optional delay adders.

# ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -2.5 | | -2.7 | | -3 | | -3.5 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | 0.28 | — | 0.28 | — | 0.28 | — | 0.28 | — | ns |
| $t_{SRR}$ | Asynchronous Reset or Set Recovery Time | 1.67 | — | 1.67 | — | 1.67 | — | 1.67 | — | ns |
| **Control Delays** | | | | | | | | | | |
| $t_{BCLK}$ | GLB PT Clock Delay | — | 1.12 | — | 1.12 | — | 1.12 | — | 1.12 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | — | 0.87 | — | 0.87 | — | 0.87 | — | 0.87 | ns |
| $t_{BSR}$ | Block PT Set/Reset Delay | — | 1.83 | — | 1.83 | — | 1.83 | — | 1.83 | ns |
| $t_{PTSR}$ | Macrocell PT Set/Reset Delay | — | 1.11 | — | 1.41 | — | 1.51 | — | 1.61 | ns |
| $t_{GPTOE}$ | Global PT OE Delay | — | 2.83 | — | 4.13 | — | 5.33 | — | 5.33 | ns |
| $t_{PTOE}$ | Macrocell PT OE Delay | — | 1.83 | — | 2.13 | — | 2.33 | — | 2.83 | ns |

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

# ispMACH 4000Z Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -45 | | -5 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PTOE}$ | Macrocell PT OE Delay | — | 2.50 | — | 2.70 | — | 2.00 | ns |

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

## ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP

| Pin Number | Bank Number | ispMACH 4032V/B/C | | ispMACH 4064V/B/C | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 1 | - | TDI | - | TDI | - |
| 2 | 0 | A5 | A^5 | A10 | A^5 |
| 3 | 0 | A6 | A^6 | A12 | A^6 |
| 4 | 0 | A7 | A^7 | A14 | A^7 |
| 5 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 6 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 7 | 0 | A8 | A^8 | B0 | B^0 |
| 8 | 0 | A9 | A^9 | B2 | B^1 |
| 9 | 0 | A10 | A^10 | B4 | B^2 |
| 10 | - | TCK | - | TCK | - |
| 11 | - | VCC | - | VCC | - |
| 12 | - | GND | - | GND | - |
| 13 | 0 | A12 | A^12 | B8 | B^4 |
| 14 | 0 | A13 | A^13 | B10 | B^5 |
| 15 | 0 | A14 | A^14 | B12 | B^6 |
| 16 | 0 | A15 | A^15 | B14 | B^7 |
| 17 | 1 | CLK2/I | - | CLK2/I | - |
| 18 | 1 | B0 | B^0 | C0 | C^0 |
| 19 | 1 | B1 | B^1 | C2 | C^1 |
| 20 | 1 | B2 | B^2 | C4 | C^2 |
| 21 | 1 | B3 | B^3 | C6 | C^3 |
| 22 | 1 | B4 | B^4 | C8 | C^4 |
| 23 | - | TMS | - | TMS | - |
| 24 | 1 | B5 | B^5 | C10 | C^5 |
| 25 | 1 | B6 | B^6 | C12 | C^6 |
| 26 | 1 | B7 | B^7 | C14 | C^7 |
| 27 | 1 | GND (Bank 1) | - | GND (Bank 1) | - |
| 28 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 29 | 1 | B8 | B^8 | D0 | D^0 |
| 30 | 1 | B9 | B^9 | D2 | D^1 |
| 31 | 1 | B10 | B^10 | D4 | D^2 |
| 32 | - | TDO | - | TDO | - |
| 33 | - | VCC | - | VCC | - |
| 34 | - | GND | - | GND | - |
| 35 | 1 | B12 | B^12 | D8 | D^4 |
| 36 | 1 | B13 | B^13 | D10 | D^5 |
| 37 | 1 | B14 | B^14 | D12 | D^6 |
| 38 | 1 | B15/GOE1 | B^15 | D14/GOE1 | D^7 |
| 39 | 0 | CLK0/I | - | CLK0/I | - |
| 40 | 0 | A0/GOE0 | A^0 | A0/GOE0 | A^0 |
| 41 | 0 | A1 | A^1 | A2 | A^1 |

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 105 | 1 | VCCO (Bank 1) | - |
| 106 | 1 | H6 | H^5 |
| 107 | 1 | H5 | H^4 |
| 108 | 1 | H4 | H^3 |
| 109 | 1 | H2 | H^2 |
| 110 | 1 | H1 | H^1 |
| 111 | 1 | H0/GOE1 | H^0 |
| 112 | 1 | CLK3/I | - |
| 113 | 0 | GND (Bank 0) | - |
| 114 | 0 | CLK0/I | - |
| 115 | 0 | VCC | - |
| 116 | 0 | A0/GOE0 | A^0 |
| 117 | 0 | A1 | A^1 |
| 118 | 0 | A2 | A^2 |
| 119 | 0 | A4 | A^3 |
| 120 | 0 | A5 | A^4 |
| 121 | 0 | A6 | A^5 |
| 122 | 0 | VCCO (Bank 0) | - |
| 123 | 0 | GND (Bank 0) | - |
| 124 | 0 | A8 | A^6 |
| 125 | 0 | A9 | A^7 |
| 126 | 0 | A10 | A^8 |
| 127 | 0 | A12 | A^9 |
| 128 | 0 | A14 | A^11 |

## ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA

| Ball Number | Bank Number | ispMACH 4064Z | | ispMACH 4128Z | | ispMACH 4256Z | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| B1 | - | GND | - | GND | - | GND | - |
| B2 | - | TDI | - | TDI | - | TDI | - |
| C1 | 0 | NC | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| C3 | 0 | NC | - | B0 | B^0 | C12 | C^6 |
| C2 | 0 | A8 | A^8 | B1 | B^1 | C10 | C^5 |
| D1 | 0 | A9 | A^9 | B2 | B^2 | C8 | C^4 |
| D3 | 0 | A10 | A^10 | B4 | B^3 | C6 | C^3 |
| D2 | 0 | A11 | A^11 | B5 | B^4 | C4 | C^2 |
| E1 | 0 | NC | | B6 | B^5 | C2 | C^1 |
| E2 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |

## ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

| | | ispMACH 4064Z | | ispMACH 4128Z | | ispMACH 4256Z | |
|---|---|---|---|---|---|---|---|
| Ball Number | Bank Number | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| P8 | 1 | NC[1] | - | NC[1] | - | I[1] | - |
| M8 | 1 | NC | - | E0 | E^0 | I2 | I^1 |
| P9 | 1 | C0 | C^0 | E1 | E^1 | I4 | I^2 |
| N9 | 1 | C1 | C^1 | E2 | E^2 | I6 | I^3 |
| M9 | 1 | C2 | C^2 | E4 | E^3 | I8 | I^4 |
| N10 | 1 | C3 | C^3 | E5 | E^4 | I10 | I^5 |
| P10 | 1 | NC | - | E6 | E^5 | I12 | I^6 |
| M10 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| N11 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| P11 | 1 | NC | - | E8 | E^6 | J2 | J^1 |
| M11 | 1 | C4 | C^4 | E9 | E^7 | J4 | J^2 |
| P12 | 1 | C5 | C^5 | E10 | E^8 | J6 | J^3 |
| N12 | 1 | C6 | C^6 | E12 | E^9 | J8 | J^4 |
| P13 | 1 | C7 | C^7 | E13 | E^10 | J10 | J^5 |
| P14 | 1 | NC | - | E14 | E^11 | J12 | J^6 |
| N14 | - | GND | - | GND | - | GND | - |
| N13 | - | TMS | - | TMS | - | TMS | - |
| M14 | 1 | NC | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| M12 | 1 | NC | - | F0 | F^0 | K12 | K^6 |
| M13 | 1 | C8 | C^8 | F1 | F^1 | K10 | K^5 |
| L14 | 1 | C9 | C^9 | F2 | F^2 | K8 | K^4 |
| L12 | 1 | C10 | C^10 | F4 | F^3 | K6 | K^3 |
| L13 | 1 | C11 | C^11 | F5 | F^4 | K4 | K^2 |
| K14 | 1 | NC | - | F6 | F^5 | K2 | K^1 |
| K13 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| K12 | 1 | NC | - | F8 | F^6 | L12 | L^6 |
| J13 | 1 | C12 | C^12 | F9 | F^7 | L10 | L^5 |
| J14 | 1 | C13 | C^13 | F10 | F^8 | L8 | L^4 |
| J12 | 1 | C14 | C^14 | F12 | F^9 | L6 | L^3 |
| H14 | 1 | C15 | C^15 | F13 | F^10 | L4 | L^2 |
| H13 | 1 | I | - | F14 | F^11 | L2 | L^1 |
| H12 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| G13 | 1 | NC | - | G14 | G^11 | M2 | M^1 |
| G14 | 1 | NC | - | G13 | G^10 | M4 | M^2 |
| G12 | 1 | D15 | D^15 | G12 | G^9 | M6 | M^3 |
| F14 | 1 | D14 | D^14 | G10 | G^8 | M8 | M^4 |
| F13 | 1 | D13 | D^13 | G9 | G^7 | M10 | M^5 |
| F12 | 1 | D12 | D^12 | G8 | G^6 | M12 | M^6 |
| E13 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| E14 | 1 | NC | - | G6 | G^5 | N2 | N^1 |
| E12 | 1 | D11 | D^11 | G5 | G^4 | N4 | N^2 |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| J6 | 0 | E14 | E^7 | E10 | E^7 | H14 | H^7 | J14 | J^7 |
| K3 | 0 | NC | - | E12 | E^8 | G0 | G^0 | I0 | I^0 |
| K4 | 0 | NC | - | E14 | E^9 | G2 | G^1 | I4 | I^1 |
| L1 | 0 | NC | - | NC | - | I14 | I^7 | K0 | K^0 |
| L2 | 0 | NC | - | NC | - | I12 | I^6 | K2 | K^1 |
| M1 | 0 | NC | - | NC | - | NC | - | K4 | K^2 |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| - | 0 | - | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| M2 | 0 | NC | - | NC | - | NC | - | K6 | K^3 |
| N1 | 0 | NC | - | NC | - | I10 | I^5 | K8 | K^4 |
| M3 | 0 | NC | - | NC | - | I8 | I^4 | K10 | K^5 |
| M4 | 0 | NC | - | F0 | F^0 | G4 | G^2 | I8 | I^2 |
| N2 | 0 | NC | - | F1 | F^1 | G6 | G^3 | I12 | I^3 |
| K5 | 0 | F0 | F^0 | F2 | F^2 | J0 | J^0 | N0 | N^0 |
| P1 | 0 | F2 | F^1 | F4 | F^3 | J2 | J^1 | N2 | N^1 |
| K6 | 0 | F4 | F^2 | F6 | F^4 | J4 | J^2 | N4 | N^2 |
| N3 | 0 | F6 | F^3 | F8 | F^5 | J6 | J^3 | N6 | N^3 |
| L5 | 0 | F8 | F^4 | F9 | F^6 | J8 | J^4 | N8 | N^4 |
| P2 | 0 | F10 | F^5 | F10 | F^7 | J10 | J^5 | N10 | N^5 |
| L6 | 0 | F12 | F^6 | F12 | F^8 | J12 | J^6 | N12 | N^6 |
| R1 | 0 | F14 | F^7 | F14 | F^9 | J14 | J^7 | N14 | N^7 |
| - | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| P3 | - | TCK | - | TCK | - | TCK | - | TCK | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| - | - | GND | - | GND | - | GND | - | GND | - |
| - | 0 | - | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| T2 | 0 | NC | - | G14 | G^9 | I6 | I^3 | K12 | K^6 |
| M5 | 0 | NC | - | G12 | G^8 | I4 | I^2 | K14 | K^7 |
| N4 | 0 | G14 | G^7 | G10 | G^7 | K14 | K^7 | O14 | O^7 |
| T3 | 0 | G12 | G^6 | G9 | G^6 | K12 | K^6 | O12 | O^6 |
| R3 | 0 | G10 | G^5 | G8 | G^5 | K10 | K^5 | O10 | O^5 |
| M6 | 0 | G8 | G^4 | G6 | G^4 | K8 | K^4 | O8 | O^4 |
| P4 | 0 | G6 | G^3 | G4 | G^3 | K6 | K^3 | O6 | O^3 |
| L7 | 0 | G4 | G^2 | G2 | G^2 | K4 | K^2 | O4 | O^2 |
| N5 | 0 | G2 | G^1 | G1 | G^1 | K2 | K^1 | O2 | O^1 |
| M7 | 0 | G0 | G^0 | G0 | G^0 | K0 | K^0 | O0 | O^0 |
| P5 | 0 | NC | - | NC | - | G8 | G^4 | M0 | M^0 |
| R4 | 0 | NC | - | NC | - | G10 | G^5 | M4 | M^1 |
| T4 | 0 | NC | - | NC | - | NC | - | L0 | L^0 |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| - | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| C12 | 1 | O0 | O^0 | O2 | O^2 | GX0 | GX^0 | OX0 | OX^0 |
| E10 | 1 | NC | - | O1 | O^1 | CX8 | CX^4 | MX0 | MX^0 |
| A13 | 1 | NC | - | O0 | O^0 | CX10 | CX^5 | MX4 | MX^1 |
| D12 | 1 | NC | - | NC | - | NC | - | LX0 | LX^0 |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| - | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| B12 | 1 | NC | - | NC | - | NC | - | LX4 | LX^1 |
| A12 | 1 | NC | - | NC | - | EX2 | EX^1 | LX8 | LX^2 |
| B11 | 1 | NC | - | NC | - | EX0 | EX^0 | LX12 | LX^3 |
| A11 | 1 | NC | - | P14 | P^9 | CX12 | CX^6 | MX8 | MX^2 |
| D10 | 1 | NC | - | P12 | P^8 | CX14 | CX^7 | MX12 | MX^3 |
| C10 | 1 | P14 | P^7 | P10 | P^7 | HX14 | HX^7 | PX14 | PX^7 |
| B10 | 1 | P12 | P^6 | P9 | P6 | HX12 | HX^6 | PX12 | PX^6 |
| A10 | 1 | P10 | P^5 | P8 | P^5 | HX10 | HX^5 | PX10 | PX^5 |
| A9 | 1 | P8 | P^4 | P6 | P^4 | HX8 | HX^4 | PX8 | PX^4 |
| F9 | 1 | P6 | P^3 | P4 | P^3 | HX6 | HX^3 | PX6 | PX^3 |
| B9 | 1 | P4 | P^2 | P2 | P^2 | HX4 | HX^2 | PX4 | PX^2 |
| E9 | 1 | P2/GOE1 | P^1 | P1/GOE1 | P^1 | HX2/GOE1 | HX^1 | PX2/GOE1 | PX^1 |
| C9 | 1 | P0 | P^0 | P0 | P^0 | HX0 | HX^0 | PX0 | PX^0 |
| - | - | GND | - | GND | | GND | - | GND | - |
| D9 | 1 | CLK3/I | - | CLK3/I | - | CLK3/I | - | CLK3/I | - |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| B8 | 0 | CLK0/I | - | CLK0/I | - | CLK0/I | - | CLK0/I | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| D8 | 0 | A0 | A^0 | A0 | A^0 | A0 | A^0 | A0 | A^0 |
| C8 | 0 | A2/GOE0 | A^1 | A1/GOE0 | A^1 | A2/GOE0 | A^1 | A2/GOE0 | A^1 |
| A8 | 0 | A4 | A^2 | A2 | A^2 | A4 | A^2 | A4 | A^2 |
| A7 | 0 | A6 | A^3 | A4 | A^3 | A6 | A^3 | A6 | A^3 |
| B7 | 0 | A8 | A^4 | A6 | A^4 | A8 | A^4 | A8 | A^4 |
| E8 | 0 | A10 | A^5 | A8 | A^5 | A10 | A^5 | A10 | A^5 |
| D7 | 0 | A12 | A^6 | A9 | A^6 | A12 | A^6 | A12 | A^6 |
| F8 | 0 | A14 | A^7 | A10 | A^7 | A14 | A^7 | A14 | A^7 |
| C7 | 0 | NC | - | A12 | A^8 | F14 | F^7 | D0 | D^0 |
| A6 | 0 | NC | - | A14 | A^9 | F12 | F^6 | D4 | D^1 |
| B6 | 0 | NC | - | NC | - | D14 | D^7 | E0 | E^0 |
| A5 | 0 | NC | - | NC | - | D12 | D^6 | E4 | E^1 |
| B5 | 0 | NC | - | NC | - | NC | - | E8 | E^2 |
| - | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| D5 | 0 | NC | - | NC | - | NC | - | E12 | E^3 |
| A4 | 0 | NC | - | B0 | B^0 | F10 | F^5 | D8 | D^2 |

## Part Number Description

LC XXXX X X – XX XX XXX X X XX

**Device Family**

**Device Number**
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells
4384 = 384 Macrocells
4512 = 512 Macrocells

**Power**
Z = Zero Power
Blank = Low Power

**Supply Voltage**
V = 3.3V
B = 2.5V
C = 1.8V

**Speed**
25 = 2.5ns
27 = 2.7ns
3 = 3.0ns
35 = 3.5ns
37 = 3.7ns
42 = 4.2ns
45 = 4.5ns
5 = 5.0ns
75 = 7.5ns
10 = 10.0ns

**Package**

| | |
|---|---|
| T = TQFP | TN = Lead-free TQFP |
| FT = ftBGA | FTN= Lead-free ftBGA |
| F = fpBGA[2] | FN = Lead-free fpBGA[2] |
| M = csBGA | MN = Lead-free csBGA |

**Pin/Ball Count**
44 (1.0mm thickness)
48 (1.0mm thickness)
56
100
128
132
144
176
256

**I/O Designator (if applicable)**
A = 128 I/Os
B = 160 I/Os

**Operating Temperature Range**
C = Commercial
I = Industrial
E = Extended[1]

**Production Status**
Blank = Final production
ES = Engineering Samples

1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000 Family Speed Grade Offering

| | -25 | -27 | -3 | -35 | -37 | -42 | -45 | -5 | | -75 | | | -10 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Com | Com | Com | Com | Com | Com | Com | Com | Ind | Com | Ind | Ext | Ind |
| ispMACH 4032V/B/C | | | | | | | | | | | | 1 | |
| ispMACH 4064V/B/C | | | | | | | | | | | | 1 | |
| ispMACH 4128V/B/C | | | | | | | | | | | | 1 | |
| ispMACH 4256V/B/C | | | | | | | | | | | | | |
| ispMACH 4384V/B/C | | | | | | | | | | | | | |
| ispMACH 4512V/B/C | | | | | | | | | | | | | |
| ispMACH 4032ZC | | | | | | | | | | | | 1 | |
| ispMACH 4064ZC | | | | | | | | | | | | 1 | |
| ispMACH 4128ZC | | | | | | | | | | | | 1 | |
| ispMACH 4256ZC | | | | | | | | | | | | | |

1. 3.3V only.

**ispMACH 4000C (1.8V) Industrial Devices**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032C | LC4032C-5T48I | 32 | 1.8 | 5 | TQFP | 48 | 32 | I |
| | LC4032C-75T48I | 32 | 1.8 | 7.5 | TQFP | 48 | 32 | I |
| | LC4032C-10T48I | 32 | 1.8 | 10 | TQFP | 48 | 32 | I |
| | LC4032C-5T44I | 32 | 1.8 | 5 | TQFP | 44 | 30 | I |
| | LC4032C-75T44I | 32 | 1.8 | 7.5 | TQFP | 44 | 30 | I |
| | LC4032C-10T44I | 32 | 1.8 | 10 | TQFP | 44 | 30 | I |
| LC4064C | LC4064C-5T100I | 64 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4064C-75T100I | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4064C-10T100I | 64 | 1.8 | 10 | TQFP | 100 | 64 | I |
| | LC4064C-5T48I | 64 | 1.8 | 5 | TQFP | 48 | 32 | I |
| | LC4064C-75T48I | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | I |
| | LC4064C-10T48I | 64 | 1.8 | 10 | TQFP | 48 | 32 | I |
| | LC4064C-5T44I | 64 | 1.8 | 5 | TQFP | 44 | 30 | I |
| | LC4064C-75T44I | 64 | 1.8 | 7.5 | TQFP | 44 | 30 | I |
| | LC4064C-10T44I | 64 | 1.8 | 10 | TQFP | 44 | 30 | I |
| LC4128C | LC4128C-5T128I | 128 | 1.8 | 5 | TQFP | 128 | 92 | I |
| | LC4128C-75T128I | 128 | 1.8 | 7.5 | TQFP | 128 | 92 | I |
| | LC4128C-10T128I | 128 | 1.8 | 10 | TQFP | 128 | 92 | I |
| | LC4128C-5T100I | 128 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4128C-75T100I | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4128C-10T100I | 128 | 1.8 | 10 | TQFP | 100 | 64 | I |
| LC4256C | LC4256C-5FT256AI | 256 | 1.8 | 5 | ftBGA | 256 | 128 | I |
| | LC4256C-75FT256AI | 256 | 1.8 | 7.5 | ftBGA | 256 | 128 | I |
| | LC4256C-10FT256AI | 256 | 1.8 | 10 | ftBGA | 256 | 128 | I |
| | LC4256C-5FT256BI | 256 | 1.8 | 5 | ftBGA | 256 | 160 | I |
| | LC4256C-75FT256BI | 256 | 1.8 | 7.5 | ftBGA | 256 | 160 | I |
| | LC4256C-10FT256BI | 256 | 1.8 | 10 | ftBGA | 256 | 160 | I |
| | LC4256C-5F256AI[1] | 256 | 1.8 | 5 | fpBGA | 256 | 128 | I |
| | LC4256C-75F256AI[1] | 256 | 1.8 | 7.5 | fpBGA | 256 | 128 | I |
| | LC4256C-10F256AI[1] | 256 | 1.8 | 10 | fpBGA | 256 | 128 | I |
| | LC4256C-5F256BI[1] | 256 | 1.8 | 5 | fpBGA | 256 | 160 | I |
| | LC4256C-75F256BI[1] | 256 | 1.8 | 7.5 | fpBGA | 256 | 160 | I |
| | LC4256C-10F256BI[1] | 256 | 1.8 | 10 | fpBGA | 256 | 160 | I |
| | LC4256C-5T176I | 256 | 1.8 | 5 | TQFP | 176 | 128 | I |
| | LC4256C-75T176I | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4256C-10T176I | 256 | 1.8 | 10 | TQFP | 176 | 128 | I |
| | LC4256C-5T100I | 256 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4256C-75T100I | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4256C-10T100I | 256 | 1.8 | 10 | TQFP | 100 | 64 | I |

**ispMACH 4000V (3.3V) Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4512V | LC4512V-35FT256C | 512 | 3.3 | 3.5 | ftBGA | 256 | 208 | C |
| | LC4512V-5FT256C | 512 | 3.3 | 5 | ftBGA | 256 | 208 | C |
| | LC4512V-75FT256C | 512 | 3.3 | 7.5 | ftBGA | 256 | 208 | C |
| | LC4512V-35F256C[1] | 512 | 3.3 | 3.5 | fpBGA | 256 | 208 | C |
| | LC4512V-5F256C[1] | 512 | 3.3 | 5 | fpBGA | 256 | 208 | C |
| | LC4512V-75F256C[1] | 512 | 3.3 | 7.5 | fpBGA | 256 | 208 | C |
| | LC4512V-35T176C | 512 | 3.3 | 3.5 | TQFP | 176 | 128 | C |
| | LC4512V-5T176C | 512 | 3.3 | 5 | TQFP | 176 | 128 | C |
| | LC4512V-75T176C | 512 | 3.3 | 7.5 | TQFP | 176 | 128 | C |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000V (3.3V) Industrial Devices**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032V | LC4032V-5T48I | 32 | 3.3 | 5 | TQFP | 48 | 32 | I |
| | LC4032V-75T48I | 32 | 3.3 | 7.5 | TQFP | 48 | 32 | I |
| | LC4032V-10T48I | 32 | 3.3 | 10 | TQFP | 48 | 32 | I |
| | LC4032V-5T44I | 32 | 3.3 | 5 | TQFP | 44 | 30 | I |
| | LC4032V-75T44I | 32 | 3.3 | 7.5 | TQFP | 44 | 30 | I |
| | LC4032V-10T44I | 32 | 3.3 | 10 | TQFP | 44 | 30 | I |
| LC4064V | LC4064V-5T100I | 64 | 3.3 | 5 | TQFP | 100 | 64 | I |
| | LC4064V-75T100I | 64 | 3.3 | 7.5 | TQFP | 100 | 64 | I |
| | LC4064V-10T100I | 64 | 3.3 | 10 | TQFP | 100 | 64 | I |
| | LC4064V-5T48I | 64 | 3.3 | 5 | TQFP | 48 | 32 | I |
| | LC4064V-75T48I | 64 | 3.3 | 7.5 | TQFP | 48 | 32 | I |
| | LC4064V-10T48I | 64 | 3.3 | 10 | TQFP | 48 | 32 | I |
| | LC4064V-5T44I | 64 | 3.3 | 5 | TQFP | 44 | 30 | I |
| | LC4064V-75T44I | 64 | 3.3 | 7.5 | TQFP | 44 | 30 | I |
| | LC4064V-10T44I | 64 | 3.3 | 10 | TQFP | 44 | 30 | I |
| LC4128V | LC4128V-5T144I | 128 | 3.3 | 5 | TQFP | 144 | 96 | I |
| | LC4128V-75T144I | 128 | 3.3 | 7.5 | TQFP | 144 | 96 | I |
| | LC4128V-10T144I | 128 | 3.3 | 10 | TQFP | 144 | 96 | I |
| | LC4128V-5T128I | 128 | 3.3 | 5 | TQFP | 128 | 92 | I |
| | LC4128V-75T128I | 128 | 3.3 | 7.5 | TQFP | 128 | 92 | I |
| | LC4128V-10T128I | 128 | 3.3 | 10 | TQFP | 128 | 92 | I |
| | LC4128V-5T100I | 128 | 3.3 | 5 | TQFP | 100 | 64 | I |
| | LC4128V-75T100I | 128 | 3.3 | 7.5 | TQFP | 100 | 64 | I |
| | LC4128V-10T100I | 128 | 3.3 | 10 | TQFP | 100 | 64 | I |

**ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4064C | LC4064C-25TN100C | 64 | 1.8 | 2.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064C-5TN100C | 64 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064C-75TN100C | 64 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064C-25TN48C | 64 | 1.8 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064C-5TN48C | 64 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064C-75TN48C | 64 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064C-25TN44C | 64 | 1.8 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064C-5TN44C | 64 | 1.8 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064C-75TN44C | 64 | 1.8 | 7.5 | Lead-free TQFP | 44 | 30 | C |
| LC4128C | LC4128C-27TN128C | 128 | 1.8 | 2.7 | Lead-free TQFP | 128 | 92 | C |
| | LC4128C-5TN128C | 128 | 1.8 | 5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128C-75TN128C | 128 | 1.8 | 7.5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128C-27TN100C | 128 | 1.8 | 2.7 | Lead-free TQFP | 100 | 64 | C |
| | LC4128C-5TN100C | 128 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4128C-75TN100C | 128 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| LC4256C | LC4256C-3FTN256AC | 256 | 1.8 | 3 | Lead-free ftBGA | 256 | 128 | C |
| | LC4256C-5FTN256AC | 256 | 1.8 | 5 | Lead-free ftBGA | 256 | 128 | C |
| | LC4256C-75FTN256AC | 256 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 128 | C |
| | LC4256C-3FTN256BC | 256 | 1.8 | 3 | Lead-free ftBGA | 256 | 160 | C |
| | LC4256C-5FTN256BC | 256 | 1.8 | 5 | Lead-free ftBGA | 256 | 160 | C |
| | LC4256C-75FTN256BC | 256 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 160 | C |
| | LC4256C-3FN256AC[1] | 256 | 1.8 | 3 | Lead-free fpBGA | 256 | 128 | C |
| | LC4256C-5FN256AC[1] | 256 | 1.8 | 5 | Lead-free fpBGA | 256 | 128 | C |
| | LC4256C-75FN256AC[1] | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 128 | C |
| | LC4256C-3FN256BC[1] | 256 | 1.8 | 3 | Lead-free fpBGA | 256 | 160 | C |
| | LC4256C-5FN256BC[1] | 256 | 1.8 | 5 | Lead-free fpBGA | 256 | 160 | C |
| | LC4256C-75FN256BC[1] | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 160 | C |
| | LC4256C-3TN176C | 256 | 1.8 | 3 | Lead-free TQFP | 176 | 128 | C |
| | LC4256C-5TN176C | 256 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | C |
| | LC4256C-75TN176C | 256 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | C |
| | LC4256C-3TN100C | 256 | 1.8 | 3 | Lead-free TQFP | 100 | 64 | C |
| | LC4256C-5TN100C | 256 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4256C-75TN100C | 256 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| LC4384C | LC4384C-35FTN256C | 384 | 1.8 | 3.5 | Lead-free ftBGA | 256 | 192 | C |
| | LC4384C-5FTN256C | 384 | 1.8 | 5 | Lead-free ftBGA | 256 | 192 | C |
| | LC4384C-75FTN256C | 384 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 192 | C |
| | LC4384C-35FN256C[1] | 384 | 1.8 | 3.5 | Lead-free fpBGA | 256 | 192 | C |
| | LC4384C-5FN256C[1] | 384 | 1.8 | 5 | Lead-free fpBGA | 256 | 192 | C |
| | LC4384C-75FN256C[1] | 384 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 192 | C |
| | LC4384C-35TN176C | 384 | 1.8 | 3.5 | Lead-free TQFP | 176 | 128 | C |
| | LC4384C-5TN176C | 384 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | C |
| | LC4384C-75TN176C | 384 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | C |