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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	128
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256b-75t176i

Table 2. ispMACH 4000Z Family Selection Guide

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t _{PD} (ns)	3.5	3.7	4.2	4.5
t _S (ns)	2.2	2.5	2.7	2.9
t _{CO} (ns)	3.0	3.2	3.5	3.8
f _{MAX} (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I _{CC} (μA)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

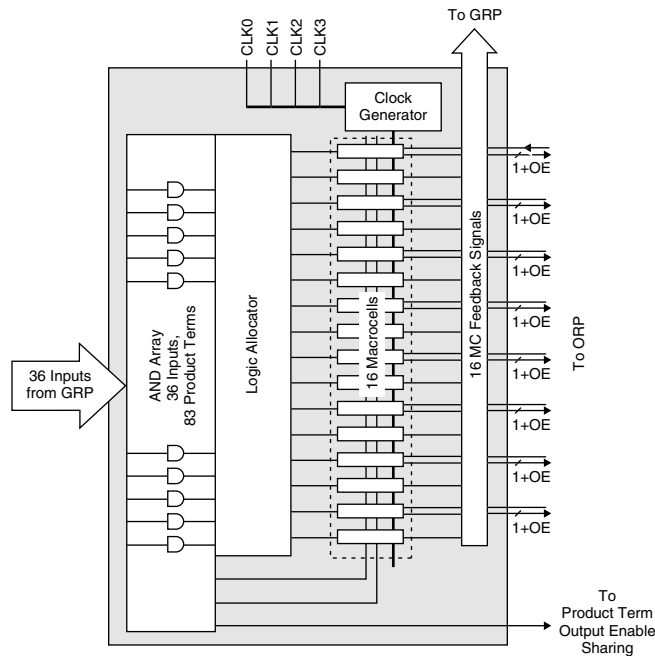
The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 2. Generic Logic Block

AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT n	Logic PT	Single PT for XOR/OR
PT $n+1$	Logic PT	Individual Clock (PT Clock)
PT $n+2$	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT $n+3$	Logic PT	Individual Initialization (PT Initialization)
PT $n+4$	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator $n+4$. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

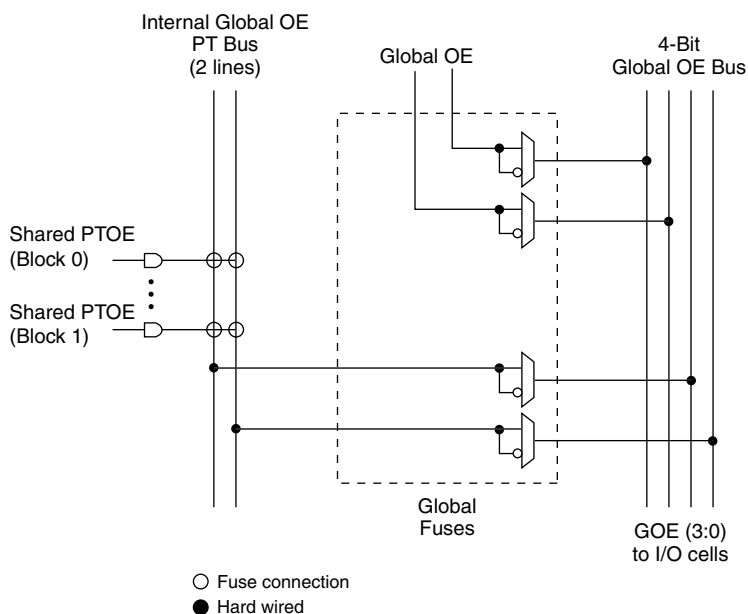
I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

Figure 10. Global OE Generation for ispMACH 4032

Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice’s ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t _S	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t _{ST}	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t _{SIR}	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t _R	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t _{RW}	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t _{CW}	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t _{WIR}	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f _{MAX} (Ext.)	clock frequency with external feedback, [1 / (t _S + t _{CO})]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t _{GOE}	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t _{BUF}	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t _{EN}	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t _{DIS}	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t _{MCELL}	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t _{FBK}	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t _{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t _{ST_PT}	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t _H	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{HT}	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t _{CES}	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t _{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t _{SL}	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t _{HL}	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t _{SRI}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹

Signal	44-pin TQFP ²	48-pin TQFP ²	56-ball csBGA ³	100-pin TQFP ²	128-pin TQFP ²
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	4032Z: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B [^] 10	D4	D [^] 2	D10	D [^] 5
34	1	B11	B [^] 11	D6	D [^] 3	D8	D [^] 4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B [^] 12	D8	D [^] 4	D6	D [^] 3
39	1	B13	B [^] 13	D10	D [^] 5	D4	D [^] 2
40	1	B14	B [^] 14	D12	D [^] 6	D2	D [^] 1
41	1	B15/GOE1	B [^] 15	D14/GOE1	D [^] 7	D0/GOE1	D [^] 0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0
45	0	A1	A [^] 1	A2	A [^] 1	A1	A [^] 1
46	0	A2	A [^] 2	A4	A [^] 2	A2	A [^] 2
47	0	A3	A [^] 3	A6	A [^] 3	A4	A [^] 3
48	0	A4	A [^] 4	A8	A [^] 4	A6	A [^] 4

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A [^] 5	A8	A [^] 5
C1	0	A6	A [^] 6	A10	A [^] 6
D1	0	A7	A [^] 7	A11	A [^] 7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC ¹	-	I ¹	-
E1	0	NC ¹	-	I ¹	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A [^] 8	B15	B [^] 7
G3	0	A9	A [^] 9	B12	B [^] 6
G1	0	A10	A [^] 10	B10	B [^] 5
H1	0	A11	A [^] 11	B8	B [^] 4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC ¹	-	I ¹	-
K4	0	A12	A [^] 12	B6	B [^] 3
H4	0	A13	A [^] 13	B4	B [^] 2
H5	0	A14	A [^] 14	B2	B [^] 1

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C ¹	E2	E ¹	I6	I ¹
43	1	C2	C ²	E4	E ²	I10	I ²
44	1	C3	C ³	E6	E ³	I12	I ³
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C ⁴	E8	E ⁴	J2	J ⁰
48	1	C5	C ⁵	E10	E ⁵	J6	J ¹
49	1	C6	C ⁶	E12	E ⁶	J10	J ²
50	1	C7	C ⁷	E14	E ⁷	J12	J ³
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C ⁸	F0	F ⁰	K12	K ³
54	1	C9	C ⁹	F2	F ¹	K10	K ²
55	1	C10	C ¹⁰	F4	F ²	K6	K ¹
56	1	C11	C ¹¹	F6	F ³	K2	K ⁰
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C ¹²	F8	F ⁴	L12	L ³
59	1	C13	C ¹³	F10	F ⁵	L10	L ²
60	1	C14	C ¹⁴	F12	F ⁶	L6	L ¹
61	1	C15	C ¹⁵	F13	F ⁷	L4	L ⁰
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D ¹⁵	G14	G ⁷	M4	M ⁰
65	1	D14	D ¹⁴	G12	G ⁶	M6	M ¹
66	1	D13	D ¹³	G10	G ⁵	M10	M ²
67	1	D12	D ¹²	G8	G ⁴	M12	M ³
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D ¹¹	G6	G ³	N2	N ⁰
70	1	D10	D ¹⁰	G5	G ²	N6	N ¹
71	1	D9	D ⁹	G4	G ¹	N10	N ²
72	1	D8	D ⁸	G2	G ⁰	N12	N ³
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D ⁷	H13	H ⁷	O12	O ³
79	1	D6	D ⁶	H12	H ⁶	O10	O ²
80	1	D5	D ⁵	H10	H ⁵	O6	O ¹
81	1	D4	D ⁴	H8	H ⁴	O2	O ⁰
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
4	0	B0	B [^] 0	C12	C [^] 6
5	0	B1	B [^] 1	C10	C [^] 5
6	0	B2	B [^] 2	C8	C [^] 4
7	0	B4	B [^] 3	C6	C [^] 3
8	0	B5	B [^] 4	C4	C [^] 2
9	0	B6	B [^] 5	C2	C [^] 1
10	0	GND (Bank 0)	-	GND (Bank 0)	-
11	0	B8	B [^] 6	D14	D [^] 7
12	0	B9	B [^] 7	D12	D [^] 6
13	0	B10	B [^] 8	D10	D [^] 5
14	0	B12	B [^] 9	D8	D [^] 4
15	0	B13	B [^] 10	D6	D [^] 3
16	0	B14	B [^] 11	D4	D [^] 2
17	-	NC ²	-	I ²	-
18	0	GND (Bank 0) ¹	-	NC ¹	-
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
20	0	NC ²	-	I ²	-
21	0	C14	C [^] 11	E2	E [^] 1
22	0	C13	C [^] 10	E4	E [^] 2
23	0	C12	C [^] 9	E6	E [^] 3
24	0	C10	C [^] 8	E8	E [^] 4
25	0	C9	C [^] 7	E10	E [^] 5
26	0	C8	C [^] 6	E12	E [^] 6
27	0	GND (Bank 0)	-	GND (Bank 0)	-
28	0	C6	C [^] 5	F2	F [^] 1
29	0	C5	C [^] 4	F4	F [^] 2
30	0	C4	C [^] 3	F6	F [^] 3
31	0	C2	C [^] 2	F8	F [^] 4
32	0	C1	C [^] 1	F10	F [^] 5
33	0	C0	C [^] 0	F12	F [^] 6
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
35	-	TCK	-	TCK	-
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	0	NC ²	-	I ²	-
39	0	D14	D [^] 11	G12	G [^] 6
40	0	D13	D [^] 10	G10	G [^] 5
41	0	D12	D [^] 9	G8	G [^] 4
42	0	D10	D [^] 8	G6	G [^] 3

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC ²	-	I ²	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.

2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C ⁷	C14	C ⁹	C14	C ⁷	C14	C ⁷
F5	0	C12	C ⁶	C12	C ⁸	C12	C ⁶	C12	C ⁶
D3	0	C10	C ⁵	C10	C ⁷	C10	C ⁵	C10	C ⁵
C1	0	C8	C ⁴	C9	C ⁶	C8	C ⁴	C8	C ⁴
C2	0	C6	C ³	C8	C ⁵	C6	C ³	C6	C ³
E3	0	C4	C ²	C6	C ⁴	C4	C ²	C4	C ²
D2	0	C2	C ¹	C4	C ³	C2	C ¹	C2	C ¹
F6	0	C0	C ⁰	C2	C ²	C0	C ⁰	C0	C ⁰
D1	0	NC	-	C1	C ¹	F6	F ³	H0	H ⁰
E2	0	NC	-	C0	C ⁰	F4	F ²	H4	H ¹
E4	0	NC	-	NC	-	D6	D ³	F4	F ²
G5	0	NC	-	NC	-	D4	D ²	F6	F ³
E1	0	NC	-	NC	-	NC	-	F8	F ⁴
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F ⁵
F1	0	NC	-	NC	-	D2	D ¹	F12	F ⁶
G1	0	NC	-	NC	-	D0	D ⁰	F14	F ⁷
G6	0	NC	-	D14	D ⁹	F2	F ¹	H8	H ²
G4	0	NC	-	D12	D ⁸	F0	F ⁰	H12	H ³
H6	0	D14	D ⁷	D10	D ⁷	E14	E ⁷	G14	G ⁷
G3	0	D12	D ⁶	D9	D ⁶	E12	E ⁶	G12	G ⁶
H5	0	D10	D ⁵	D8	D ⁵	E10	E ⁵	G10	G ⁵
G2	0	D8	D ⁴	D6	D ⁴	E8	E ⁴	G8	G ⁴
H1	0	D6	D ³	D4	D ³	E6	E ³	G6	G ³
H2	0	D4	D ²	D2	D ²	E4	E ²	G4	G ²
H3	0	D2	D ¹	D1	D ¹	E2	E ¹	G2	G ¹
H4	0	D0	D ⁰	D0	D ⁰	E0	E ⁰	G0	G ⁰
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E ⁰	E0	E ⁰	H0	H ⁰	J0	J ⁰
J3	0	E2	E ¹	E1	E ¹	H2	H ¹	J2	J ¹
J2	0	E4	E ²	E2	E ²	H4	H ²	J4	J ²
J1	0	E6	E ³	E4	E ³	H6	H ³	J6	J ³
K1	0	E8	E ⁴	E6	E ⁴	H8	H ⁴	J8	J ⁴
J5	0	E10	E ⁵	E8	E ⁵	H10	H ⁵	J10	J ⁵
K2	0	E12	E ⁶	E9	E ⁶	H12	H ⁶	J12	J ⁶

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M ¹	M1	M ¹	DX2	DX ¹	JX2	JX ¹
H14	1	M4	M ²	M2	M ²	DX4	DX ²	JX4	JX ²
H13	1	M6	M ³	M4	M ³	DX6	DX ³	JX6	JX ³
G16	1	M8	M ⁴	M6	M ⁴	DX8	DX ⁴	JX8	JX ⁴
H12	1	M10	M ⁵	M8	M ⁵	DX10	DX ⁵	JX10	JX ⁵
G15	1	M12	M ⁶	M9	M ⁶	DX12	DX ⁶	JX12	JX ⁶
H11	1	M14	M ⁷	M10	M ⁷	DX14	DX ⁷	JX14	JX ⁷
F16	1	NC	-	M12	M ⁸	CX0	CX ⁰	IX0	IX ⁰
G13	1	NC	-	M14	M ⁹	CX2	CX ¹	IX4	IX ¹
G14	1	NC	-	NC	-	EX14	EX ⁷	KX0	KX ⁰
F15	1	NC	-	NC	-	EX12	EX ⁶	KX2	KX ¹
E16	1	NC	-	NC	-	NC	-	KX4	KX ²
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX ³
G12	1	NC	-	NC	-	EX10	EX ⁵	KX8	KX ⁴
E13	1	NC	-	NC	-	EX8	EX ⁴	KX10	KX ⁵
D16	1	NC	-	N0	N ⁰	CX4	CX ²	IX8	IX ²
E14	1	NC	-	N1	N ¹	CX6	CX ³	IX12	IX ³
G11	1	N0	N ⁰	N2	N ²	FX0	FX ⁰	NX0	NX ⁰
D15	1	N2	N ¹	N4	N ³	FX2	FX ¹	NX2	NX ¹
F11	1	N4	N ²	N6	N ⁴	FX4	FX ²	NX4	NX ²
C16	1	N6	N ³	N8	N ⁵	FX6	FX ³	NX6	NX ³
F12	1	N8	N ⁴	N9	N ⁶	FX8	FX ⁴	NX8	NX ⁴
D14	1	N10	N ⁵	N10	N ⁷	FX10	FX ⁵	NX10	NX ⁵
C15	1	N12	N ⁶	N12	N ⁸	FX12	FX ⁶	NX12	NX ⁶
B16	1	N14	N ⁷	N14	N ⁹	FX14	FX ⁷	NX14	NX ⁷
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX ³	KX12	KX ⁶
B14	1	NC	-	NC	-	EX4	EX ²	KX14	KX ⁷
E12	1	O14	O ⁷	O14	O ⁹	GX14	GX ⁷	OX14	OX ⁷
A14	1	O12	O ⁶	O12	O ⁸	GX12	GX ⁶	OX12	OX ⁶
C13	1	O10	O ⁵	O10	O ⁷	GX10	GX ⁵	OX10	OX ⁵
D13	1	O8	O ⁴	O9	O ⁶	GX8	GX ⁴	OX8	OX ⁴
E11	1	O6	O ³	O8	O ⁵	GX6	GX ³	OX6	OX ³
B13	1	O4	O ²	O6	O ⁴	GX4	GX ²	OX4	OX ²
F10	1	O2	O ¹	O4	O ³	GX2	GX ¹	OX2	OX ¹

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI ¹	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI ¹	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI ¹	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI ¹	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI ¹	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI ¹	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI ¹	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI ¹	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI ¹	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI ¹	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI ¹	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI ¹	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
	LC4256V-10T100I	256	3.3	10	TQFP	100	64	I
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I ¹	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I ¹	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I ¹	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I ¹	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I ¹	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I ¹	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI ¹	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI ¹	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI ¹	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI ¹	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI ¹	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI ¹	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I ¹	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I ¹	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I ¹	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I ¹	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I ¹	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I ¹	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C ¹	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C ¹	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
	LC4384B-75TN176C	384	2.5	7.5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C ¹	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C ¹	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 μ A to -200 μ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to "LA" automotive data sheet under the "Broad Device Offering" bullet.
		Added footnote 1 to Part Number Description to reference the "LA" automotive data sheet.
		Changed device temperature references from 'Automotive' to "Extended Temperature" for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.