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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (Tj)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256c-10t100i

Table 2. ispMACH 4000Z Family Selection Guide

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t _{PD} (ns)	3.5	3.7	4.2	4.5
t _S (ns)	2.2	2.5	2.7	2.9
t _{CO} (ns)	3.0	3.2	3.5	3.8
f _{MAX} (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I _{CC} (μA)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT n	Logic PT	Single PT for XOR/OR
PT $n+1$	Logic PT	Individual Clock (PT Clock)
PT $n+2$	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT $n+3$	Logic PT	Individual Initialization (PT Initialization)
PT $n+4$	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator $n+4$. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

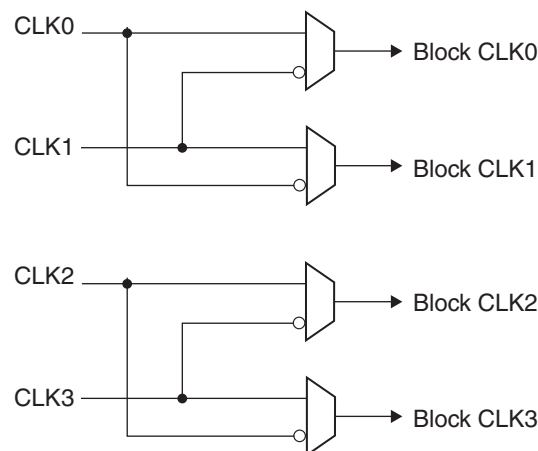
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTTL	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	$0.35 * V_{CC}$	$0.65 * V_{CC}$	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	$0.3 * 3.3 * (V_{CC} / 1.8)$	$0.5 * 3.3 * (V_{CC} / 1.8)$	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t _S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t _{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t _{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t _R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t _{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t _{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t _{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f _{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t _S + t _{CO})]	—	250	—	222	—	212	—	212	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.3.2

2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
t_S	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
t_R	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
t_{RW}	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
t_{CW}	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
t_{WIR}	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
f_{MAX}^4	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
$f_{MAX} (Ext.)$	clock frequency with external feedback, $[1 / (t_S + t_{CO})]$	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

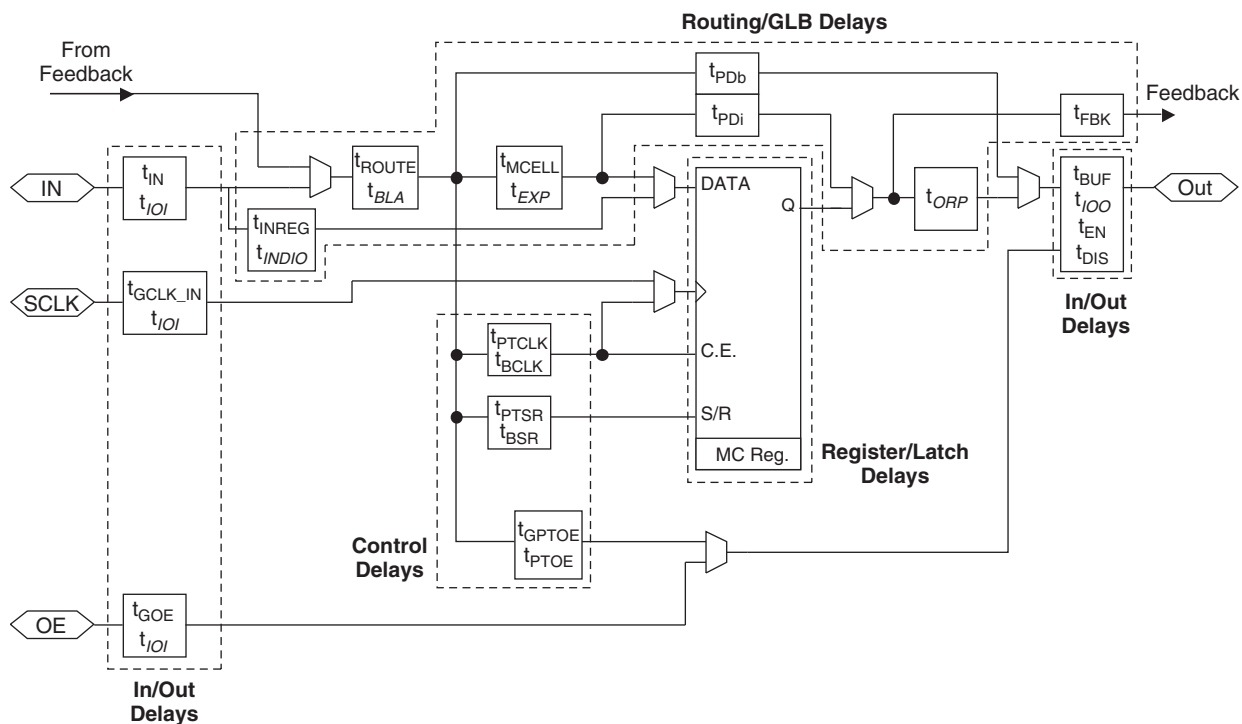
3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#).

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.95	—	1.25	—	1.80	ns
t _{GOE}	Global OE Pin Delay	—	3.00	—	3.50	—	4.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.05	—	2.15	ns
t _{BUF}	Delay through Output Buffer	—	1.10	—	1.00	—	1.30	ns
t _{EN}	Output Enable Time	—	2.50	—	2.50	—	2.70	ns
t _{DIS}	Output Disable Time	—	2.50	—	2.50	—	2.70	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	2.25	—	2.05	—	2.50	ns
t _{MCELL}	Macrocell Delay	—	0.65	—	0.65	—	1.00	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	—	1.00	ns
t _{FBK}	Internal Feedback Delay	—	0.35	—	0.05	—	0.05	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.20	—	0.70	—	1.90	ns
t _{PDi}	Macrocell Propagation Delay	—	0.45	—	0.65	—	1.00	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	1.00	—	1.10	—	1.35	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	2.10	—	1.90	—	2.45	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.20	—	1.30	—	1.55	—	ns
t _{ST_PT}	T-register Setup Time (Product Term Clock)	2.30	—	2.10	—	2.75	—	ns
t _H	D-Register Hold Time	1.90	—	1.90	—	3.15	—	ns
t _{HT}	T-Resister Hold Time	1.90	—	1.90	—	3.15	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	1.30	—	1.10	—	0.75	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	1.30	—	1.50	—	1.95	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.00	—	1.00	—	1.18	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.75	—	1.15	—	1.05	ns
t _{CES}	Clock Enable Setup Time	2.00	—	2.00	—	2.00	—	ns
t _{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t _{SL}	Latch Setup Time (Global Clock)	1.00	—	1.00	—	1.65	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	2.10	—	1.90	—	2.15	—	ns
t _{HL}	Latch Hold Time	2.00	—	2.00	—	1.17	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t _{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.97	—	0.97	—	0.28	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.80	—	1.80	—	1.67	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.83	—	1.83	—	2.72	ns
t _{GPTOE}	Global PT OE Delay	—	4.30	—	4.20	—	3.50	ns

ispMACH 4000V/B/C Timing Adders¹ (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.00	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t _{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t _{BLA}	t _{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

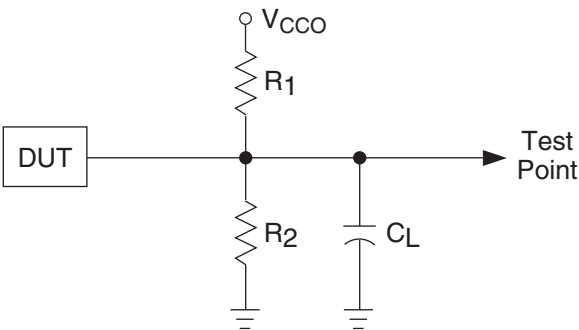
Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTTL and LVCMOS Standards



0213A/ispm4k

Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L^1	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106 Ω	106 Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $V_{CCO}/2$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $V_{CCO}/2$	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106 Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106 Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106 Ω	5pF	$V_{OH} - 0.3$	3.0V
LVCMOS I/O (L -> Z)	106 Ω	∞	5pF	$V_{OL} + 0.3$	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹

Signal	44-pin TQFP ²	48-pin TQFP ²	56-ball csBGA ³	100-pin TQFP ²	128-pin TQFP ²
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	4032Z: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹ (Cont.)

Signal	132-ball csBGA ⁷	144-pin TQFP ⁴	176-pin TQFP ⁴	256-ball ftBGA/fpBGA ^{2,3,7,9}
VCC	P1, A14, B7, N8	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
VCCO0 VCCO (Bank 0)	G3, P5, C1 ⁸ , M2 ⁸ , C5	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1 VCCO (Bank 1)	M10, M14 ⁸ , H12, A10, C13 ⁸	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	B1, P2, N14, A13	1, 37, 73, 109	2, 46 ⁵ , 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank 0)	E2, K2, N4, B4	10, 18 ⁶ , 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	N11, K13, E13, B11	55, 65, 82, 90 ⁶ , 99, 118	67, 79, 101, 119, 143	
NC	4064Z: C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1 4128Z: P8, A7	4128V: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 4256V: 18, 90	1, 43, 44, 45, 89, 131, 132, 133	4256V/B/C, 128 I/O: A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15 4256V/B/C, 160 I/O: A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15 4384V/B/C: B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4 4512V/B/C: None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. VCCO balls connect to two power planes within the package, one for VCCO0 and one for VCCO1.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

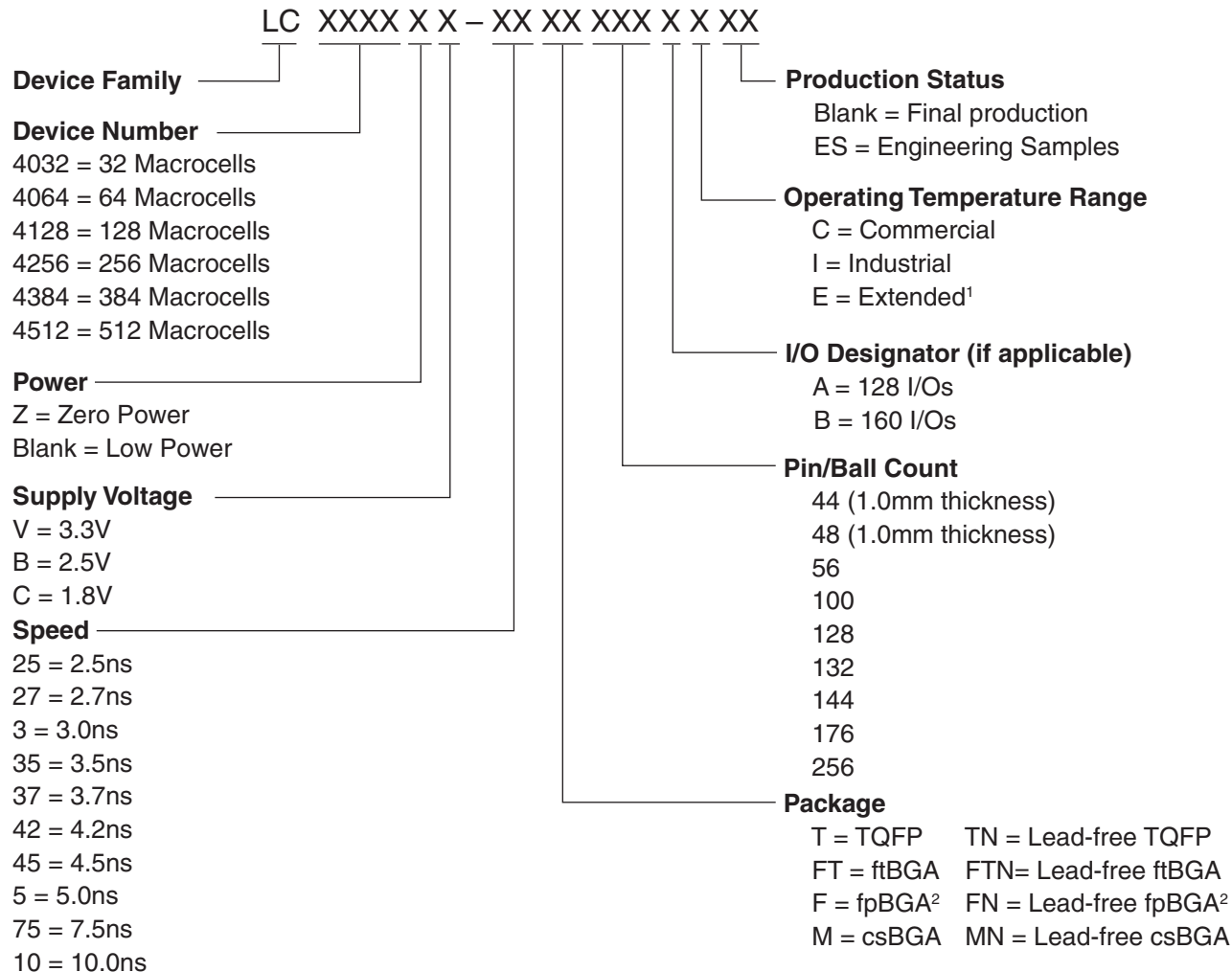
**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C^1	E2	E^1	I6	I^1
43	1	C2	C^2	E4	E^2	I10	I^2
44	1	C3	C^3	E6	E^3	I12	I^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4	J2	J^0
48	1	C5	C^5	E10	E^5	J6	J^1
49	1	C6	C^6	E12	E^6	J10	J^2
50	1	C7	C^7	E14	E^7	J12	J^3
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0	K12	K^3
54	1	C9	C^9	F2	F^1	K10	K^2
55	1	C10	C^10	F4	F^2	K6	K^1
56	1	C11	C^11	F6	F^3	K2	K^0
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4	L12	L^3
59	1	C13	C^13	F10	F^5	L10	L^2
60	1	C14	C^14	F12	F^6	L6	L^1
61	1	C15	C^15	F13	F^7	L4	L^0
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7	M4	M^0
65	1	D14	D^14	G12	G^6	M6	M^1
66	1	D13	D^13	G10	G^5	M10	M^2
67	1	D12	D^12	G8	G^4	M12	M^3
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3	N2	N^0
70	1	D10	D^10	G5	G^2	N6	N^1
71	1	D9	D^9	G4	G^1	N10	N^2
72	1	D8	D^8	G2	G^0	N12	N^3
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D^7	H13	H^7	O12	O^3
79	1	D6	D^6	H12	H^6	O10	O^2
80	1	D5	D^5	H10	H^5	O6	O^1
81	1	D4	D^4	H8	H^4	O2	O^0
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F ⁹	L8	L ⁴
87	1	F13	F ¹⁰	L6	L ³
88	1	F14	F ¹¹	L4	L ²
89	1	NC ²	-	I ²	-
90	1	GND (Bank 1) ¹	-	NC ¹	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC ²	-	I ²	-
93	1	G14	G ¹¹	M2	M ¹
94	1	G13	G ¹⁰	M4	M ²
95	1	G12	G ⁹	M6	M ³
96	1	G10	G ⁸	M8	M ⁴
97	1	G9	G ⁷	M10	M ⁵
98	1	G8	G ⁶	M12	M ⁶
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G ⁵	N2	N ¹
101	1	G5	G ⁴	N4	N ²
102	1	G4	G ³	N6	N ³
103	1	G2	G ²	N8	N ⁴
104	1	G1	G ¹	N10	N ⁵
105	1	G0	G ⁰	N12	N ⁶
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC ²	-	I ²	-
111	1	H14	H ¹¹	O12	O ⁶
112	1	H13	H ¹⁰	O10	O ⁵
113	1	H12	H ⁹	O8	O ⁴
114	1	H10	H ⁸	O6	O ³
115	1	H9	H ⁷	O4	O ²
116	1	H8	H ⁶	O2	O ¹
117	1	NC ²	-	I ²	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H ⁵	P12	P ⁶
121	1	H5	H ⁴	P10	P ⁵
122	1	H4	H ³	P8	P ⁴
123	1	H2	H ²	P6	P ³
124	1	H1	H ¹	P4	P ²
125	1	H0/GOE1	H ⁰	P2/GOE1	P ¹
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

ispMACH 4000C (1.8V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032C-75T48I	32	1.8	7.5	TQFP	48	32	I
	LC4032C-10T48I	32	1.8	10	TQFP	48	32	I
	LC4032C-5T44I	32	1.8	5	TQFP	44	30	I
	LC4032C-75T44I	32	1.8	7.5	TQFP	44	30	I
	LC4032C-10T44I	32	1.8	10	TQFP	44	30	I
LC4064C	LC4064C-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064C-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064C-10T100I	64	1.8	10	TQFP	100	64	I
	LC4064C-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064C-75T48I	64	1.8	7.5	TQFP	48	32	I
	LC4064C-10T48I	64	1.8	10	TQFP	48	32	I
	LC4064C-5T44I	64	1.8	5	TQFP	44	30	I
	LC4064C-75T44I	64	1.8	7.5	TQFP	44	30	I
	LC4064C-10T44I	64	1.8	10	TQFP	44	30	I
LC4128C	LC4128C-5T128I	128	1.8	5	TQFP	128	92	I
	LC4128C-75T128I	128	1.8	7.5	TQFP	128	92	I
	LC4128C-10T128I	128	1.8	10	TQFP	128	92	I
	LC4128C-5T100I	128	1.8	5	TQFP	100	64	I
	LC4128C-75T100I	128	1.8	7.5	TQFP	100	64	I
	LC4128C-10T100I	128	1.8	10	TQFP	100	64	I
LC4256C	LC4256C-5FT256AI	256	1.8	5	ftBGA	256	128	I
	LC4256C-75FT256AI	256	1.8	7.5	ftBGA	256	128	I
	LC4256C-10FT256AI	256	1.8	10	ftBGA	256	128	I
	LC4256C-5FT256BI	256	1.8	5	ftBGA	256	160	I
	LC4256C-75FT256BI	256	1.8	7.5	ftBGA	256	160	I
	LC4256C-10FT256BI	256	1.8	10	ftBGA	256	160	I
	LC4256C-5F256AI ¹	256	1.8	5	fpBGA	256	128	I
	LC4256C-75F256AI ¹	256	1.8	7.5	fpBGA	256	128	I
	LC4256C-10F256AI ¹	256	1.8	10	fpBGA	256	128	I
	LC4256C-5F256BI ¹	256	1.8	5	fpBGA	256	160	I
	LC4256C-75F256BI ¹	256	1.8	7.5	fpBGA	256	160	I
	LC4256C-10F256BI ¹	256	1.8	10	fpBGA	256	160	I
	LC4256C-5T176I	256	1.8	5	TQFP	176	128	I
	LC4256C-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256C-10T176I	256	1.8	10	TQFP	176	128	I
	LC4256C-5T100I	256	1.8	5	TQFP	100	64	I
	LC4256C-75T100I	256	1.8	7.5	TQFP	100	64	I
	LC4256C-10T100I	256	1.8	10	TQFP	100	64	I

ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064C	LC4064C-25TN100C	64	1.8	2.5	Lead-free TQFP	100	64	C
	LC4064C-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064C-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064C-25TN48C	64	1.8	2.5	Lead-free TQFP	48	32	C
	LC4064C-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064C-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
	LC4064C-25TN44C	64	1.8	2.5	Lead-free TQFP	44	30	C
	LC4064C-5TN44C	64	1.8	5	Lead-free TQFP	44	30	C
	LC4064C-75TN44C	64	1.8	7.5	Lead-free TQFP	44	30	C
LC4128C	LC4128C-27TN128C	128	1.8	2.7	Lead-free TQFP	128	92	C
	LC4128C-5TN128C	128	1.8	5	Lead-free TQFP	128	92	C
	LC4128C-75TN128C	128	1.8	7.5	Lead-free TQFP	128	92	C
	LC4128C-27TN100C	128	1.8	2.7	Lead-free TQFP	100	64	C
	LC4128C-5TN100C	128	1.8	5	Lead-free TQFP	100	64	C
	LC4128C-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256C	LC4256C-3FTN256AC	256	1.8	3	Lead-free ftBGA	256	128	C
	LC4256C-5FTN256AC	256	1.8	5	Lead-free ftBGA	256	128	C
	LC4256C-75FTN256AC	256	1.8	7.5	Lead-free ftBGA	256	128	C
	LC4256C-3FTN256BC	256	1.8	3	Lead-free ftBGA	256	160	C
	LC4256C-5FTN256BC	256	1.8	5	Lead-free ftBGA	256	160	C
	LC4256C-75FTN256BC	256	1.8	7.5	Lead-free ftBGA	256	160	C
	LC4256C-3FN256AC ¹	256	1.8	3	Lead-free fpBGA	256	128	C
	LC4256C-5FN256AC ¹	256	1.8	5	Lead-free fpBGA	256	128	C
	LC4256C-75FN256AC ¹	256	1.8	7.5	Lead-free fpBGA	256	128	C
	LC4256C-3FN256BC ¹	256	1.8	3	Lead-free fpBGA	256	160	C
	LC4256C-5FN256BC ¹	256	1.8	5	Lead-free fpBGA	256	160	C
	LC4256C-75FN256BC ¹	256	1.8	7.5	Lead-free fpBGA	256	160	C
	LC4256C-3TN176C	256	1.8	3	Lead-free TQFP	176	128	C
	LC4256C-5TN176C	256	1.8	5	Lead-free TQFP	176	128	C
	LC4256C-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256C-3TN100C	256	1.8	3	Lead-free TQFP	100	64	C
	LC4256C-5TN100C	256	1.8	5	Lead-free TQFP	100	64	C
	LC4256C-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C
LC4384C	LC4384C-35FTN256C	384	1.8	3.5	Lead-free ftBGA	256	192	C
	LC4384C-5FTN256C	384	1.8	5	Lead-free ftBGA	256	192	C
	LC4384C-75FTN256C	384	1.8	7.5	Lead-free ftBGA	256	192	C
	LC4384C-35FN256C ¹	384	1.8	3.5	Lead-free fpBGA	256	192	C
	LC4384C-5FN256C ¹	384	1.8	5	Lead-free fpBGA	256	192	C
	LC4384C-75FN256C ¹	384	1.8	7.5	Lead-free fpBGA	256	192	C
	LC4384C-35TN176C	384	1.8	3.5	Lead-free TQFP	176	128	C
	LC4384C-5TN176C	384	1.8	5	Lead-free TQFP	176	128	C
	LC4384C-75TN176C	384	1.8	7.5	Lead-free TQFP	176	128	C

ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
	LC4064B-75TN44C	64	2.5	7.5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC ¹	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC ¹	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC ¹	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC ¹	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC ¹	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC ¹	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
	LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C
	LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C

ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C ¹	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C ¹	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
	LC4384B-75TN176C	384	2.5	7.5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C ¹	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C ¹	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I