**Welcome to E-XFL.COM**

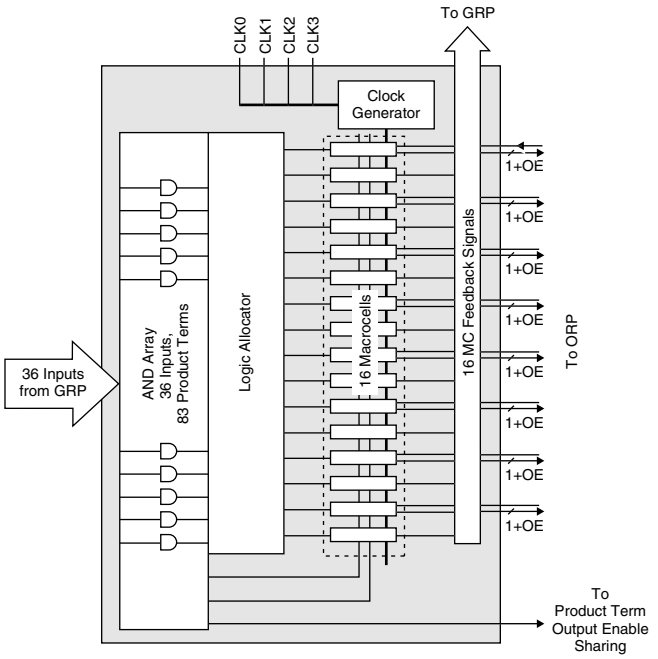
## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 64 |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256v-10t100i |

***Figure 2. Generic Logic Block***

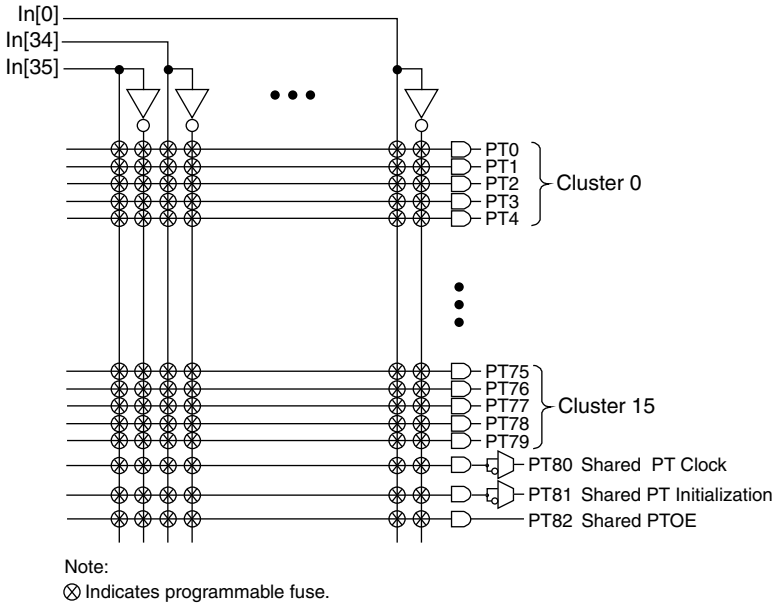



## AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

***Figure 3. AND Array***




## Enhanced Logic Allocator

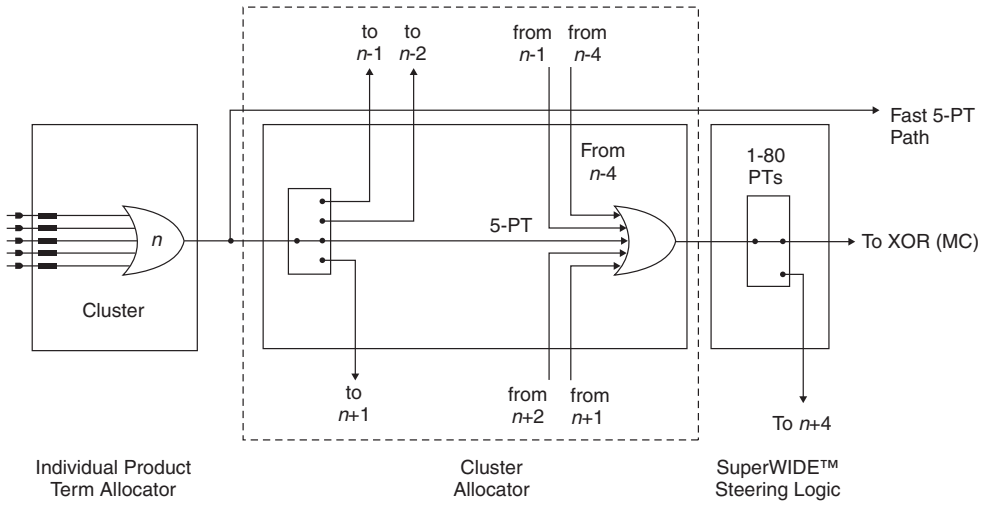
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

***Figure 4. Macrocell Slice***



## Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

***Table 3. Individual PT Steering***

| Product Term | Logic | Control |
|---|---|---|
| PT*n* | Logic PT | Single PT for XOR/OR |
| PT*n*+1 | Logic PT | Individual Clock (PT Clock) |
| PT*n*+2 | Logic PT | Individual Initialization or Individual Clock Enable (PT Initialization/CE) |
| PT*n*+3 | Logic PT | Individual Initialization (PT Initialization) |
| PT*n*+4 | Logic PT | Individual OE (PTOE) |

## Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

***Table 4. Available Clusters for Each Macrocell***

| Macrocell | Available Clusters | | | |
|---|---|---|---|---|
| M0 | — | C0 | C1 | C2 |
| M1 | C0 | C1 | C2 | C3 |
| M2 | C1 | C2 | C3 | C4 |
| M3 | C2 | C3 | C4 | C5 |
| M4 | C3 | C4 | C5 | C6 |
| M5 | C4 | C5 | C6 | C7 |
| M6 | C5 | C6 | C7 | C8 |
| M7 | C6 | C7 | C8 | C9 |
| M8 | C7 | C8 | C9 | C10 |
| M9 | C8 | C9 | C10 | C11 |
| M10 | C9 | C10 | C11 | C12 |
| M11 | C10 | C11 | C12 | C13 |
| M12 | C11 | C12 | C13 | C14 |
| M13 | C12 | C13 | C14 | C15 |
| M14 | C13 | C14 | C15 | — |
| M15 | C14 | C15 | — | — |

## Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

*Table 7. ORP Combinations for I/O Blocks with 16 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M1, M2, M3, M4, M5, M6, M7, M8 |
| I/O 2 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 3 | M3, M4, M5, M6, M7, M8, M9, M10 |
| I/O 4 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 5 | M5, M6, M7, M8, M9, M10, M11, M12 |
| I/O 6 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 7 | M7, M8, M9, M10, M11, M12, M13, M14 |
| I/O 8 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 9 | M9, M10, M11, M12, M13, M14, M15, M0 |
| I/O 10 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 11 | M11, M12, M13, M14, M15, M0, M1, M2 |
| I/O 12 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 13 | M13, M14, M15, M0, M1, M2, M3, M4 |
| I/O 14 | M14, M15, M0, M1, M2, M3, M4, M5 |
| I/O 15 | M15, M0, M1, M2, M3, M4, M5, M6 |

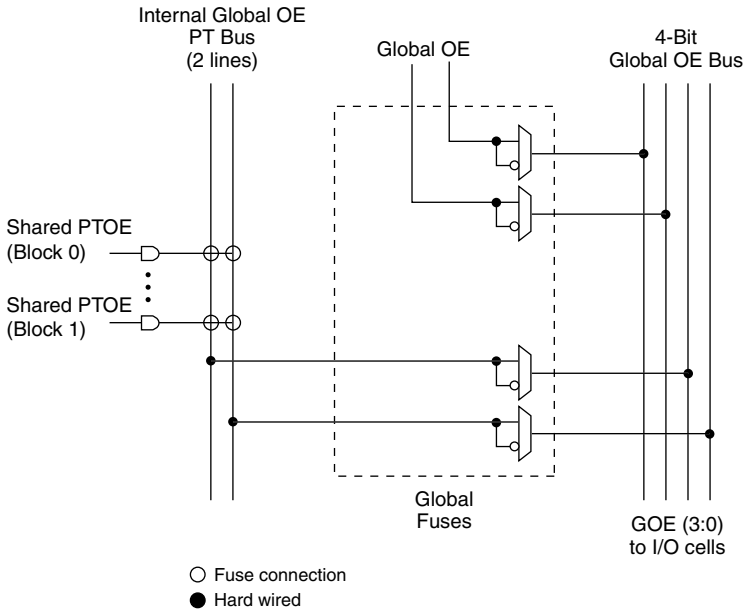
*Table 8. ORP Combinations for I/O Blocks with 4 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 2 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 3 | M12, M13, M14, M15, M0, M1, M2, M3 |

*Table 9. ORP Combinations for I/O Blocks with 10 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 2 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 3 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 4 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 5 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 6 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 7 | M14, M15, M0, M1, M2, M3, M4, M5 |
| I/O 8 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 9 | M10, M11, M12, M13, M14, M15, M0, M1 |

***Figure 10. Global OE Generation for ispMACH 4032***




## Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced $E^2$ low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

## IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

## I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

## IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

## User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in $E^2$CMOS memory. The ispMACH 4000 device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

## Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

## Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

# Supply Current, ispMACH 4000V/B/C

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ispMACH 4032V/B/C** | | | | | | |
| $ICC^{1,2,3}$ | Operating Power Supply Current | Vcc = 3.3V | — | 11.8 | — | mA |
| | | Vcc = 2.5V | — | 11.8 | — | mA |
| | | Vcc = 1.8V | — | 1.8 | — | mA |
| $ICC^{4}$ | Standby Power Supply Current | Vcc = 3.3V | — | 11.3 | — | mA |
| | | Vcc = 2.5V | — | 11.3 | — | mA |
| | | Vcc = 1.8V | — | 1.3 | — | mA |
| **ispMACH 4064V/B/C** | | | | | | |
| $ICC^{1,2,3}$ | Operating Power Supply Current | Vcc = 3.3V | — | 12 | — | mA |
| | | Vcc = 2.5V | — | 12 | — | mA |
| | | Vcc = 1.8V | — | 2 | — | mA |
| $ICC^{5}$ | Standby Power Supply Current | Vcc = 3.3V | — | 11.5 | — | mA |
| | | Vcc = 2.5V | — | 11.5 | — | mA |
| | | Vcc = 1.8V | — | 1.5 | — | mA |
| **ispMACH 4128V/B/C** | | | | | | |
| $ICC^{1,2,3}$ | Operating Power Supply Current | Vcc = 3.3V | — | 12 | — | mA |
| | | Vcc = 2.5V | — | 12 | — | mA |
| | | Vcc = 1.8V | — | 2 | — | mA |
| $ICC^{4}$ | Standby Power Supply Current | Vcc = 3.3V | — | 11.5 | — | mA |
| | | Vcc = 2.5V | — | 11.5 | — | mA |
| | | Vcc = 1.8V | — | 1.5 | — | mA |
| **ispMACH 4256V/B/C** | | | | | | |
| $I_{CC}^{1,2,3}$ | Operating Power Supply Current | Vcc = 3.3V | — | 12.5 | — | mA |
| | | Vcc = 2.5V | — | 12.5 | — | mA |
| | | Vcc = 1.8V | — | 2.5 | — | mA |
| $I_{CC}^{4}$ | Standby Power Supply Current | Vcc = 3.3V | — | 12 | — | mA |
| | | Vcc = 2.5V | — | 12 | — | mA |
| | | Vcc = 1.8V | — | 2 | — | mA |
| **ispMACH 4384V/B/C** | | | | | | |
| $I_{CC}^{1,2,3}$ | Operating Power Supply Current | Vcc = 3.3V | — | 13.5 | — | mA |
| | | Vcc = 2.5V | — | 13.5 | — | mA |
| | | Vcc = 1.8V | — | 3.5 | — | mA |
| $I_{CC}^{4}$ | Standby Power Supply Current | Vcc = 3.3V | — | 12.5 | — | mA |
| | | Vcc = 2.5V | — | 12.5 | — | mA |
| | | Vcc = 1.8V | — | 2.5 | — | mA |
| **ispMACH 4512V/B/C** | | | | | | |
| $I_{CC}^{1,2,3}$ | Operating Power Supply Current | Vcc = 3.3V | — | 14 | — | mA |
| | | Vcc = 2.5V | — | 14 | — | mA |
| | | Vcc = 1.8V | — | 4 | — | mA |

# Supply Current, ispMACH 4000Z (Cont.)

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ispMACH 4256ZC** | | | | | | |
| ICC[1, 2, 3, 5] | Operating Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 341 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 70°C | — | 361 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 85°C | — | 372 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 125°C | — | 468 | — | µA |
| ICC[4, 5] | Standby Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 13 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 70°C | — | 32 | 55 | µA |
| | | Vcc = 1.9V, $T_A$ = 85°C | — | 43 | 90 | µA |
| | | Vcc = 1.9V, $T_A$ = 125°C | — | 135 | — | µA |

1. $T_A$ = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. $I_{CC}$ varies with specific device configuration and operating frequency.
4. $V_{CCO}$ = 3.6V, $V_{IN}$ = 0V or $V_{CCO,}$ bus maintenance turned off. $V_{IN}$ above $V_{CCO}$ will add transient current above the specified standby $I_{CC}$.
5. Includes $V_{CCO}$ current without output loading.

# ispMACH 4000V/B/C External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -25 | | -27 | | -3 | | -35 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 2.5 | — | 2.7 | — | 3.0 | — | 3.5 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 3.2 | — | 3.5 | — | 3.8 | — | 4.2 | ns |
| $t_S$ | GLB register setup time before clock | 1.8 | — | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 2.0 | — | 2.0 | — | 2.2 | — | 2.2 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 0.7 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 1.7 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 0.9 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 2.2 | — | 2.7 | — | 2.7 | — | 2.7 | ns |
| $t_R$ | External reset pin to output delay | — | 3.5 | — | 4.0 | — | 4.4 | — | 4.5 | ns |
| $t_{RW}$ | External reset pulse duration | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | - | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 4.0 | — | 4.5 | — | 5.0 | — | 5.5 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 5.0 | — | 6.5 | — | 8.0 | — | 8.0 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 3.0 | — | 3.5 | — | 4.0 | — | 4.5 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.1 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.1 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.1 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 400 | — | 333 | — | 322 | — | 322 | MHz |
| $f_{MAX}$ (Ext.) | Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$ | — | 250 | — | 222 | — | 212 | — | 212 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

# ispMACH 4000Z External Switching Characteristics (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -45 | | -5 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 4.5 | — | 5.0 | — | 7.5 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 5.8 | — | 6.0 | — | 8.0 | ns |
| $t_S$ | GLB register setup time before clock | 2.9 | — | 3.0 | — | 4.5 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 3.1 | — | 3.2 | — | 4.7 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.3 | — | 1.3 | — | 1.4 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.6 | — | 2.6 | — | 2.7 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.8 | — | 4.2 | — | 4.5 | ns |
| $t_R$ | External reset pin to output delay | — | 7.5 | — | 7.5 | — | 9.0 | ns |
| $t_{RW}$ | External reset pulse duration | 2.0 | — | 2.0 | — | 4.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 8.2 | — | 8.5 | — | 9.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 10.0 | — | 10.0 | — | 10.5 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 5.5 | — | 6.0 | — | 7.0 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.8 | — | 2.0 | — | 2.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.8 | — | 2.0 | — | 2.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.8 | — | 2.0 | — | 2.8 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 200 | — | 200 | — | 168 | MHz |
| $f_{MAX}$ (Ext.) | clock frequency with external feedback, [1 / ($t_S$ + $t_{CO}$)] | — | 150 | — | 139 | — | 111 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

# ispMACH 4000Z Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{GPTOE}$ | Global PT OE Delay | — | 1.9 | — | 2.35 | — | 2.60 | ns |
| $t_{PTOE}$ | Macrocell PT OE Delay | — | 2.4 | — | 3.35 | — | 2.60 | ns |

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

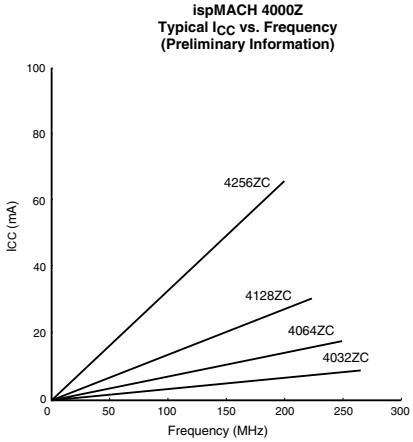
Timing v.2.2

# ispMACH 4000Z Internal Timing Parameters (Cont.)

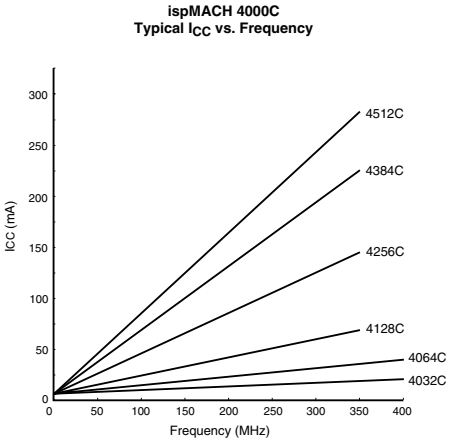
**Over Recommended Operating Conditions**

| Parameter | Description | -45 | | -5 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 0.95 | — | 1.25 | — | 1.80 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 3.00 | — | 3.50 | — | 4.30 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 1.95 | — | 2.05 | — | 2.15 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 1.10 | — | 1.00 | — | 1.30 | ns |
| $t_{EN}$ | Output Enable Time | — | 2.50 | — | 2.50 | — | 2.70 | ns |
| $t_{DIS}$ | Output Disable Time | — | 2.50 | — | 2.50 | — | 2.70 | ns |
| **Routing/GLB Delays** | | | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 2.25 | — | 2.05 | — | 2.50 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 0.65 | — | 0.65 | — | 1.00 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 1.00 | — | 1.00 | — | 1.00 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.35 | — | 0.05 | — | 0.05 | ns |
| $t_{PDb}$ | 5-PT Bypass Propagation Delay | — | 0.20 | — | 0.70 | — | 1.90 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.45 | — | 0.65 | — | 1.00 | ns |
| **Register/Latch Delays** | | | | | | | | |
| $t_{S}$ | D-Register Setup Time (Global Clock) | 1.00 | — | 1.10 | — | 1.35 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 2.10 | — | 1.90 | — | 2.45 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.20 | — | 1.30 | — | 1.55 | — | ns |
| $t_{ST\_PT}$ | T-register Setup Time (Product Term Clock) | 2.30 | — | 2.10 | — | 2.75 | — | ns |
| $t_{H}$ | D-Register Hold Time | 1.90 | — | 1.90 | — | 3.15 | — | ns |
| $t_{HT}$ | T-Resister Hold Time | 1.90 | — | 1.90 | — | 3.15 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 1.30 | — | 1.10 | — | 0.75 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 1.30 | — | 1.50 | — | 1.95 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 1.00 | — | 1.00 | — | 1.18 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.75 | — | 1.15 | — | 1.05 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 1.00 | — | 1.00 | — | 1.65 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 2.10 | — | 1.90 | — | 2.15 | — | ns |
| $t_{HL}$ | Latch Hold Time | 2.00 | — | 2.00 | — | 1.17 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.33 | — | 0.33 | — | 0.33 | ns |
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.97 | — | 0.97 | — | 0.28 | ns |
| $t_{SRR}$ | Asynchronous Reset or Set Recovery Delay | — | 1.80 | — | 1.80 | — | 1.67 | ns |
| **Control Delays** | | | | | | | | |
| $t_{BCLK}$ | GLB PT Clock Delay | — | 1.55 | — | 1.55 | — | 1.25 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | — | 1.55 | — | 1.55 | — | 1.25 | ns |
| $t_{BSR}$ | GLB PT Set/Reset Delay | — | 1.83 | — | 1.83 | — | 1.83 | ns |
| $t_{PTSR}$ | Macrocell PT Set/Reset Delay | — | 1.83 | — | 1.83 | — | 2.72 | ns |
| $t_{GPTOE}$ | Global PT OE Delay | — | 4.30 | — | 4.20 | — | 3.50 | ns |

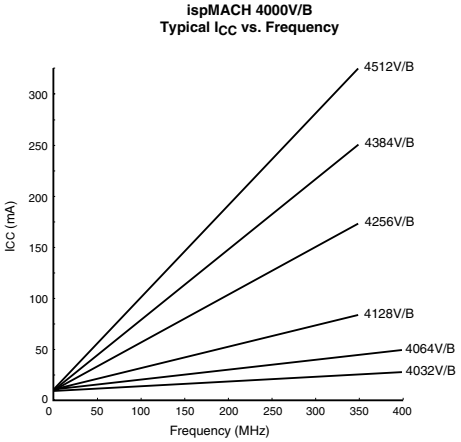
# Power Consumption




Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.




Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.




Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

# Power Estimation Coefficients[1]

| Device | A | B |
|---|---|---|
| ispMACH 4032V/B | 11.3 | 0.010 |
| ispMACH 4032C | 1.3 | 0.010 |
| ispMACH 4064V/B | 11.5 | 0.010 |
| ispMACH 4064C | 1.5 | 0.010 |
| ispMACH 4128V/B | 11.5 | 0.011 |
| ispMACH 4128C | 1.5 | 0.011 |
| ispMACH 4256V/B | 12 | 0.011 |
| ispMACH 4256C | 2 | 0.011 |
| ispMACH 4384V/B | 12.5 | 0.013 |
| ispMACH 4384C | 2.5 | 0.013 |
| ispMACH 4512V/B | 13 | 0.013 |
| ispMACH 4512C | 3 | 0.013 |
| ispMACH 4032ZC | 0.010 | 0.010 |
| ispMACH 4064ZC | 0.011 | 0.010 |
| ispMACH 4128ZC | 0.012 | 0.010 |
| ispMACH 4256ZC | 0.013 | 0.010 |

1. For further information about the use of these coefficients, refer to TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices.

## ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4032V/B/C | | ispMACH 4064V/B/C | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 42 | 0 | A2 | A^2 | A4 | A^2 |
| 43 | 0 | A3 | A^3 | A6 | A^3 |
| 44 | 0 | A4 | A^4 | A8 | A^4 |

## ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP

| Pin Number | Bank Number | ispMACH 4032V/B/C/Z | | ispMACH 4064V/B/C | | ispMACH 4064Z | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 1 | - | TDI | - | TDI | - | TDI | - |
| 2 | 0 | A5 | A^5 | A10 | A^5 | A8 | A^5 |
| 3 | 0 | A6 | A^6 | A12 | A^6 | A10 | A^6 |
| 4 | 0 | A7 | A^7 | A14 | A^7 | A11 | A^7 |
| 5 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 6 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 7 | 0 | A8 | A^8 | B0 | B^0 | B15 | B^7 |
| 8 | 0 | A9 | A^9 | B2 | B^1 | B12 | B^6 |
| 9 | 0 | A10 | A^10 | B4 | B^2 | B10 | B^5 |
| 10 | 0 | A11 | A^11 | B6 | B^3 | B8 | B^4 |
| 11 | - | TCK | - | TCK | - | TCK | - |
| 12 | - | VCC | - | VCC | - | VCC | - |
| 13 | - | GND | - | GND | - | GND | - |
| 14 | 0 | A12 | A^12 | B8 | B^4 | B6 | B^3 |
| 15 | 0 | A13 | A^13 | B10 | B^5 | B4 | B^2 |
| 16 | 0 | A14 | A^14 | B12 | B^6 | B2 | B^1 |
| 17 | 0 | A15 | A^15 | B14 | B^7 | B0 | B^0 |
| 18 | 0 | CLK1/I | - | CLK1/I | - | CLK1/I | - |
| 19 | 1 | CLK2/I | - | CLK2/I | - | CLK2/I | - |
| 20 | 1 | B0 | B^0 | C0 | C^0 | C0 | C^0 |
| 21 | 1 | B1 | B^1 | C2 | C^1 | C1 | C^1 |
| 22 | 1 | B2 | B^2 | C4 | C^2 | C2 | C^2 |
| 23 | 1 | B3 | B^3 | C6 | C^3 | C4 | C^3 |
| 24 | 1 | B4 | B^4 | C8 | C^4 | C6 | C^4 |
| 25 | - | TMS | - | TMS | - | TMS | - |
| 26 | 1 | B5 | B^5 | C10 | C^5 | C8 | C^5 |
| 27 | 1 | B6 | B^6 | C12 | C^6 | C10 | C^6 |
| 28 | 1 | B7 | B^7 | C14 | C^7 | C11 | C^7 |
| 29 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| 30 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 31 | 1 | B8 | B^8 | D0 | D^0 | D15 | D^7 |
| 32 | 1 | B9 | B^9 | D2 | D^1 | D12 | D^6 |

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 62 | 1 | E10 | E^8 |
| 63 | 1 | E12 | E^9 |
| 64 | 1 | E14 | E^11 |
| 65 | 1 | GND | - |
| 66 | 1 | TMS | - |
| 67 | 1 | VCCO (Bank 1) | - |
| 68 | 1 | F0 | F^0 |
| 69 | 1 | F1 | F^1 |
| 70 | 1 | F2 | F^2 |
| 71 | 1 | F4 | F^3 |
| 72 | 1 | F5 | F^4 |
| 73 | 1 | F6 | F^5 |
| 74 | 1 | GND (Bank 1) | - |
| 75 | 1 | F8 | F^6 |
| 76 | 1 | F9 | F^7 |
| 77 | 1 | F10 | F^8 |
| 78 | 1 | F12 | F^9 |
| 79 | 1 | F13 | F^10 |
| 80 | 1 | F14 | F^11 |
| 81 | 1 | VCCO (Bank 1) | - |
| 82 | 1 | G14 | G^11 |
| 83 | 1 | G13 | G^10 |
| 84 | 1 | G12 | G^9 |
| 85 | 1 | G10 | G^8 |
| 86 | 1 | G9 | G^7 |
| 87 | 1 | G8 | G^6 |
| 88 | 1 | GND (Bank 1) | - |
| 89 | 1 | G6 | G^5 |
| 90 | 1 | G5 | G^4 |
| 91 | 1 | G4 | G^3 |
| 92 | 1 | G2 | G^2 |
| 93 | 1 | G0 | G^0 |
| 94 | 1 | VCCO (Bank 1) | - |
| 95 | 1 | TDO | - |
| 96 | 1 | VCC | - |
| 97 | 1 | GND | - |
| 98 | 1 | H14 | H^11 |
| 99 | 1 | H13 | H^10 |
| 100 | 1 | H12 | H^9 |
| 101 | 1 | H10 | H^8 |
| 102 | 1 | H9 | H^7 |
| 103 | 1 | H8 | H^6 |
| 104 | 1 | GND (Bank 1) | - |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| E7 | 0 | NC | - | B1 | B^1 | F8 | F^4 | D12 | D^3 |
| A3 | 0 | B0 | B^0 | B2 | B^2 | B0 | B^0 | B0 | B^0 |
| F7 | 0 | B2 | B^1 | B4 | B^3 | B2 | B^1 | B2 | B^1 |
| B4 | 0 | B4 | B^2 | B6 | B^4 | B4 | B^2 | B4 | B^2 |
| C5 | 0 | B6 | B^3 | B8 | B^5 | B6 | B^3 | B6 | B^3 |
| A2 | 0 | B8 | B^4 | B9 | B^6 | B8 | B^4 | B8 | B^4 |
| E6 | 0 | B10 | B^5 | B10 | B^7 | B10 | B^5 | B10 | B^5 |
| B3 | 0 | B12 | B^6 | B12 | B^8 | B12 | B^6 | B12 | B^6 |
| C4 | 0 | B14 | B^7 | B14 | B^9 | B14 | B^7 | B14 | B^7 |
| D4 | 0 | NC | - | NC | - | D10 | D^5 | F0 | F^0 |
| E5 | 0 | NC | - | NC | - | D8 | D^4 | F2 | F^1 |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| - | - | - | - | - | - | GND | - | GND | - |
| - | 0 | - | - | - | - | GND (Bank 0) | - | GND (Bank 0) | - |

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

**ispMACH 4000C (1.8V) Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4128C | LC4128C-27T128C | 128 | 1.8 | 2.7 | TQFP | 128 | 92 | C |
| | LC4128C-5T128C | 128 | 1.8 | 5 | TQFP | 128 | 92 | C |
| | LC4128C-75T128C | 128 | 1.8 | 7.5 | TQFP | 128 | 92 | C |
| | LC4128C-27T100C | 128 | 1.8 | 2.7 | TQFP | 100 | 64 | C |
| | LC4128C-5T100C | 128 | 1.8 | 5 | TQFP | 100 | 64 | C |
| | LC4128C-75T100C | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | C |
| LC4256C | LC4256C-3FT256AC | 256 | 1.8 | 3 | ftBGA | 256 | 128 | C |
| | LC4256C-5FT256AC | 256 | 1.8 | 5 | ftBGA | 256 | 128 | C |
| | LC4256C-75FT256AC | 256 | 1.8 | 7.5 | ftBGA | 256 | 128 | C |
| | LC4256C-3FT256BC | 256 | 1.8 | 3 | ftBGA | 256 | 160 | C |
| | LC4256C-5FT256BC | 256 | 1.8 | 5 | ftBGA | 256 | 160 | C |
| | LC4256C-75FT256BC | 256 | 1.8 | 7.5 | ftBGA | 256 | 160 | C |
| | LC4256C-3F256AC[1] | 256 | 1.8 | 3 | fpBGA | 256 | 128 | C |
| | LC4256C-5F256AC[1] | 256 | 1.8 | 5 | fpBGA | 256 | 128 | C |
| | LC4256C-75F256AC[1] | 256 | 1.8 | 7.5 | fpBGA | 256 | 128 | C |
| | LC4256C-3F256BC[1] | 256 | 1.8 | 3 | fpBGA | 256 | 160 | C |
| | LC4256C-5F256BC[1] | 256 | 1.8 | 5 | fpBGA | 256 | 160 | C |
| | LC4256C-75F256BC[1] | 256 | 1.8 | 7.5 | fpBGA | 256 | 160 | C |
| | LC4256C-3T176C | 256 | 1.8 | 3 | TQFP | 176 | 128 | C |
| | LC4256C-5T176C | 256 | 1.8 | 5 | TQFP | 176 | 128 | C |
| | LC4256C-75T176C | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | C |
| | LC4256C-3T100C | 256 | 1.8 | 3 | TQFP | 100 | 64 | C |
| | LC4256C-5T100C | 256 | 1.8 | 5 | TQFP | 100 | 64 | C |
| | LC4256C-75T100C | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | C |
| LC4384C | LC4384C-35FT256C | 384 | 1.8 | 3.5 | ftBGA | 256 | 192 | C |
| | LC4384C-5FT256C | 384 | 1.8 | 5 | ftBGA | 256 | 192 | C |
| | LC4384C-75FT256C | 384 | 1.8 | 7.5 | ftBGA | 256 | 192 | C |
| | LC4384C-35F256C[1] | 384 | 1.8 | 3.5 | fpBGA | 256 | 192 | C |
| | LC4384C-5F256C[1] | 384 | 1.8 | 5 | fpBGA | 256 | 192 | C |
| | LC4384C-75F256C[1] | 384 | 1.8 | 7.5 | fpBGA | 256 | 192 | C |
| | LC4384C-35T176C | 384 | 1.8 | 3.5 | TQFP | 176 | 128 | C |
| | LC4384C-5T176C | 384 | 1.8 | 5 | TQFP | 176 | 128 | C |
| | LC4384C-75T176C | 384 | 1.8 | 7.5 | TQFP | 176 | 128 | C |
| LC4512C | LC4512C-35FT256C | 512 | 1.8 | 3.5 | ftBGA | 256 | 208 | C |
| | LC4512C-5FT256C | 512 | 1.8 | 5 | ftBGA | 256 | 208 | C |
| | LC4512C-75FT256C | 512 | 1.8 | 7.5 | ftBGA | 256 | 208 | C |
| | LC4512C-35F256C[1] | 512 | 1.8 | 3.5 | fpBGA | 256 | 208 | C |
| | LC4512C-5F256C[1] | 512 | 1.8 | 5 | fpBGA | 256 | 208 | C |
| | LC4512C-75F256C[1] | 512 | 1.8 | 7.5 | fpBGA | 256 | 208 | C |
| | LC4512C-35T176C | 512 | 1.8 | 3.5 | TQFP | 176 | 128 | C |
| | LC4512C-5T176C | 512 | 1.8 | 5 | TQFP | 176 | 128 | C |
| | LC4512C-75T176C | 512 | 1.8 | 7.5 | TQFP | 176 | 128 | C |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000B (2.5V) Industrial Devices**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032B | LC4032B-5T48I | 32 | 2.5 | 5 | TQFP | 48 | 32 | I |
| | LC4032B-75T48I | 32 | 2.5 | 7.5 | TQFP | 48 | 32 | I |
| | LC4032B-10T48I | 32 | 2.5 | 10 | TQFP | 48 | 32 | I |
| | LC4032B-5T44I | 32 | 2.5 | 5 | TQFP | 44 | 30 | I |
| | LC4032B-75T44I | 32 | 2.5 | 7.5 | TQFP | 44 | 30 | I |
| | LC4032B-10T44I | 32 | 2.5 | 10 | TQFP | 44 | 30 | I |
| LC4064B | LC4064B-5T100I | 64 | 2.5 | 5 | TQFP | 100 | 64 | I |
| | LC4064B-75T100I | 64 | 2.5 | 7.5 | TQFP | 100 | 64 | I |
| | LC4064B-10T100I | 64 | 2.5 | 10 | TQFP | 100 | 64 | I |
| | LC4064B-5T48I | 64 | 2.5 | 5 | TQFP | 48 | 32 | I |
| | LC4064B-75T48I | 64 | 2.5 | 7.5 | TQFP | 48 | 32 | I |
| | LC4064B-10T48I | 64 | 2.5 | 10 | TQFP | 48 | 32 | I |
| | LC4064B-5T44I | 64 | 2.5 | 5 | TQFP | 44 | 30 | I |
| | LC4064B-75T44I | 64 | 2.5 | 7.5 | TQFP | 44 | 30 | I |
| | LC4064B-10T44I | 64 | 2.5 | 10 | TQFP | 44 | 30 | I |
| LC4128B | LC4128B-5T128I | 128 | 2.5 | 5 | TQFP | 128 | 92 | I |
| | LC4128B-75T128I | 128 | 2.5 | 7.5 | TQFP | 128 | 92 | I |
| | LC4128B-10T128I | 128 | 2.5 | 10 | TQFP | 128 | 92 | I |
| | LC4128B-5T100I | 128 | 2.5 | 5 | TQFP | 100 | 64 | I |
| | LC4128B-75T100I | 128 | 2.5 | 7.5 | TQFP | 100 | 64 | I |
| | LC4128B-10T100I | 128 | 2.5 | 10 | TQFP | 100 | 64 | I |
| LC4256B | LC4256B-5FT256AI | 256 | 2.5 | 5 | ftBGA | 256 | 128 | I |
| | LC4256B-75FT256AI | 256 | 2.5 | 7.5 | ftBGA | 256 | 128 | I |
| | LC4256B-10FT256AI | 256 | 2.5 | 10 | ftBGA | 256 | 128 | I |
| | LC4256B-5FT256BI | 256 | 2.5 | 5 | ftBGA | 256 | 160 | I |
| | LC4256B-75FT256BI | 256 | 2.5 | 7.5 | ftBGA | 256 | 160 | I |
| | LC4256B-10FT256BI | 256 | 2.5 | 10 | ftBGA | 256 | 160 | I |
| | LC4256B-5F256AI[1] | 256 | 2.5 | 5 | fpBGA | 256 | 128 | I |
| | LC4256B-75F256AI[1] | 256 | 2.5 | 7.5 | fpBGA | 256 | 128 | I |
| | LC4256B-10F256AI[1] | 256 | 2.5 | 10 | fpBGA | 256 | 128 | I |
| | LC4256B-5F256BI[1] | 256 | 2.5 | 5 | fpBGA | 256 | 160 | I |
| | LC4256B-75F256BI[1] | 256 | 2.5 | 7.5 | fpBGA | 256 | 160 | I |
| | LC4256B-10F256BI[1] | 256 | 2.5 | 10 | fpBGA | 256 | 160 | I |
| | LC4256B-5T176I | 256 | 2.5 | 5 | TQFP | 176 | 128 | I |
| | LC4256B-75T176I | 256 | 2.5 | 7.5 | TQFP | 176 | 128 | I |
| | LC4256B-10T176I | 256 | 2.5 | 10 | TQFP | 176 | 128 | I |
| | LC4256B-5T100I | 256 | 2.5 | 5 | TQFP | 100 | 64 | I |
| | LC4256B-75T100I | 256 | 2.5 | 7.5 | TQFP | 100 | 64 | I |
| | LC4256B-10T100I | 256 | 2.5 | 10 | TQFP | 100 | 64 | I |

**ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4384B | LC4384B-35FTN256C | 384 | 2.5 | 3.5 | Lead-Free ftBGA | 256 | 192 | C |
| | LC4384B-5FTN256C | 384 | 2.5 | 5 | Lead-Free ftBGA | 256 | 192 | C |
| | LC4384B-75FTN256C | 384 | 2.5 | 7.5 | Lead-Free ftBGA | 256 | 192 | C |
| | LC4384B-35FN256C[1] | 384 | 2.5 | 3.5 | Lead-Free fpBGA | 256 | 192 | C |
| | LC4384B-5FN256C[1] | 384 | 2.5 | 5 | Lead-Free fpBGA | 256 | 192 | C |
| | LC4384B-75FN256C[1] | 384 | 2.5 | 7.5 | Lead-Free fpBGA | 256 | 192 | C |
| | LC4384B-35TN176C | 384 | 2.5 | 3.5 | Lead-Free TQFP | 176 | 128 | C |
| | LC4384B-5TN176C | 384 | 2.5 | 5 | Lead-Free TQFP | 176 | 128 | C |
| | LC4384B-75TN176C | 384 | 2.5 | 7.5 | Lead-Free TQFP | 176 | 128 | C |
| LC4512B | LC4512B-35FTN256C | 512 | 2.5 | 3.5 | Lead-Free ftBGA | 256 | 208 | C |
| | LC4512B-5FTN256C | 512 | 2.5 | 5 | Lead-Free ftBGA | 256 | 208 | C |
| | LC4512B-75FTN256C | 512 | 2.5 | 7.5 | Lead-Free ftBGA | 256 | 208 | C |
| | LC4512B-35FN256C[1] | 512 | 2.5 | 3.5 | Lead-Free fpBGA | 256 | 208 | C |
| | LC4512B-5FN256C[1] | 512 | 2.5 | 5 | Lead-Free fpBGA | 256 | 208 | C |
| | LC4512B-75FN256C[1] | 512 | 2.5 | 7.5 | Lead-Free fpBGA | 256 | 208 | C |
| | LC4512B-35TN176C | 512 | 2.5 | 3.5 | Lead-Free TQFP | 176 | 128 | C |
| | LC4512B-5TN176C | 512 | 2.5 | 5 | Lead-Free TQFP | 176 | 128 | C |
| | LC4512B-75TN176C | 512 | 2.5 | 7.5 | Lead-Free TQFP | 176 | 128 | C |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000B (2.5V) Lead-Free Industrial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032B | LC4032B-5TN48I | 32 | 2.5 | 5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032B-75TN48I | 32 | 2.5 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032B-10TN48I | 32 | 2.5 | 10 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032B-5TN44I | 32 | 2.5 | 5 | Lead-Free TQFP | 44 | 30 | I |
| | LC4032B-75TN44I | 32 | 2.5 | 7.5 | Lead-Free TQFP | 44 | 30 | I |
| | LC4032B-10TN44I | 32 | 2.5 | 10 | Lead-Free TQFP | 44 | 30 | I |
| LC4064B | LC4064B-5TN100I | 64 | 2.5 | 5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064B-75TN100I | 64 | 2.5 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064B-10TN100I | 64 | 2.5 | 10 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064B-5TN48I | 64 | 2.5 | 5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064B-75TN48I | 64 | 2.5 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064B-10TN48I | 64 | 2.5 | 10 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064B-5TN44I | 64 | 2.5 | 5 | Lead-Free TQFP | 44 | 30 | I |
| | LC4064B-75TN44I | 64 | 2.5 | 7.5 | Lead-Free TQFP | 44 | 30 | I |
| | LC4064B-10TN44I | 64 | 2.5 | 10 | Lead-Free TQFP | 44 | 30 | I |

**ispMACH 4000V (3.3V) Lead-Free Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032V | LC4032V-25TN48C | 32 | 3.3 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032V-5TN48C | 32 | 3.3 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032V-75TN48C | 32 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032V-25TN44C | 32 | 3.3 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4032V-5TN44C | 32 | 3.3 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4032V-75TN44C | 32 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | C |
| LC4064V | LC4064V-25TN100C | 64 | 3.3 | 2.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064V-5TN100C | 64 | 3.3 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064V-75TN100C | 64 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064V-25TN48C | 64 | 3.3 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064V-5TN48C | 64 | 3.3 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064V-75TN48C | 64 | 3.3 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064V-25TN44C | 64 | 3.3 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064V-5TN44C | 64 | 3.3 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064V-75TN44C | 64 | 3.3 | 7.5 | Lead-free TQFP | 44 | 30 | C |
| LC4128V | LC4128V-27TN144C | 128 | 3.3 | 2.7 | Lead-free TQFP | 144 | 96 | C |
| | LC4128V-5TN144C | 128 | 3.3 | 5 | Lead-free TQFP | 144 | 96 | C |
| | LC4128V-75TN144C | 128 | 3.3 | 7.5 | Lead-free TQFP | 144 | 96 | C |
| | LC4128V-27TN128C | 128 | 3.3 | 2.7 | Lead-free TQFP | 128 | 92 | C |
| | LC4128V-5TN128C | 128 | 3.3 | 5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128V-75TN128C | 128 | 3.3 | 7.5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128V-27TN100C | 128 | 3.3 | 2.7 | Lead-free TQFP | 100 | 64 | C |
| | LC4128V-5TN100C | 128 | 3.3 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4128V-75TN100C | 128 | 3.3 | 7.5 | Lead-free TQFP | 100 | 64 | C |