Lattice Semiconductor Corporation - LC4256V-10TN100I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256v-10tn100i

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator

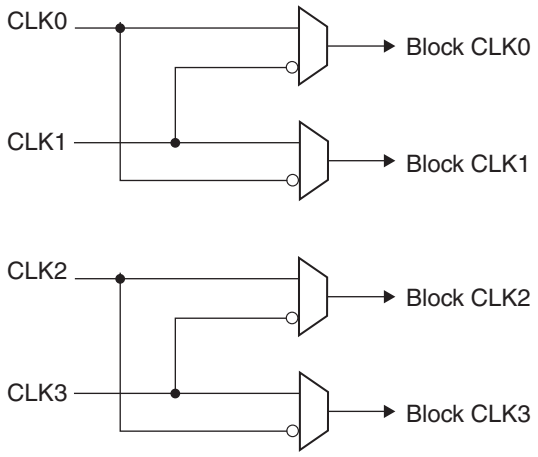


Table 10. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

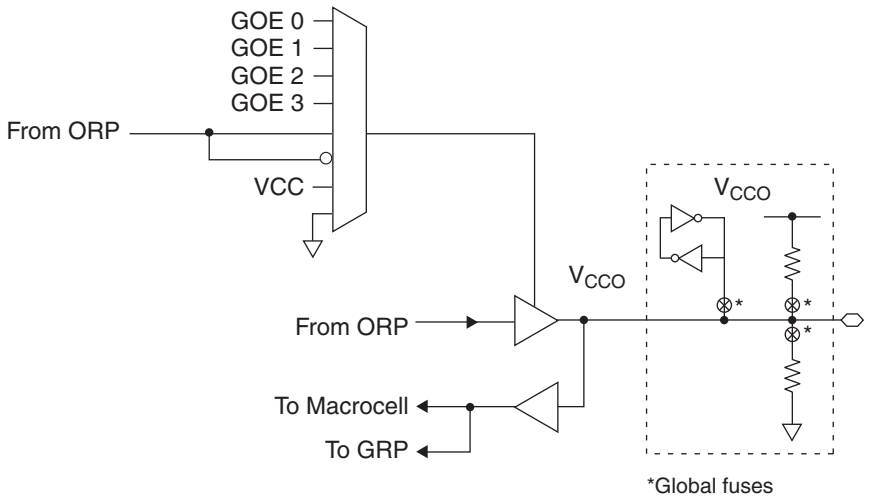
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}[4]	Standby Power Supply Current	Vcc = 3.3V	—	13	—	mA
		Vcc = 2.5V	—	13	—	mA
		Vcc = 1.8V	—	3	—	mA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. T_A = 25°C

Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22	—	µA
ispMACH 4064ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37	—	µA
ispMACH 4128ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

ispMACH 4000V/B/C External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t_R	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t_{CW}	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t_{WIR}	Input register clock width, high or low	2.2	—	2.8	—	4.0		ns
f_{MAX}[4]	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{GPTOE}	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
t_{PTOE}	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

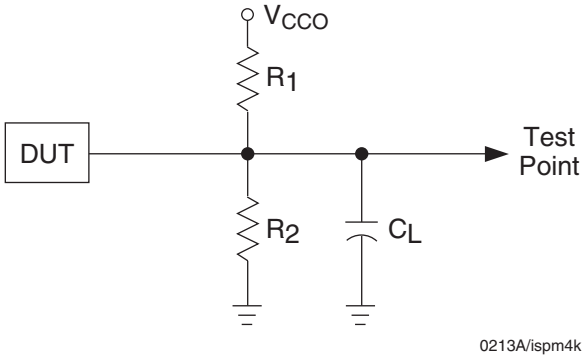


Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4000V/B/C/Z Power Supply and NC Connections[1]

Signal	44-pin TQFP[2]	48-pin TQFP[2]	56-ball csBGA[3]	100-pin TQFP[2]	128-pin TQFP[2]
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	**4032Z**: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3	P12	P^3
85	1	D2	D^2	H4	H^2	P10	P^2
86	1	D1	D^1	H2	H^1	P6	P^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	P^0
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^0
92	0	A1	A^1	A2	A^1	A6	A^1
93	0	A2	A^2	A4	A^2	A10	A^2
94	0	A3	A^3	A6	A^3	A12	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4	B2	B^0
98	0	A5	A^5	A10	A^5	B6	B^1
99	0	A6	A^6	A12	A^6	B10	B^2
100	0	A7	A^7	A14	A^7	B12	B^3

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
105	1	VCCO (Bank 1)	-
106	1	H6	H^5
107	1	H5	H^4
108	1	H4	H^3
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^3
120	0	A5	A^4
121	0	A6	A^5
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A^6
125	0	A9	A^7
126	0	A10	A^8
127	0	A12	A^9
128	0	A14	A^11

ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	GND	-	GND	-	GND	-
B2	-	TDI	-	TDI	-	TDI	-
C1	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
C3	0	NC	-	B0	B^0	C12	C^6
C2	0	A8	A^8	B1	B^1	C10	C^5
D1	0	A9	A^9	B2	B^2	C8	C^4
D3	0	A10	A^10	B4	B^3	C6	C^3
D2	0	A11	A^11	B5	B^4	C4	C^2
E1	0	NC		B6	B^5	C2	C^1
E2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-

ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

		ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
Ball Number	Bank Number	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
D13	1	D10	D^10	G4	G^3	N6	N^3
D14	1	D9	D^9	G2	G^2	N8	N^4
D12	1	D8	D^8	G1	G^1	N10	N^5
C14	1	I	-	G0	G^0	N12	N^6
C13	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B14	-	TDO	-	TDO	-	TDO	-
A14	-	VCC	-	VCC	-	VCC	-
A13	-	GND	-	GND	-	GND	-
B13	1	NC	-	H14	H^11	O12	O^6
A12	1	I	-	H13	H^10	O10	O^5
C12	1	D7	D^7	H12	H^9	O8	O^4
B12	1	D6	D^6	H10	H^8	O6	O^3
A11	1	D5	D^5	H9	H^7	O4	O^2
C11	1	D4	D^4	H8	H^6	O2	O^1
B11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B10	1	NC	-	H6	H^5	P12	P^6
C10	1	NC	-	H5	H^4	P10	P^5
B9	1	D3	D^3	H4	H^3	P8	P^4
A9	1	D2	D^2	H2	H^2	P6	P^3
C9	1	D1	D^1	H1	H^1	P4	P^2
A8	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/GOE1	P^1
B8	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
C8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
B7	-	VCC	-	VCC	-	VCC	-
A7	0	NC[1]	-	NC[1]	-	I[1]	-
C7	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^1
A6	0	A1	A^1	A1	A^1	A4	A^2
B6	0	A2	A^2	A2	A^2	A6	A^3
C6	0	A3	A^3	A4	A^3	A8	A^4
B5	0	NC	-	A5	A^4	A10	A^5
A5	0	NC	-	A6	A^5	A12	A^6
C5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
A4	0	NC	-	A8	A^6	B2	B^1
C4	0	A4	A^4	A9	A^7	B4	B^2
A3	0	A5	A^5	A10	A^8	B6	B^3
B3	0	A6	A^6	A12	A^9	B8	B^4
A2	0	A7	A^7	A13	A^10	B10	B^5
A1	0	NC	-	A14	A^11	B12	B^6

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
4	0	B0	B^0	C12	C^6
5	0	B1	B^1	C10	C^5
6	0	B2	B^2	C8	C^4
7	0	B4	B^3	C6	C^3
8	0	B5	B^4	C4	C^2
9	0	B6	B^5	C2	C^1
10	0	GND (Bank 0)	-	GND (Bank 0)	-
11	0	B8	B^6	D14	D^7
12	0	B9	B^7	D12	D^6
13	0	B10	B^8	D10	D^5
14	0	B12	B^9	D8	D^4
15	0	B13	B^10	D6	D^3
16	0	B14	B^11	D4	D^2
17	-	NC[2]	-	I[2]	-
18	0	GND (Bank 0)[1]	-	NC[1]	-
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
20	0	NC[2]	-	I[2]	-
21	0	C14	C^11	E2	E^1
22	0	C13	C^10	E4	E^2
23	0	C12	C^9	E6	E^3
24	0	C10	C^8	E8	E^4
25	0	C9	C^7	E10	E^5
26	0	C8	C^6	E12	E^6
27	0	GND (Bank 0)	-	GND (Bank 0)	-
28	0	C6	C^5	F2	F^1
29	0	C5	C^4	F4	F^2
30	0	C4	C^3	F6	F^3
31	0	C2	C^2	F8	F^4
32	0	C1	C^1	F10	F^5
33	0	C0	C^0	F12	F^6
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
35	-	TCK	-	TCK	-
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	0	NC[2]	-	I[2]	-
39	0	D14	D^11	G12	G^6
40	0	D13	D^10	G10	G^5
41	0	D12	D^9	G8	G^4
42	0	D10	D^8	G6	G^3

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D^7	G4	G^2
44	0	D8	D^6	G2	G^1
45	0	NC[2]	-	I[2]	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D^5	H12	H^6
49	0	D5	D^4	H10	H^5
50	0	D4	D^3	H8	H^4
51	0	D2	D^2	H6	H^3
52	0	D1	D^1	H4	H^2
53	0	D0	D^0	H2	H^1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E^0	I2	I^1
59	1	E1	E^1	I4	I^2
60	1	E2	E^2	I6	I^3
61	1	E4	E^3	I8	I^4
62	1	E5	E^4	I10	I^5
63	1	E6	E^5	I12	I^6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E^6	J2	J^1
67	1	E9	E^7	J4	J^2
68	1	E10	E^8	J6	J^3
69	1	E12	E^9	J8	J^4
70	1	E13	E^10	J10	J^5
71	1	E14	E^11	J12	J^6
72	1	NC[2]	-	I[2]	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F^0	K12	K^6
77	1	F1	F^1	K10	K^5
78	1	F2	F^2	K8	K^4
79	1	F4	F^3	K6	K^3
80	1	F5	F^4	K4	K^2
81	1	F6	F^5	K2	K^1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F^6	L14	L^7
84	1	F9	F^7	L12	L^6
85	1	F10	F^8	L10	L^5

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C^7	C14	C^9	C14	C^7	C14	C^7
F5	0	C12	C^6	C12	C^8	C12	C^6	C12	C^6
D3	0	C10	C^5	C10	C^7	C10	C^5	C10	C^5
C1	0	C8	C^4	C9	C^6	C8	C^4	C8	C^4
C2	0	C6	C^3	C8	C^5	C6	C^3	C6	C^3
E3	0	C4	C^2	C6	C^4	C4	C^2	C4	C^2
D2	0	C2	C^1	C4	C^3	C2	C^1	C2	C^1
F6	0	C0	C^0	C2	C^2	C0	C^0	C0	C^0
D1	0	NC	-	C1	C^1	F6	F^3	H0	H^0
E2	0	NC	-	C0	C^0	F4	F^2	H4	H^1
E4	0	NC	-	NC	-	D6	D^3	F4	F^2
G5	0	NC	-	NC	-	D4	D^2	F6	F^3
E1	0	NC	-	NC	-	NC	-	F8	F^4
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F^5
F1	0	NC	-	NC	-	D2	D^1	F12	F^6
G1	0	NC	-	NC	-	D0	D^0	F14	F^7
G6	0	NC	-	D14	D^9	F2	F^1	H8	H^2
G4	0	NC	-	D12	D^8	F0	F^0	H12	H^3
H6	0	D14	D^7	D10	D^7	E14	E^7	G14	G^7
G3	0	D12	D^6	D9	D^6	E12	E^6	G12	G^6
H5	0	D10	D^5	D8	D^5	E10	E^5	G10	G^5
G2	0	D8	D^4	D6	D^4	E8	E^4	G8	G^4
H1	0	D6	D^3	D4	D^3	E6	E^3	G6	G^3
H2	0	D4	D^2	D2	D^2	E4	E^2	G4	G^2
H3	0	D2	D^1	D1	D^1	E2	E^1	G2	G^1
H4	0	D0	D^0	D0	D^0	E0	E^0	G0	G^0
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E^0	E0	E^0	H0	H^0	J0	J^0
J3	0	E2	E^1	E1	E^1	H2	H^1	J2	J^1
J2	0	E4	E^2	E2	E^2	H4	H^2	J4	J^2
J1	0	E6	E^3	E4	E^3	H6	H^3	J6	J^3
K1	0	E8	E^4	E6	E^4	H8	H^4	J8	J^4
J5	0	E10	E^5	E8	E^5	H10	H^5	J10	J^5
K2	0	E12	E^6	E9	E^6	H12	H^6	J12	J^6

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L^1
T5	0	NC	-	NC	-	I2	I^1	L8	L^2
R6	0	NC	-	NC	-	I0	I^0	L12	L^3
T6	0	NC	-	H14	H^9	G12	G^6	M8	M^2
N7	0	NC	-	H12	H^8	G14	G^7	M12	M^3
P7	0	H14	H^7	H10	H^7	L14	L^7	P14	P^7
R7	0	H12	H^6	H9	H^6	L12	L^6	P12	P^6
L8	0	H10	H^5	H8	H^5	L10	L^5	P10	P^5
T7	0	H8	H^4	H6	H^4	L8	L^4	P8	P^4
M8	0	H6	H^3	H4	H^3	L6	L^3	P6	P^3
N8	0	H4	H^2	H2	H^2	L4	L^2	P4	P^2
R8	0	H2	H^1	H1	H^1	L2	L^1	P2	P^1
P8	0	H0	H^0	H0	H^0	L0	L^0	P0	P^0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I^0	I0	I^0	M0	M^0	AX0	AX^0
R9	1	I2	I^1	I1	I^1	M2	M^1	AX2	AX^1
T9	1	I4	I^2	I2	I^2	M4	M^2	AX4	AX^2
T10	1	I6	I^3	I4	I^3	M6	M^3	AX6	AX^3
R10	1	I8	I^4	I6	I^4	M8	M^4	AX8	AX^4
M9	1	I10	I^5	I8	I^5	M10	M^5	AX10	AX^5
P10	1	I12	I^6	I9	I^6	M12	M^6	AX12	AX^6
L9	1	I14	I^7	I10	I^7	M14	M^7	AX14	AX^7
N10	1	NC	-	I12	I^8	BX14	BX^7	DX0	DX^0
T11	1	NC	-	I14	I^9	BX12	BX^6	DX4	DX^1
R11	1	NC	-	NC	-	P0	P^0	EX0	EX^0
T12	1	NC	-	NC	-	P2	P^1	EX4	EX^1
N12	1	NC	-	NC	-	NC	-	EX8	EX^2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX^3
T13	1	NC	-	J0	J^0	BX10	BX^5	DX8	DX^2
P12	1	NC	-	J1	J^1	BX8	BX^4	DX12	DX^3
M10	1	J0	J^0	J2	J^2	N0	N^0	BX0	BX^0
R13	1	J2	J^1	J4	J^3	N2	N^1	BX2	BX^1
L10	1	J4	J^2	J6	J^4	N4	N^2	BX4	BX^2
T14	1	J6	J^3	J8	J^5	N6	N^3	BX6	BX^3
M11	1	J8	J^4	J9	J^6	N8	N^4	BX8	BX^4

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI[1]	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI[1]	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI[1]	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI[1]	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI[1]	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI[1]	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C[1]	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C[1]	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C[1]	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI[1]	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI[1]	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI[1]	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI[1]	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI[1]	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI[1]	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
	LC4256V-10T100I	256	3.3	10	TQFP	100	64	I
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I[1]	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I[1]	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I[1]	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I[1]	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I[1]	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I[1]	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
	LC4064B-75TN44C	64	2.5	7.5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC[1]	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC[1]	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC[1]	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC[1]	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC[1]	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC[1]	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
	LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C
	LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C