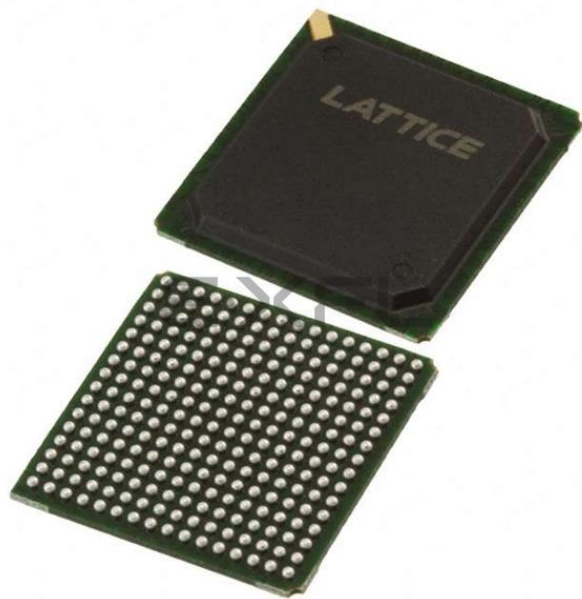




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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

|                                 |                                                                                                                                                                         |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                                                                |
| Programmable Type               | In System Programmable                                                                                                                                                  |
| Delay Time tpd(1) Max           | 7.5 ns                                                                                                                                                                  |
| Voltage Supply - Internal       | 3V ~ 3.6V                                                                                                                                                               |
| Number of Logic Elements/Blocks | 16                                                                                                                                                                      |
| Number of Macrocells            | 256                                                                                                                                                                     |
| Number of Gates                 | -                                                                                                                                                                       |
| Number of I/O                   | 160                                                                                                                                                                     |
| Operating Temperature           | -40°C ~ 105°C (Tj)                                                                                                                                                      |
| Mounting Type                   | Surface Mount                                                                                                                                                           |
| Package / Case                  | 256-BGA                                                                                                                                                                 |
| Supplier Device Package         | 256-FPBGA (17x17)                                                                                                                                                       |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256v-75fn256bi">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256v-75fn256bi</a> |

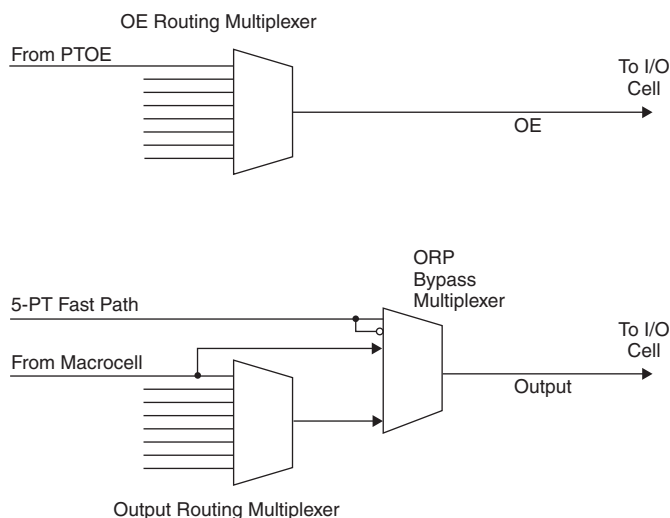
## Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

**Figure 7. ORP Slice**



## Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

**Table 6. ORP Combinations for I/O Blocks with 8 I/Os**

| I/O Cell | Available Macrocells                 |
|----------|--------------------------------------|
| I/O 0    | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/O 1    | M2, M3, M4, M5, M6, M7, M8, M9       |
| I/O 2    | M4, M5, M6, M7, M8, M9, M10, M11     |
| I/O 3    | M6, M7, M8, M9, M10, M11, M12, M13   |
| I/O 4    | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 5    | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 6    | M12, M13, M14, M15, M0, M1, M2, M3   |
| I/O 7    | M14, M15, M0, M1, M2, M3, M4, M5     |

**Table 7. ORP Combinations for I/O Blocks with 16 I/Os**

| I/O Cell | Available Macrocells                 |
|----------|--------------------------------------|
| I/O 0    | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/O 1    | M1, M2, M3, M4, M5, M6, M7, M8       |
| I/O 2    | M2, M3, M4, M5, M6, M7, M8, M9       |
| I/O 3    | M3, M4, M5, M6, M7, M8, M9, M10      |
| I/O 4    | M4, M5, M6, M7, M8, M9, M10, M11     |
| I/O 5    | M5, M6, M7, M8, M9, M10, M11, M12    |
| I/O 6    | M6, M7, M8, M9, M10, M11, M12, M13   |
| I/O 7    | M7, M8, M9, M10, M11, M12, M13, M14  |
| I/O 8    | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 9    | M9, M10, M11, M12, M13, M14, M15, M0 |
| I/O 10   | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 11   | M11, M12, M13, M14, M15, M0, M1, M2  |
| I/O 12   | M12, M13, M14, M15, M0, M1, M2, M3   |
| I/O 13   | M13, M14, M15, M0, M1, M2, M3, M4    |
| I/O 14   | M14, M15, M0, M1, M2, M3, M4, M5     |
| I/O 15   | M15, M0, M1, M2, M3, M4, M5, M6      |

**Table 8. ORP Combinations for I/O Blocks with 4 I/Os**

| I/O Cell | Available Macrocells                 |
|----------|--------------------------------------|
| I/O 0    | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/O 1    | M4, M5, M6, M7, M8, M9, M10, M11     |
| I/O 2    | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 3    | M12, M13, M14, M15, M0, M1, M2, M3   |

**Table 9. ORP Combinations for I/O Blocks with 10 I/Os**

| I/O Cell | Available Macrocells                 |
|----------|--------------------------------------|
| I/O 0    | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/O 1    | M2, M3, M4, M5, M6, M7, M8, M9       |
| I/O 2    | M4, M5, M6, M7, M8, M9, M10, M11     |
| I/O 3    | M6, M7, M8, M9, M10, M11, M12, M13   |
| I/O 4    | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 5    | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 6    | M12, M13, M14, M15, M0, M1, M2, M3   |
| I/O 7    | M14, M15, M0, M1, M2, M3, M4, M5     |
| I/O 8    | M2, M3, M4, M5, M6, M7, M8, M9       |
| I/O 9    | M10, M11, M12, M13, M14, M15, M0, M1 |

## I/O Recommended Operating Conditions

| Standard                          | $V_{CCO}$ (V) <sup>1</sup> |      |
|-----------------------------------|----------------------------|------|
|                                   | Min.                       | Max. |
| LVTTTL                            | 3.0                        | 3.6  |
| LVC MOS 3.3                       | 3.0                        | 3.6  |
| Extended LVC MOS 3.3 <sup>2</sup> | 2.7                        | 3.6  |
| LVC MOS 2.5                       | 2.3                        | 2.7  |
| LVC MOS 1.8                       | 1.65                       | 1.95 |
| PCI 3.3                           | 3.0                        | 3.6  |

1. Typical values for  $V_{CCO}$  are the average of the min. and max. values.

2. ispMACH 4000Z only.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

| Symbol                 | Parameter                                             | Condition                                                                     | Min.             | Typ. | Max.             | Units   |
|------------------------|-------------------------------------------------------|-------------------------------------------------------------------------------|------------------|------|------------------|---------|
| $I_{IL}, I_{IH}^{1,4}$ | Input Leakage Current (ispMACH 4000Z)                 | $0 \leq V_{IN} < V_{CCO}$                                                     | —                | 0.5  | 1                | $\mu A$ |
| $I_{IH}^1$             | Input High Leakage Current (ispMACH 4000Z)            | $V_{CCO} < V_{IN} \leq 5.5V$                                                  | —                | —    | 10               | $\mu A$ |
| $I_{IL}, I_{IH}^1$     | Input Leakage Current (ispMACH 4000V/B/C)             | $0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$                                  | —                | —    | 10               | $\mu A$ |
|                        |                                                       | $0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$                                  | —                | —    | 15               | $\mu A$ |
| $I_{IH}^{1,2}$         | Input High Leakage Current (ispMACH 4000V/B/C)        | $3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$<br>$3.0V \leq V_{CCO} \leq 3.6V$ | —                | —    | 20               | $\mu A$ |
|                        |                                                       | $3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$<br>$3.0V \leq V_{CCO} \leq 3.6V$ | —                | —    | 50               | $\mu A$ |
| $I_{PU}$               | I/O Weak Pull-up Resistor Current (ispMACH 4000Z)     | $0 \leq V_{IN} \leq 0.7V_{CCO}$                                               | -30              | —    | -150             | $\mu A$ |
|                        | I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C) | $0 \leq V_{IN} \leq 0.7V_{CCO}$                                               | -30              | —    | -200             | $\mu A$ |
| $I_{PD}$               | I/O Weak Pull-down Resistor Current                   | $V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$                                  | 30               | —    | 150              | $\mu A$ |
| $I_{BHLS}$             | Bus Hold Low Sustaining Current                       | $V_{IN} = V_{IL} (MAX)$                                                       | 30               | —    | —                | $\mu A$ |
| $I_{BHHS}$             | Bus Hold High Sustaining Current                      | $V_{IN} = 0.7 V_{CCO}$                                                        | -30              | —    | —                | $\mu A$ |
| $I_{BHLO}$             | Bus Hold Low Overdrive Current                        | $0V \leq V_{IN} \leq V_{BHT}$                                                 | —                | —    | 150              | $\mu A$ |
| $I_{BHHO}$             | Bus Hold High Overdrive Current                       | $V_{BHT} \leq V_{IN} \leq V_{CCO}$                                            | —                | —    | -150             | $\mu A$ |
| $V_{BHT}$              | Bus Hold Trip Points                                  | —                                                                             | $V_{CCO} * 0.35$ | —    | $V_{CCO} * 0.65$ | V       |
| $C_1$                  | I/O Capacitance <sup>3</sup>                          | $V_{CCO} = 3.3V, 2.5V, 1.8V$                                                  | —                | 8    | —                | pf      |
|                        |                                                       | $V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$                          | —                |      | —                |         |
| $C_2$                  | Clock Capacitance <sup>3</sup>                        | $V_{CCO} = 3.3V, 2.5V, 1.8V$                                                  | —                | 6    | —                | pf      |
|                        |                                                       | $V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$                          | —                |      | —                |         |
| $C_3$                  | Global Input Capacitance <sup>3</sup>                 | $V_{CCO} = 3.3V, 2.5V, 1.8V$                                                  | —                | 6    | —                | pf      |
|                        |                                                       | $V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$                          | —                |      | —                |         |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where  $3.0V \leq V_{CCO} \leq 3.6V$ .

3.  $T_A = 25^\circ C$ ,  $f = 1.0MHz$

4.  $I_{IH}$  excursions of up to 1.5 $\mu A$  maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

## ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

| Parameter                     | Description <sup>1, 2, 3</sup>                                                    | -35  |      | -37  |      | -42  |      | Units |
|-------------------------------|-----------------------------------------------------------------------------------|------|------|------|------|------|------|-------|
|                               |                                                                                   | Min. | Max. | Min. | Max. | Min. | Max. |       |
| t <sub>PD</sub>               | 5-PT bypass combinatorial propagation delay                                       | —    | 3.5  | —    | 3.7  | —    | 4.2  | ns    |
| t <sub>PD_MC</sub>            | 20-PT combinatorial propagation delay through macrocell                           | —    | 4.4  | —    | 4.7  | —    | 5.7  | ns    |
| t <sub>S</sub>                | GLB register setup time before clock                                              | 2.2  | —    | 2.5  | —    | 2.7  | —    | ns    |
| t <sub>ST</sub>               | GLB register setup time before clock with T-type register                         | 2.4  | —    | 2.7  | —    | 2.9  | —    | ns    |
| t <sub>SIR</sub>              | GLB register setup time before clock, input register path                         | 1.0  | —    | 1.1  | —    | 1.3  | —    | ns    |
| t <sub>SIRZ</sub>             | GLB register setup time before clock with zero hold                               | 2.0  | —    | 2.1  | —    | 2.6  | —    | ns    |
| t <sub>H</sub>                | GLB register hold time after clock                                                | 0.0  | —    | 0.0  | —    | 0.0  | —    | ns    |
| t <sub>HT</sub>               | GLB register hold time after clock with T-type register                           | 0.0  | —    | 0.0  | —    | 0.0  | —    | ns    |
| t <sub>HIR</sub>              | GLB register hold time after clock, input register path                           | 1.0  | —    | 1.0  | —    | 1.3  | —    | ns    |
| t <sub>HIRZ</sub>             | GLB register hold time after clock, input register path with zero hold            | 0.0  | —    | 0.0  | —    | 0.0  | —    | ns    |
| t <sub>CO</sub>               | GLB register clock-to-output delay                                                | —    | 3.0  | —    | 3.2  | —    | 3.5  | ns    |
| t <sub>R</sub>                | External reset pin to output delay                                                | —    | 5.0  | —    | 6.0  | —    | 7.3  | ns    |
| t <sub>RW</sub>               | External reset pulse duration                                                     | 1.5  | —    | 1.7  | —    | 2.0  | —    | ns    |
| t <sub>PTOE/DIS</sub>         | Input to output local product term output enable/disable                          | —    | 7.0  | —    | 8.0  | —    | 8.0  | ns    |
| t <sub>GPTOE/DIS</sub>        | Input to output global product term output enable/disable                         | —    | 6.5  | —    | 7.0  | —    | 8.0  | ns    |
| t <sub>GOE/DIS</sub>          | Global OE input to output enable/disable                                          | —    | 4.5  | —    | 4.5  | —    | 4.8  | ns    |
| t <sub>CW</sub>               | Global clock width, high or low                                                   | 1.0  | —    | 1.5  | —    | 1.8  | —    | ns    |
| t <sub>GW</sub>               | Global gate width low (for low transparent) or high (for high transparent)        | 1.0  | —    | 1.5  | —    | 1.8  | —    | ns    |
| t <sub>WIR</sub>              | Input register clock width, high or low                                           | 1.0  | —    | 1.5  | —    | 1.8  | —    | ns    |
| f <sub>MAX</sub> <sup>4</sup> | Clock frequency with internal feedback                                            | —    | 267  | —    | 250  | —    | 220  | MHz   |
| f <sub>MAX</sub> (Ext.)       | clock frequency with external feedback, [1 / (t <sub>S</sub> + t <sub>CO</sub> )] | —    | 192  | —    | 175  | —    | 161  | MHz   |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

## ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

| Parameter             | Description                                      | -2.5 |      | -2.7 |      | -3   |      | -3.5 |      | Units |
|-----------------------|--------------------------------------------------|------|------|------|------|------|------|------|------|-------|
| In/Out Delays         |                                                  |      |      |      |      |      |      |      |      |       |
| t <sub>IN</sub>       | Input Buffer Delay                               | —    | 0.60 | —    | 0.60 | —    | 0.70 | —    | 0.70 | ns    |
| t <sub>GOE</sub>      | Global OE Pin Delay                              | —    | 2.04 | —    | 2.54 | —    | 3.04 | —    | 3.54 | ns    |
| t <sub>GCLK_IN</sub>  | Global Clock Input Buffer Delay                  | —    | 0.78 | —    | 1.28 | —    | 1.28 | —    | 1.28 | ns    |
| t <sub>BUF</sub>      | Delay through Output Buffer                      | —    | 0.85 | —    | 0.85 | —    | 0.85 | —    | 0.85 | ns    |
| t <sub>EN</sub>       | Output Enable Time                               | —    | 0.96 | —    | 0.96 | —    | 0.96 | —    | 0.96 | ns    |
| t <sub>DIS</sub>      | Output Disable Time                              | —    | 0.96 | —    | 0.96 | —    | 0.96 | —    | 0.96 | ns    |
| Routing/GLB Delays    |                                                  |      |      |      |      |      |      |      |      |       |
| t <sub>ROUTE</sub>    | Delay through GRP                                | —    | 0.61 | —    | 0.81 | —    | 1.01 | —    | 1.01 | ns    |
| t <sub>MCELL</sub>    | Macrocell Delay                                  | —    | 0.45 | —    | 0.55 | —    | 0.55 | —    | 0.65 | ns    |
| t <sub>INREG</sub>    | Input Buffer to Macrocell Register Delay         | —    | 0.11 | —    | 0.31 | —    | 0.31 | —    | 0.31 | ns    |
| t <sub>FBK</sub>      | Internal Feedback Delay                          | —    | 0.00 | —    | 0.00 | —    | 0.00 | —    | 0.00 | ns    |
| t <sub>PDb</sub>      | 5-PT Bypass Propagation Delay                    | —    | 0.44 | —    | 0.44 | —    | 0.44 | —    | 0.94 | ns    |
| t <sub>PDi</sub>      | Macrocell Propagation Delay                      | —    | 0.64 | —    | 0.64 | —    | 0.64 | —    | 0.94 | ns    |
| Register/Latch Delays |                                                  |      |      |      |      |      |      |      |      |       |
| t <sub>S</sub>        | D-Register Setup Time (Global Clock)             | 0.92 | —    | 1.12 | —    | 1.02 | —    | 0.92 | —    | ns    |
| t <sub>S_PT</sub>     | D-Register Setup Time (Product Term Clock)       | 1.42 | —    | 1.32 | —    | 1.32 | —    | 1.32 | —    | ns    |
| t <sub>ST</sub>       | T-Register Setup Time (Global Clock)             | 1.12 | —    | 1.32 | —    | 1.22 | —    | 1.12 | —    | ns    |
| t <sub>ST_PT</sub>    | T-Register Setup Time (Product Term Clock)       | 1.42 | —    | 1.32 | —    | 1.32 | —    | 1.32 | —    | ns    |
| t <sub>H</sub>        | D-Register Hold Time                             | 0.88 | —    | 0.68 | —    | 0.98 | —    | 1.08 | —    | ns    |
| t <sub>HT</sub>       | T-Register Hold Time                             | 0.88 | —    | 0.68 | —    | 0.98 | —    | 1.08 | —    | ns    |
| t <sub>SIR</sub>      | D-Input Register Setup Time (Global Clock)       | 0.82 | —    | 1.37 | —    | 1.27 | —    | 1.27 | —    | ns    |
| t <sub>SIR_PT</sub>   | D-Input Register Setup Time (Product Term Clock) | 1.45 | —    | 1.45 | —    | 1.45 | —    | 1.45 | —    | ns    |
| t <sub>HIR</sub>      | D-Input Register Hold Time (Global Clock)        | 0.88 | —    | 0.63 | —    | 0.73 | —    | 0.73 | —    | ns    |
| t <sub>HIR_PT</sub>   | D-Input Register Hold Time (Product Term Clock)  | 0.88 | —    | 0.63 | —    | 0.73 | —    | 0.73 | —    | ns    |
| t <sub>COi</sub>      | Register Clock to Output/Feedback MUX Time       | —    | 0.52 | —    | 0.52 | —    | 0.52 | —    | 0.52 | ns    |
| t <sub>CES</sub>      | Clock Enable Setup Time                          | 2.25 | —    | 2.25 | —    | 2.25 | —    | 2.25 | —    | ns    |
| t <sub>CEH</sub>      | Clock Enable Hold Time                           | 1.88 | —    | 1.88 | —    | 1.88 | —    | 1.88 | —    | ns    |
| t <sub>SL</sub>       | Latch Setup Time (Global Clock)                  | 0.92 | —    | 1.12 | —    | 1.02 | —    | 0.92 | —    | ns    |
| t <sub>SL_PT</sub>    | Latch Setup Time (Product Term Clock)            | 1.42 | —    | 1.32 | —    | 1.32 | —    | 1.32 | —    | ns    |
| t <sub>HL</sub>       | Latch Hold Time                                  | 1.17 | —    | 1.17 | —    | 1.17 | —    | 1.17 | —    | ns    |
| t <sub>GOi</sub>      | Latch Gate to Output/Feedback MUX Time           | —    | 0.33 | —    | 0.33 | —    | 0.33 | —    | 0.33 | ns    |

**ispMACH 4000V/B/C Timing Adders<sup>1</sup> (Cont.)**

| Adder Type                        | Base Parameter                                            | Description                                | -5   |      | -75  |      | -10  |      | Units |
|-----------------------------------|-----------------------------------------------------------|--------------------------------------------|------|------|------|------|------|------|-------|
|                                   |                                                           |                                            | Min. | Max. | Min. | Max. | Min. | Max. |       |
| Optional Delay Adders             |                                                           |                                            |      |      |      |      |      |      |       |
| t <sub>INDIO</sub>                | t <sub>INREG</sub>                                        | Input register delay                       | —    | 1.00 | —    | 1.00 | —    | 1.00 | ns    |
| t <sub>EXP</sub>                  | t <sub>MCELL</sub>                                        | Product term expander delay                | —    | 0.33 | —    | 0.33 | —    | 0.33 | ns    |
| t <sub>ORP</sub>                  | —                                                         | Output routing pool delay                  | —    | 0.05 | —    | 0.05 | —    | 0.05 | ns    |
| t <sub>BLA</sub>                  | t <sub>ROUTE</sub>                                        | Additional block loading adder             | —    | 0.05 | —    | 0.05 | —    | 0.05 | ns    |
| t <sub>IOI</sub> Input Adjusters  |                                                           |                                            |      |      |      |      |      |      |       |
| LVTTTL_in                         | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVTTTL standard                      | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| LVC MOS33_in                      | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVC MOS 3.3 standard                 | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| LVC MOS25_in                      | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVC MOS 2.5 standard                 | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| LVC MOS18_in                      | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVC MOS 1.8 standard                 | —    | 0.00 | —    | 0.00 | —    | 0.00 | ns    |
| PCI_in                            | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using PCI compatible input                 | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| t <sub>IOO</sub> Output Adjusters |                                                           |                                            |      |      |      |      |      |      |       |
| LVTTTL_out                        | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as TTL buffer            | —    | 0.20 | —    | 0.20 | —    | 0.20 | ns    |
| LVC MOS33_out                     | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as 3.3V buffer           | —    | 0.20 | —    | 0.20 | —    | 0.20 | ns    |
| LVC MOS25_out                     | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as 2.5V buffer           | —    | 0.10 | —    | 0.10 | —    | 0.10 | ns    |
| LVC MOS18_out                     | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as 1.8V buffer           | —    | 0.00 | —    | 0.00 | —    | 0.00 | ns    |
| PCI_out                           | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as PCI compatible buffer | —    | 0.20 | —    | 0.20 | —    | 0.20 | ns    |
| Slow Slew                         | t <sub>BUF</sub> , t <sub>EN</sub>                        | Output configured for slow slew rate       | —    | 1.00 | —    | 1.00 | —    | 1.00 | ns    |

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

**ispMACH 4000Z Timing Adders <sup>1</sup>**

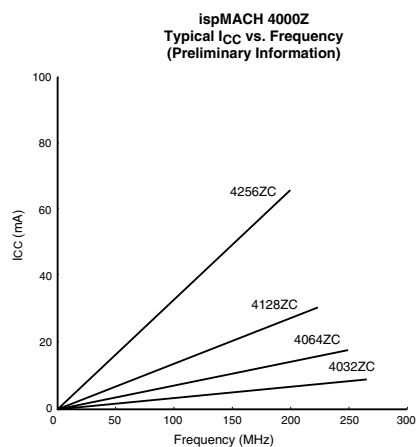
| Adder Type                        | Base Parameter                                            | Description                                | -35  |      | -37  |      | -42  |      | Units |
|-----------------------------------|-----------------------------------------------------------|--------------------------------------------|------|------|------|------|------|------|-------|
|                                   |                                                           |                                            | Min. | Max. | Min. | Max. | Min. | Max. |       |
| Optional Delay Adders             |                                                           |                                            |      |      |      |      |      |      |       |
| t <sub>INDIO</sub>                | t <sub>INREG</sub>                                        | Input register delay                       | —    | 1.00 | —    | 1.00 | —    | 1.30 | ns    |
| t <sub>EXP</sub>                  | t <sub>MCELL</sub>                                        | Product term expander delay                | —    | 0.40 | —    | 0.40 | —    | 0.45 | ns    |
| t <sub>ORP</sub>                  | —                                                         | Output routing pool delay                  | —    | 0.40 | —    | 0.40 | —    | 0.40 | ns    |
| t <sub>BLA</sub>                  | t <sub>ROUTE</sub>                                        | Additional block load-ing adder            | —    | 0.04 | —    | 0.05 | —    | 0.05 | ns    |
| t <sub>IOI</sub> Input Adjusters  |                                                           |                                            |      |      |      |      |      |      |       |
| LVTTTL_in                         | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVTTTL standard                      | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| LVC MOS33_in                      | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVC MOS 3.3 standard                 | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| LVC MOS25_in                      | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVC MOS 2.5 standard                 | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| LVC MOS18_in                      | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using LVC MOS 1.8 standard                 | —    | 0.00 | —    | 0.00 | —    | 0.00 | ns    |
| PCI_in                            | t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub> | Using PCI compatible input                 | —    | 0.60 | —    | 0.60 | —    | 0.60 | ns    |
| t <sub>IOO</sub> Output Adjusters |                                                           |                                            |      |      |      |      |      |      |       |
| LVTTTL_out                        | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as TTL buffer            | —    | 0.20 | —    | 0.20 | —    | 0.20 | ns    |
| LVC MOS33_out                     | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as 3.3V buffer           | —    | 0.20 | —    | 0.20 | —    | 0.20 | ns    |
| LVC MOS25_out                     | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as 2.5V buffer           | —    | 0.10 | —    | 0.10 | —    | 0.10 | ns    |
| LVC MOS18_out                     | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as 1.8V buffer           | —    | 0.00 | —    | 0.00 | —    | 0.00 | ns    |
| PCI_out                           | t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>     | Output configured as PCI compatible buffer | —    | 0.20 | —    | 0.20 | —    | 0.20 | ns    |
| Slow Slew                         | t <sub>BUF</sub> , t <sub>EN</sub>                        | Output configured for slow slew rate       | —    | 1.00 | —    | 1.00 | —    | 1.00 | ns    |

Note: Open drain timing is the same as corresponding LVC MOS timing.

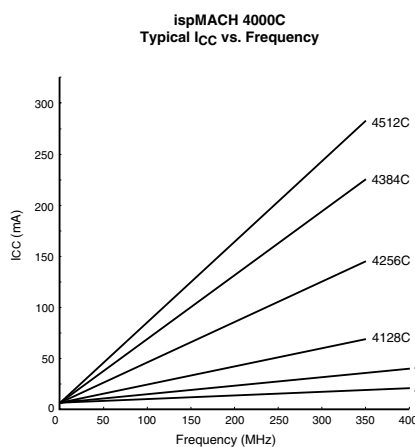
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

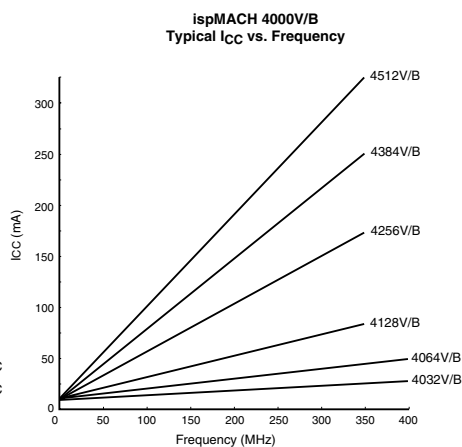
## Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

## Power Estimation Coefficients<sup>1</sup>

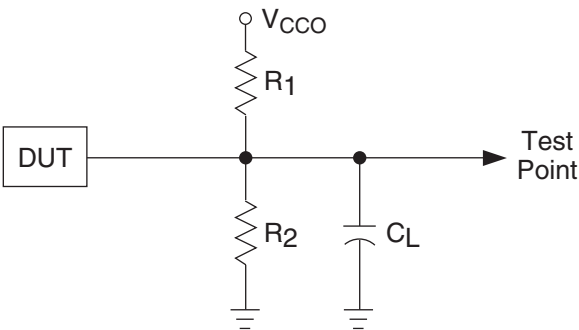
| Device          | A     | B     |
|-----------------|-------|-------|
| ispMACH 4032V/B | 11.3  | 0.010 |
| ispMACH 4032C   | 1.3   | 0.010 |
| ispMACH 4064V/B | 11.5  | 0.010 |
| ispMACH 4064C   | 1.5   | 0.010 |
| ispMACH 4128V/B | 11.5  | 0.011 |
| ispMACH 4128C   | 1.5   | 0.011 |
| ispMACH 4256V/B | 12    | 0.011 |
| ispMACH 4256C   | 2     | 0.011 |
| ispMACH 4384V/B | 12.5  | 0.013 |
| ispMACH 4384C   | 2.5   | 0.013 |
| ispMACH 4512V/B | 13    | 0.013 |
| ispMACH 4512C   | 3     | 0.013 |
| ispMACH 4032ZC  | 0.010 | 0.010 |
| ispMACH 4064ZC  | 0.011 | 0.010 |
| ispMACH 4128ZC  | 0.012 | 0.010 |
| ispMACH 4256ZC  | 0.013 | 0.010 |

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTTL and LVCMOS Standards



0213A/ispm4k

Table 11. Test Fixture Required Components

| Test Condition               | $R_1$        | $R_2$        | $C_L^1$ | Timing Ref.              | $V_{CCO}$          |
|------------------------------|--------------|--------------|---------|--------------------------|--------------------|
| LVCMOS I/O, (L -> H, H -> L) | 106 $\Omega$ | 106 $\Omega$ | 35pF    | LVCMOS 3.3 = 1.5V        | LVCMOS 3.3 = 3.0V  |
|                              |              |              |         | LVCMOS 2.5 = $V_{CCO}/2$ | LVCMOS 2.5 = 2.3V  |
|                              |              |              |         | LVCMOS 1.8 = $V_{CCO}/2$ | LVCMOS 1.8 = 1.65V |
| LVCMOS I/O (Z -> H)          | $\infty$     | 106 $\Omega$ | 35pF    | 1.5V                     | 3.0V               |
| LVCMOS I/O (Z -> L)          | 106 $\Omega$ | $\infty$     | 35pF    | 1.5V                     | 3.0V               |
| LVCMOS I/O (H -> Z)          | $\infty$     | 106 $\Omega$ | 5pF     | $V_{OH} - 0.3$           | 3.0V               |
| LVCMOS I/O (L -> Z)          | 106 $\Omega$ | $\infty$     | 5pF     | $V_{OL} + 0.3$           | 3.0V               |

1.  $C_L$  includes test fixtures and probe capacitance.

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:  
48-Pin TQFP (Cont.)**

| Pin Number | Bank Number | ispMACH 4032V/B/C/Z |                 | ispMACH 4064V/B/C |                | ispMACH 4064Z |                |
|------------|-------------|---------------------|-----------------|-------------------|----------------|---------------|----------------|
|            |             | GLB/MC/Pad          | ORP             | GLB/MC/Pad        | ORP            | GLB/MC/Pad    | ORP            |
| 33         | 1           | B10                 | B <sup>10</sup> | D4                | D <sup>2</sup> | D10           | D <sup>5</sup> |
| 34         | 1           | B11                 | B <sup>11</sup> | D6                | D <sup>3</sup> | D8            | D <sup>4</sup> |
| 35         | -           | TDO                 | -               | TDO               | -              | TDO           | -              |
| 36         | -           | VCC                 | -               | VCC               | -              | VCC           | -              |
| 37         | -           | GND                 | -               | GND               | -              | GND           | -              |
| 38         | 1           | B12                 | B <sup>12</sup> | D8                | D <sup>4</sup> | D6            | D <sup>3</sup> |
| 39         | 1           | B13                 | B <sup>13</sup> | D10               | D <sup>5</sup> | D4            | D <sup>2</sup> |
| 40         | 1           | B14                 | B <sup>14</sup> | D12               | D <sup>6</sup> | D2            | D <sup>1</sup> |
| 41         | 1           | B15/GOE1            | B <sup>15</sup> | D14/GOE1          | D <sup>7</sup> | D0/GOE1       | D <sup>0</sup> |
| 42         | 1           | CLK3/I              | -               | CLK3/I            | -              | CLK3/I        | -              |
| 43         | 0           | CLK0/I              | -               | CLK0/I            | -              | CLK0/I        | -              |
| 44         | 0           | A0/GOE0             | A <sup>0</sup>  | A0/GOE0           | A <sup>0</sup> | A0/GOE0       | A <sup>0</sup> |
| 45         | 0           | A1                  | A <sup>1</sup>  | A2                | A <sup>1</sup> | A1            | A <sup>1</sup> |
| 46         | 0           | A2                  | A <sup>2</sup>  | A4                | A <sup>2</sup> | A2            | A <sup>2</sup> |
| 47         | 0           | A3                  | A <sup>3</sup>  | A6                | A <sup>3</sup> | A4            | A <sup>3</sup> |
| 48         | 0           | A4                  | A <sup>4</sup>  | A8                | A <sup>4</sup> | A6            | A <sup>4</sup> |

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA**

| Ball Number | Bank Number | ispMACH 4032Z   |                 | ispMACH 4064Z  |                |
|-------------|-------------|-----------------|-----------------|----------------|----------------|
|             |             | GLB/MC/Pad      | ORP             | GLB/MC/Pad     | ORP            |
| B1          | -           | TDI             | -               | TDI            | -              |
| C3          | 0           | A5              | A <sup>5</sup>  | A8             | A <sup>5</sup> |
| C1          | 0           | A6              | A <sup>6</sup>  | A10            | A <sup>6</sup> |
| D1          | 0           | A7              | A <sup>7</sup>  | A11            | A <sup>7</sup> |
| D3          | 0           | GND (Bank 0)    | -               | GND (Bank 0)   | -              |
| E3          | 0           | NC <sup>1</sup> | -               | I <sup>1</sup> | -              |
| E1          | 0           | NC <sup>1</sup> | -               | I <sup>1</sup> | -              |
| F3          | 0           | VCCO (Bank 0)   | -               | VCCO (Bank 0)  | -              |
| F1          | 0           | A8              | A <sup>8</sup>  | B15            | B <sup>7</sup> |
| G3          | 0           | A9              | A <sup>9</sup>  | B12            | B <sup>6</sup> |
| G1          | 0           | A10             | A <sup>10</sup> | B10            | B <sup>5</sup> |
| H1          | 0           | A11             | A <sup>11</sup> | B8             | B <sup>4</sup> |
| J1          | 0           | NC              | -               | I              | -              |
| K1          | -           | TCK             | -               | TCK            | -              |
| K2          | -           | VCC             | -               | VCC            | -              |
| H3          | -           | GND             | -               | GND            | -              |
| K3          | -           | NC <sup>1</sup> | -               | I <sup>1</sup> | -              |
| K4          | 0           | A12             | A <sup>12</sup> | B6             | B <sup>3</sup> |
| H4          | 0           | A13             | A <sup>13</sup> | B4             | B <sup>2</sup> |
| H5          | 0           | A14             | A <sup>14</sup> | B2             | B <sup>1</sup> |

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP (Cont.)**

| Pin Number | Bank Number | ispMACH 4064V/B/C/Z |                 | ispMACH 4128V/B/C/Z |                | ispMACH 4256V/B/C/Z |                |
|------------|-------------|---------------------|-----------------|---------------------|----------------|---------------------|----------------|
|            |             | GLB/MC/Pad          | ORP             | GLB/MC/Pad          | ORP            | GLB/MC/Pad          | ORP            |
| 42         | 1           | C1                  | C <sup>1</sup>  | E2                  | E <sup>1</sup> | I6                  | I <sup>1</sup> |
| 43         | 1           | C2                  | C <sup>2</sup>  | E4                  | E <sup>2</sup> | I10                 | I <sup>2</sup> |
| 44         | 1           | C3                  | C <sup>3</sup>  | E6                  | E <sup>3</sup> | I12                 | I <sup>3</sup> |
| 45         | 1           | VCCO (Bank 1)       | -               | VCCO (Bank 1)       | -              | VCCO (Bank 1)       | -              |
| 46         | 1           | GND (Bank 1)        | -               | GND (Bank 1)        | -              | GND (Bank 1)        | -              |
| 47         | 1           | C4                  | C <sup>4</sup>  | E8                  | E <sup>4</sup> | J2                  | J <sup>0</sup> |
| 48         | 1           | C5                  | C <sup>5</sup>  | E10                 | E <sup>5</sup> | J6                  | J <sup>1</sup> |
| 49         | 1           | C6                  | C <sup>6</sup>  | E12                 | E <sup>6</sup> | J10                 | J <sup>2</sup> |
| 50         | 1           | C7                  | C <sup>7</sup>  | E14                 | E <sup>7</sup> | J12                 | J <sup>3</sup> |
| 51         | -           | GND                 | -               | GND                 | -              | GND                 | -              |
| 52         | -           | TMS                 | -               | TMS                 | -              | TMS                 | -              |
| 53         | 1           | C8                  | C <sup>8</sup>  | F0                  | F <sup>0</sup> | K12                 | K <sup>3</sup> |
| 54         | 1           | C9                  | C <sup>9</sup>  | F2                  | F <sup>1</sup> | K10                 | K <sup>2</sup> |
| 55         | 1           | C10                 | C <sup>10</sup> | F4                  | F <sup>2</sup> | K6                  | K <sup>1</sup> |
| 56         | 1           | C11                 | C <sup>11</sup> | F6                  | F <sup>3</sup> | K2                  | K <sup>0</sup> |
| 57         | 1           | GND (Bank 1)        | -               | GND (Bank 1)        | -              | GND (Bank 1)        | -              |
| 58         | 1           | C12                 | C <sup>12</sup> | F8                  | F <sup>4</sup> | L12                 | L <sup>3</sup> |
| 59         | 1           | C13                 | C <sup>13</sup> | F10                 | F <sup>5</sup> | L10                 | L <sup>2</sup> |
| 60         | 1           | C14                 | C <sup>14</sup> | F12                 | F <sup>6</sup> | L6                  | L <sup>1</sup> |
| 61         | 1           | C15                 | C <sup>15</sup> | F13                 | F <sup>7</sup> | L4                  | L <sup>0</sup> |
| 62*        | 1           | I                   | -               | I                   | -              | I                   | -              |
| 63         | 1           | VCCO (Bank 1)       | -               | VCCO (Bank 1)       | -              | VCCO (Bank 1)       | -              |
| 64         | 1           | D15                 | D <sup>15</sup> | G14                 | G <sup>7</sup> | M4                  | M <sup>0</sup> |
| 65         | 1           | D14                 | D <sup>14</sup> | G12                 | G <sup>6</sup> | M6                  | M <sup>1</sup> |
| 66         | 1           | D13                 | D <sup>13</sup> | G10                 | G <sup>5</sup> | M10                 | M <sup>2</sup> |
| 67         | 1           | D12                 | D <sup>12</sup> | G8                  | G <sup>4</sup> | M12                 | M <sup>3</sup> |
| 68         | 1           | GND (Bank 1)        | -               | GND (Bank 1)        | -              | GND (Bank 1)        | -              |
| 69         | 1           | D11                 | D <sup>11</sup> | G6                  | G <sup>3</sup> | N2                  | N <sup>0</sup> |
| 70         | 1           | D10                 | D <sup>10</sup> | G5                  | G <sup>2</sup> | N6                  | N <sup>1</sup> |
| 71         | 1           | D9                  | D <sup>9</sup>  | G4                  | G <sup>1</sup> | N10                 | N <sup>2</sup> |
| 72         | 1           | D8                  | D <sup>8</sup>  | G2                  | G <sup>0</sup> | N12                 | N <sup>3</sup> |
| 73*        | 1           | I                   | -               | I                   | -              | I                   | -              |
| 74         | -           | TDO                 | -               | TDO                 | -              | TDO                 | -              |
| 75         | -           | VCC                 | -               | VCC                 | -              | VCC                 | -              |
| 76         | -           | GND                 | -               | GND                 | -              | GND                 | -              |
| 77*        | 1           | I                   | -               | I                   | -              | I                   | -              |
| 78         | 1           | D7                  | D <sup>7</sup>  | H13                 | H <sup>7</sup> | O12                 | O <sup>3</sup> |
| 79         | 1           | D6                  | D <sup>6</sup>  | H12                 | H <sup>6</sup> | O10                 | O <sup>2</sup> |
| 80         | 1           | D5                  | D <sup>5</sup>  | H10                 | H <sup>5</sup> | O6                  | O <sup>1</sup> |
| 81         | 1           | D4                  | D <sup>4</sup>  | H8                  | H <sup>4</sup> | O2                  | O <sup>0</sup> |
| 82         | 1           | GND (Bank 1)        | -               | GND (Bank 1)        | -              | GND (Bank 1)        | -              |

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP (Cont.)**

| Pin Number | Bank Number | ispMACH 4064V/B/C/Z |                | ispMACH 4128V/B/C/Z |                | ispMACH 4256V/B/C/Z |                |
|------------|-------------|---------------------|----------------|---------------------|----------------|---------------------|----------------|
|            |             | GLB/MC/Pad          | ORP            | GLB/MC/Pad          | ORP            | GLB/MC/Pad          | ORP            |
| 83         | 1           | VCCO (Bank 1)       | -              | VCCO (Bank 1)       | -              | VCCO (Bank 1)       | -              |
| 84         | 1           | D3                  | D <sup>3</sup> | H6                  | H <sup>3</sup> | P12                 | P <sup>3</sup> |
| 85         | 1           | D2                  | D <sup>2</sup> | H4                  | H <sup>2</sup> | P10                 | P <sup>2</sup> |
| 86         | 1           | D1                  | D <sup>1</sup> | H2                  | H <sup>1</sup> | P6                  | P <sup>1</sup> |
| 87         | 1           | D0/GOE1             | D <sup>0</sup> | H0/GOE1             | H <sup>0</sup> | P2/OE1              | P <sup>0</sup> |
| 88         | 1           | CLK3/I              | -              | CLK3/I              | -              | CLK3/I              | -              |
| 89         | 0           | CLK0/I              | -              | CLK0/I              | -              | CLK0/I              | -              |
| 90         | -           | VCC                 | -              | VCC                 | -              | VCC                 | -              |
| 91         | 0           | A0/GOE0             | A <sup>0</sup> | A0/GOE0             | A <sup>0</sup> | A2/GOE0             | A <sup>0</sup> |
| 92         | 0           | A1                  | A <sup>1</sup> | A2                  | A <sup>1</sup> | A6                  | A <sup>1</sup> |
| 93         | 0           | A2                  | A <sup>2</sup> | A4                  | A <sup>2</sup> | A10                 | A <sup>2</sup> |
| 94         | 0           | A3                  | A <sup>3</sup> | A6                  | A <sup>3</sup> | A12                 | A <sup>3</sup> |
| 95         | 0           | VCCO (Bank 0)       | -              | VCCO (Bank 0)       | -              | VCCO (Bank 0)       | -              |
| 96         | 0           | GND (Bank 0)        | -              | GND (Bank 0)        | -              | GND (Bank 0)        | -              |
| 97         | 0           | A4                  | A <sup>4</sup> | A8                  | A <sup>4</sup> | B2                  | B <sup>0</sup> |
| 98         | 0           | A5                  | A <sup>5</sup> | A10                 | A <sup>5</sup> | B6                  | B <sup>1</sup> |
| 99         | 0           | A6                  | A <sup>6</sup> | A12                 | A <sup>6</sup> | B10                 | B <sup>2</sup> |
| 100        | 0           | A7                  | A <sup>7</sup> | A14                 | A <sup>7</sup> | B12                 | B <sup>3</sup> |

\*This pin is input only.

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP**

| Pin Number | Bank Number | ispMACH 4128V/B/C |                 |
|------------|-------------|-------------------|-----------------|
|            |             | GLB/MC/Pad        | ORP             |
| 1          | 0           | GND               | -               |
| 2          | 0           | TDI               | -               |
| 3          | 0           | VCCO (Bank 0)     | -               |
| 4          | 0           | B0                | B <sup>0</sup>  |
| 5          | 0           | B1                | B <sup>1</sup>  |
| 6          | 0           | B2                | B <sup>2</sup>  |
| 7          | 0           | B4                | B <sup>3</sup>  |
| 8          | 0           | B5                | B <sup>4</sup>  |
| 9          | 0           | B6                | B <sup>5</sup>  |
| 10         | 0           | GND (Bank 0)      | -               |
| 11         | 0           | B8                | B <sup>6</sup>  |
| 12         | 0           | B9                | B <sup>7</sup>  |
| 13         | 0           | B10               | B <sup>8</sup>  |
| 14         | 0           | B12               | B <sup>9</sup>  |
| 15         | 0           | B13               | B <sup>10</sup> |
| 16         | 0           | B14               | B <sup>11</sup> |
| 17         | 0           | VCCO (Bank 0)     | -               |
| 18         | 0           | C14               | C <sup>11</sup> |

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)**

| Pin Number | Bank Number | ispMACH 4128V/B/C |                 |
|------------|-------------|-------------------|-----------------|
|            |             | GLB/MC/Pad        | ORP             |
| 105        | 1           | VCCO (Bank 1)     | -               |
| 106        | 1           | H6                | H <sup>5</sup>  |
| 107        | 1           | H5                | H <sup>4</sup>  |
| 108        | 1           | H4                | H <sup>3</sup>  |
| 109        | 1           | H2                | H <sup>2</sup>  |
| 110        | 1           | H1                | H <sup>1</sup>  |
| 111        | 1           | H0/GOE1           | H <sup>0</sup>  |
| 112        | 1           | CLK3/I            | -               |
| 113        | 0           | GND (Bank 0)      | -               |
| 114        | 0           | CLK0/I            | -               |
| 115        | 0           | VCC               | -               |
| 116        | 0           | A0/GOE0           | A <sup>0</sup>  |
| 117        | 0           | A1                | A <sup>1</sup>  |
| 118        | 0           | A2                | A <sup>2</sup>  |
| 119        | 0           | A4                | A <sup>3</sup>  |
| 120        | 0           | A5                | A <sup>4</sup>  |
| 121        | 0           | A6                | A <sup>5</sup>  |
| 122        | 0           | VCCO (Bank 0)     | -               |
| 123        | 0           | GND (Bank 0)      | -               |
| 124        | 0           | A8                | A <sup>6</sup>  |
| 125        | 0           | A9                | A <sup>7</sup>  |
| 126        | 0           | A10               | A <sup>8</sup>  |
| 127        | 0           | A12               | A <sup>9</sup>  |
| 128        | 0           | A14               | A <sup>11</sup> |

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:  
132-Ball csBGA**

| Ball Number | Bank Number | ispMACH 4064Z |                 | ispMACH 4128Z |                | ispMACH 4256Z |                |
|-------------|-------------|---------------|-----------------|---------------|----------------|---------------|----------------|
|             |             | GLB/MC/Pad    | ORP             | GLB/MC/Pad    | ORP            | GLB/MC/Pad    | ORP            |
| B1          | -           | GND           | -               | GND           | -              | GND           | -              |
| B2          | -           | TDI           | -               | TDI           | -              | TDI           | -              |
| C1          | 0           | NC            | -               | VCCO (Bank 0) | -              | VCCO (Bank 0) | -              |
| C3          | 0           | NC            | -               | B0            | B <sup>0</sup> | C12           | C <sup>6</sup> |
| C2          | 0           | A8            | A <sup>8</sup>  | B1            | B <sup>1</sup> | C10           | C <sup>5</sup> |
| D1          | 0           | A9            | A <sup>9</sup>  | B2            | B <sup>2</sup> | C8            | C <sup>4</sup> |
| D3          | 0           | A10           | A <sup>10</sup> | B4            | B <sup>3</sup> | C6            | C <sup>3</sup> |
| D2          | 0           | A11           | A <sup>11</sup> | B5            | B <sup>4</sup> | C4            | C <sup>2</sup> |
| E1          | 0           | NC            | -               | B6            | B <sup>5</sup> | C2            | C <sup>1</sup> |
| E2          | 0           | GND (Bank 0)  | -               | GND (Bank 0)  | -              | GND (Bank 0)  | -              |

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:  
132-Ball csBGA (Cont.)**

| Ball Number | Bank Number | ispMACH 4064Z   |                   | ispMACH 4128Z   |                   | ispMACH 4256Z  |                  |
|-------------|-------------|-----------------|-------------------|-----------------|-------------------|----------------|------------------|
|             |             | GLB/MC/Pad      | ORP               | GLB/MC/Pad      | ORP               | GLB/MC/Pad     | ORP              |
| D13         | 1           | D10             | D <sup>^</sup> 10 | G4              | G <sup>^</sup> 3  | N6             | N <sup>^</sup> 3 |
| D14         | 1           | D9              | D <sup>^</sup> 9  | G2              | G <sup>^</sup> 2  | N8             | N <sup>^</sup> 4 |
| D12         | 1           | D8              | D <sup>^</sup> 8  | G1              | G <sup>^</sup> 1  | N10            | N <sup>^</sup> 5 |
| C14         | 1           | I               | -                 | G0              | G <sup>^</sup> 0  | N12            | N <sup>^</sup> 6 |
| C13         | 1           | NC              | -                 | VCCO (Bank 1)   | -                 | VCCO (Bank 1)  | -                |
| B14         | -           | TDO             | -                 | TDO             | -                 | TDO            | -                |
| A14         | -           | VCC             | -                 | VCC             | -                 | VCC            | -                |
| A13         | -           | GND             | -                 | GND             | -                 | GND            | -                |
| B13         | 1           | NC              | -                 | H14             | H <sup>^</sup> 11 | O12            | O <sup>^</sup> 6 |
| A12         | 1           | I               | -                 | H13             | H <sup>^</sup> 10 | O10            | O <sup>^</sup> 5 |
| C12         | 1           | D7              | D <sup>^</sup> 7  | H12             | H <sup>^</sup> 9  | O8             | O <sup>^</sup> 4 |
| B12         | 1           | D6              | D <sup>^</sup> 6  | H10             | H <sup>^</sup> 8  | O6             | O <sup>^</sup> 3 |
| A11         | 1           | D5              | D <sup>^</sup> 5  | H9              | H <sup>^</sup> 7  | O4             | O <sup>^</sup> 2 |
| C11         | 1           | D4              | D <sup>^</sup> 4  | H8              | H <sup>^</sup> 6  | O2             | O <sup>^</sup> 1 |
| B11         | 1           | GND (Bank 1)    | -                 | GND (Bank 1)    | -                 | GND (Bank 1)   | -                |
| A10         | 1           | VCCO (Bank 1)   | -                 | VCCO (Bank 1)   | -                 | VCCO (Bank 1)  | -                |
| B10         | 1           | NC              | -                 | H6              | H <sup>^</sup> 5  | P12            | P <sup>^</sup> 6 |
| C10         | 1           | NC              | -                 | H5              | H <sup>^</sup> 4  | P10            | P <sup>^</sup> 5 |
| B9          | 1           | D3              | D <sup>^</sup> 3  | H4              | H <sup>^</sup> 3  | P8             | P <sup>^</sup> 4 |
| A9          | 1           | D2              | D <sup>^</sup> 2  | H2              | H <sup>^</sup> 2  | P6             | P <sup>^</sup> 3 |
| C9          | 1           | D1              | D <sup>^</sup> 1  | H1              | H <sup>^</sup> 1  | P4             | P <sup>^</sup> 2 |
| A8          | 1           | D0/GOE1         | D <sup>^</sup> 0  | H0/GOE1         | H <sup>^</sup> 0  | P2/GOE1        | P <sup>^</sup> 1 |
| B8          | 1           | CLK3/I          | -                 | CLK3/I          | -                 | CLK3/I         | -                |
| C8          | 0           | CLK0/I          | -                 | CLK0/I          | -                 | CLK0/I         | -                |
| B7          | -           | VCC             | -                 | VCC             | -                 | VCC            | -                |
| A7          | 0           | NC <sup>1</sup> | -                 | NC <sup>1</sup> | -                 | I <sup>1</sup> | -                |
| C7          | 0           | A0/GOE0         | A <sup>^</sup> 0  | A0/GOE0         | A <sup>^</sup> 0  | A2/GOE0        | A <sup>^</sup> 1 |
| A6          | 0           | A1              | A <sup>^</sup> 1  | A1              | A <sup>^</sup> 1  | A4             | A <sup>^</sup> 2 |
| B6          | 0           | A2              | A <sup>^</sup> 2  | A2              | A <sup>^</sup> 2  | A6             | A <sup>^</sup> 3 |
| C6          | 0           | A3              | A <sup>^</sup> 3  | A4              | A <sup>^</sup> 3  | A8             | A <sup>^</sup> 4 |
| B5          | 0           | NC              | -                 | A5              | A <sup>^</sup> 4  | A10            | A <sup>^</sup> 5 |
| A5          | 0           | NC              | -                 | A6              | A <sup>^</sup> 5  | A12            | A <sup>^</sup> 6 |
| C5          | 0           | VCCO (Bank 0)   | -                 | VCCO (Bank 0)   | -                 | VCCO (Bank 0)  | -                |
| B4          | 0           | GND (Bank 0)    | -                 | GND (Bank 0)    | -                 | GND (Bank 0)   | -                |
| A4          | 0           | NC              | -                 | A8              | A <sup>^</sup> 6  | B2             | B <sup>^</sup> 1 |
| C4          | 0           | A4              | A <sup>^</sup> 4  | A9              | A <sup>^</sup> 7  | B4             | B <sup>^</sup> 2 |
| A3          | 0           | A5              | A <sup>^</sup> 5  | A10             | A <sup>^</sup> 8  | B6             | B <sup>^</sup> 3 |
| B3          | 0           | A6              | A <sup>^</sup> 6  | A12             | A <sup>^</sup> 9  | B8             | B <sup>^</sup> 4 |
| A2          | 0           | A7              | A <sup>^</sup> 7  | A13             | A <sup>^</sup> 10 | B10            | B <sup>^</sup> 5 |
| A1          | 0           | NC              | -                 | A14             | A <sup>^</sup> 11 | B12            | B <sup>^</sup> 6 |

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

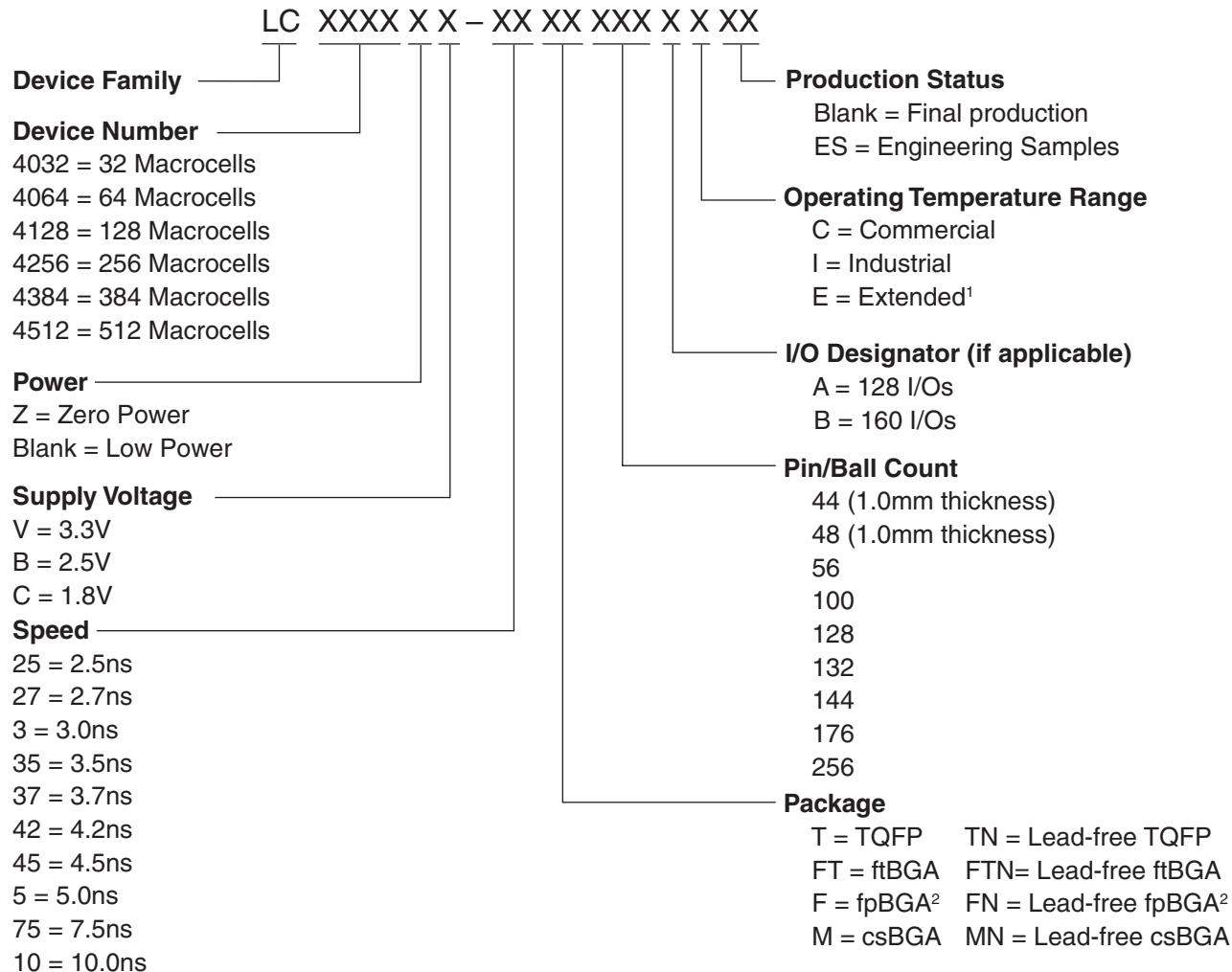
**ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)**

| Pin Number | Bank Number | ispMACH 4128V   |                   | ispMACH 4256V  |                  |
|------------|-------------|-----------------|-------------------|----------------|------------------|
|            |             | GLB/MC/Pad      | ORP               | GLB/MC/Pad     | ORP              |
| 43         | 0           | D9              | D <sup>^</sup> 7  | G4             | G <sup>^</sup> 2 |
| 44         | 0           | D8              | D <sup>^</sup> 6  | G2             | G <sup>^</sup> 1 |
| 45         | 0           | NC <sup>2</sup> | -                 | I <sup>2</sup> | -                |
| 46         | 0           | GND (Bank 0)    | -                 | GND (Bank 0)   | -                |
| 47         | 0           | VCCO (Bank 0)   | -                 | VCCO (Bank 0)  | -                |
| 48         | 0           | D6              | D <sup>^</sup> 5  | H12            | H <sup>^</sup> 6 |
| 49         | 0           | D5              | D <sup>^</sup> 4  | H10            | H <sup>^</sup> 5 |
| 50         | 0           | D4              | D <sup>^</sup> 3  | H8             | H <sup>^</sup> 4 |
| 51         | 0           | D2              | D <sup>^</sup> 2  | H6             | H <sup>^</sup> 3 |
| 52         | 0           | D1              | D <sup>^</sup> 1  | H4             | H <sup>^</sup> 2 |
| 53         | 0           | D0              | D <sup>^</sup> 0  | H2             | H <sup>^</sup> 1 |
| 54         | 0           | CLK1/I          | -                 | CLK1/I         | -                |
| 55         | 1           | GND (Bank 1)    | -                 | GND (Bank 1)   | -                |
| 56         | 1           | CLK2/I          | -                 | CLK2/I         | -                |
| 57         | -           | VCC             | -                 | VCC            | -                |
| 58         | 1           | E0              | E <sup>^</sup> 0  | I2             | I <sup>^</sup> 1 |
| 59         | 1           | E1              | E <sup>^</sup> 1  | I4             | I <sup>^</sup> 2 |
| 60         | 1           | E2              | E <sup>^</sup> 2  | I6             | I <sup>^</sup> 3 |
| 61         | 1           | E4              | E <sup>^</sup> 3  | I8             | I <sup>^</sup> 4 |
| 62         | 1           | E5              | E <sup>^</sup> 4  | I10            | I <sup>^</sup> 5 |
| 63         | 1           | E6              | E <sup>^</sup> 5  | I12            | I <sup>^</sup> 6 |
| 64         | 1           | VCCO (Bank 1)   | -                 | VCCO (Bank 1)  | -                |
| 65         | 1           | GND (Bank 1)    | -                 | GND (Bank 1)   | -                |
| 66         | 1           | E8              | E <sup>^</sup> 6  | J2             | J <sup>^</sup> 1 |
| 67         | 1           | E9              | E <sup>^</sup> 7  | J4             | J <sup>^</sup> 2 |
| 68         | 1           | E10             | E <sup>^</sup> 8  | J6             | J <sup>^</sup> 3 |
| 69         | 1           | E12             | E <sup>^</sup> 9  | J8             | J <sup>^</sup> 4 |
| 70         | 1           | E13             | E <sup>^</sup> 10 | J10            | J <sup>^</sup> 5 |
| 71         | 1           | E14             | E <sup>^</sup> 11 | J12            | J <sup>^</sup> 6 |
| 72         | 1           | NC <sup>2</sup> | -                 | I <sup>2</sup> | -                |
| 73         | -           | GND             | -                 | GND            | -                |
| 74         | -           | TMS             | -                 | TMS            | -                |
| 75         | 1           | VCCO (Bank 1)   | -                 | VCCO (Bank 1)  | -                |
| 76         | 1           | F0              | F <sup>^</sup> 0  | K12            | K <sup>^</sup> 6 |
| 77         | 1           | F1              | F <sup>^</sup> 1  | K10            | K <sup>^</sup> 5 |
| 78         | 1           | F2              | F <sup>^</sup> 2  | K8             | K <sup>^</sup> 4 |
| 79         | 1           | F4              | F <sup>^</sup> 3  | K6             | K <sup>^</sup> 3 |
| 80         | 1           | F5              | F <sup>^</sup> 4  | K4             | K <sup>^</sup> 2 |
| 81         | 1           | F6              | F <sup>^</sup> 5  | K2             | K <sup>^</sup> 1 |
| 82         | 1           | GND (Bank 1)    | -                 | GND (Bank 1)   | -                |
| 83         | 1           | F8              | F <sup>^</sup> 6  | L14            | L <sup>^</sup> 7 |
| 84         | 1           | F9              | F <sup>^</sup> 7  | L12            | L <sup>^</sup> 6 |
| 85         | 1           | F10             | F <sup>^</sup> 8  | L10            | L <sup>^</sup> 5 |

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

| Ball Number | I/O Bank | ispMACH 4256V/B/C<br>128-I/O |                | ispMACH 4256V/B/C<br>160-I/O |                | ispMACH 4384V/B/C |                 | ispMACH 4512V/B/C |                 |
|-------------|----------|------------------------------|----------------|------------------------------|----------------|-------------------|-----------------|-------------------|-----------------|
|             |          | GLB/MC/Pad                   | ORP            | GLB/MC/Pad                   | ORP            | GLB/MC/Pad        | ORP             | GLB/MC/Pad        | ORP             |
| C12         | 1        | O0                           | O <sup>0</sup> | O2                           | O <sup>2</sup> | GX0               | GX <sup>0</sup> | OX0               | OX <sup>0</sup> |
| E10         | 1        | NC                           | -              | O1                           | O <sup>1</sup> | CX8               | CX <sup>4</sup> | MX0               | MX <sup>0</sup> |
| A13         | 1        | NC                           | -              | O0                           | O <sup>0</sup> | CX10              | CX <sup>5</sup> | MX4               | MX <sup>1</sup> |
| D12         | 1        | NC                           | -              | NC                           | -              | NC                | -               | LX0               | LX <sup>0</sup> |
| -           | 1        | GND (Bank 1)                 | -              | GND (Bank 1)                 | -              | GND (Bank 1)      | -               | GND (Bank 1)      | -               |
| -           | 1        | VCCO (Bank 1)                | -              | VCCO (Bank 1)                | -              | VCCO (Bank 1)     | -               | VCCO (Bank 1)     | -               |
| B12         | 1        | NC                           | -              | NC                           | -              | NC                | -               | LX4               | LX <sup>1</sup> |
| A12         | 1        | NC                           | -              | NC                           | -              | EX2               | EX <sup>1</sup> | LX8               | LX <sup>2</sup> |
| B11         | 1        | NC                           | -              | NC                           | -              | EX0               | EX <sup>0</sup> | LX12              | LX <sup>3</sup> |
| A11         | 1        | NC                           | -              | P14                          | P <sup>9</sup> | CX12              | CX <sup>6</sup> | MX8               | MX <sup>2</sup> |
| D10         | 1        | NC                           | -              | P12                          | P <sup>8</sup> | CX14              | CX <sup>7</sup> | MX12              | MX <sup>3</sup> |
| C10         | 1        | P14                          | P <sup>7</sup> | P10                          | P <sup>7</sup> | HX14              | HX <sup>7</sup> | PX14              | PX <sup>7</sup> |
| B10         | 1        | P12                          | P <sup>6</sup> | P9                           | P <sup>6</sup> | HX12              | HX <sup>6</sup> | PX12              | PX <sup>6</sup> |
| A10         | 1        | P10                          | P <sup>5</sup> | P8                           | P <sup>5</sup> | HX10              | HX <sup>5</sup> | PX10              | PX <sup>5</sup> |
| A9          | 1        | P8                           | P <sup>4</sup> | P6                           | P <sup>4</sup> | HX8               | HX <sup>4</sup> | PX8               | PX <sup>4</sup> |
| F9          | 1        | P6                           | P <sup>3</sup> | P4                           | P <sup>3</sup> | HX6               | HX <sup>3</sup> | PX6               | PX <sup>3</sup> |
| B9          | 1        | P4                           | P <sup>2</sup> | P2                           | P <sup>2</sup> | HX4               | HX <sup>2</sup> | PX4               | PX <sup>2</sup> |
| E9          | 1        | P2/GOE1                      | P <sup>1</sup> | P1/GOE1                      | P <sup>1</sup> | HX2/GOE1          | HX <sup>1</sup> | PX2/GOE1          | PX <sup>1</sup> |
| C9          | 1        | P0                           | P <sup>0</sup> | P0                           | P <sup>0</sup> | HX0               | HX <sup>0</sup> | PX0               | PX <sup>0</sup> |
| -           | -        | GND                          | -              | GND                          | -              | GND               | -               | GND               | -               |
| D9          | 1        | CLK3/I                       | -              | CLK3/I                       | -              | CLK3/I            | -               | CLK3/I            | -               |
| -           | 0        | GND (Bank 0)                 | -              | GND (Bank 0)                 | -              | GND (Bank 0)      | -               | GND (Bank 0)      | -               |
| B8          | 0        | CLK0/I                       | -              | CLK0/I                       | -              | CLK0/I            | -               | CLK0/I            | -               |
| -           | -        | VCC                          | -              | VCC                          | -              | VCC               | -               | VCC               | -               |
| D8          | 0        | A0                           | A <sup>0</sup> | A0                           | A <sup>0</sup> | A0                | A <sup>0</sup>  | A0                | A <sup>0</sup>  |
| C8          | 0        | A2/GOE0                      | A <sup>1</sup> | A1/GOE0                      | A <sup>1</sup> | A2/GOE0           | A <sup>1</sup>  | A2/GOE0           | A <sup>1</sup>  |
| A8          | 0        | A4                           | A <sup>2</sup> | A2                           | A <sup>2</sup> | A4                | A <sup>2</sup>  | A4                | A <sup>2</sup>  |
| A7          | 0        | A6                           | A <sup>3</sup> | A4                           | A <sup>3</sup> | A6                | A <sup>3</sup>  | A6                | A <sup>3</sup>  |
| B7          | 0        | A8                           | A <sup>4</sup> | A6                           | A <sup>4</sup> | A8                | A <sup>4</sup>  | A8                | A <sup>4</sup>  |
| E8          | 0        | A10                          | A <sup>5</sup> | A8                           | A <sup>5</sup> | A10               | A <sup>5</sup>  | A10               | A <sup>5</sup>  |
| D7          | 0        | A12                          | A <sup>6</sup> | A9                           | A <sup>6</sup> | A12               | A <sup>6</sup>  | A12               | A <sup>6</sup>  |
| F8          | 0        | A14                          | A <sup>7</sup> | A10                          | A <sup>7</sup> | A14               | A <sup>7</sup>  | A14               | A <sup>7</sup>  |
| C7          | 0        | NC                           | -              | A12                          | A <sup>8</sup> | F14               | F <sup>7</sup>  | D0                | D <sup>0</sup>  |
| A6          | 0        | NC                           | -              | A14                          | A <sup>9</sup> | F12               | F <sup>6</sup>  | D4                | D <sup>1</sup>  |
| B6          | 0        | NC                           | -              | NC                           | -              | D14               | D <sup>7</sup>  | E0                | E <sup>0</sup>  |
| A5          | 0        | NC                           | -              | NC                           | -              | D12               | D <sup>6</sup>  | E4                | E <sup>1</sup>  |
| B5          | 0        | NC                           | -              | NC                           | -              | NC                | -               | E8                | E <sup>2</sup>  |
| -           | 0        | VCCO (Bank 0)                | -              | VCCO (Bank 0)                | -              | VCCO (Bank 0)     | -               | VCCO (Bank 0)     | -               |
| -           | 0        | GND (Bank 0)                 | -              | GND (Bank 0)                 | -              | GND (Bank 0)      | -               | GND (Bank 0)      | -               |
| D5          | 0        | NC                           | -              | NC                           | -              | NC                | -               | E12               | E <sup>3</sup>  |
| A4          | 0        | NC                           | -              | B0                           | B <sup>0</sup> | F10               | F <sup>5</sup>  | D8                | D <sup>2</sup>  |

## Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000 Family Speed Grade Offering

|                   | -25 | -27 | -3  | -35 | -37 | -42 | -45 | -5  |     | -75 |     |     | -10 |
|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|                   | Com | Com | Com | Com | Com | Com | Com | Com | Ind | Com | Ind | Ext | Ind |
| ispMACH 4032V/B/C |     |     |     |     |     |     |     |     |     |     |     | 1   |     |
| ispMACH 4064V/B/C |     |     |     |     |     |     |     |     |     |     |     | 1   |     |
| ispMACH 4128V/B/C |     |     |     |     |     |     |     |     |     |     |     | 1   |     |
| ispMACH 4256V/B/C |     |     |     |     |     |     |     |     |     |     |     |     |     |
| ispMACH 4384V/B/C |     |     |     |     |     |     |     |     |     |     |     |     |     |
| ispMACH 4512V/B/C |     |     |     |     |     |     |     |     |     |     |     |     |     |
| ispMACH 4032ZC    |     |     |     |     |     |     |     |     |     |     |     | 1   |     |
| ispMACH 4064ZC    |     |     |     |     |     |     |     |     |     |     |     | 1   |     |
| ispMACH 4128ZC    |     |     |     |     |     |     |     |     |     |     |     | 1   |     |
| ispMACH 4256ZC    |     |     |     |     |     |     |     |     |     |     |     |     |     |

1. 3.3V only.

## ispMACH 4000V (3.3V) Commercial Devices (Cont.)

| Device  | Part Number                   | Macrocells | Voltage | t <sub>PD</sub> | Package | Pin/Ball Count | I/O | Grade |
|---------|-------------------------------|------------|---------|-----------------|---------|----------------|-----|-------|
| LC4128V | LC4128V-27T144C               | 128        | 3.3     | 2.7             | TQFP    | 144            | 96  | C     |
|         | LC4128V-5T144C                | 128        | 3.3     | 5               | TQFP    | 144            | 96  | C     |
|         | LC4128V-75T144C               | 128        | 3.3     | 7.5             | TQFP    | 144            | 96  | C     |
|         | LC4128V-27T128C               | 128        | 3.3     | 2.7             | TQFP    | 128            | 92  | C     |
|         | LC4128V-5T128C                | 128        | 3.3     | 5               | TQFP    | 128            | 92  | C     |
|         | LC4128V-75T128C               | 128        | 3.3     | 7.5             | TQFP    | 128            | 92  | C     |
|         | LC4128V-27T100C               | 128        | 3.3     | 2.7             | TQFP    | 100            | 64  | C     |
|         | LC4128V-5T100C                | 128        | 3.3     | 5               | TQFP    | 100            | 64  | C     |
|         | LC4128V-75T100C               | 128        | 3.3     | 7.5             | TQFP    | 100            | 64  | C     |
| LC4256V | LC4256V-3FT256AC              | 256        | 3.3     | 3               | ftBGA   | 256            | 128 | C     |
|         | LC4256V-5FT256AC              | 256        | 3.3     | 5               | ftBGA   | 256            | 128 | C     |
|         | LC4256V-75FT256AC             | 256        | 3.3     | 7.5             | ftBGA   | 256            | 128 | C     |
|         | LC4256V-3FT256BC              | 256        | 3.3     | 3               | ftBGA   | 256            | 160 | C     |
|         | LC4256V-5FT256BC              | 256        | 3.3     | 5               | ftBGA   | 256            | 160 | C     |
|         | LC4256V-75FT256BC             | 256        | 3.3     | 7.5             | ftBGA   | 256            | 160 | C     |
|         | LC4256V-3F256AC <sup>1</sup>  | 256        | 3.3     | 3               | fpBGA   | 256            | 128 | C     |
|         | LC4256V-5F256AC <sup>1</sup>  | 256        | 3.3     | 5               | fpBGA   | 256            | 128 | C     |
|         | LC4256V-75F256AC <sup>1</sup> | 256        | 3.3     | 7.5             | fpBGA   | 256            | 128 | C     |
|         | LC4256V-3F256BC <sup>1</sup>  | 256        | 3.3     | 3               | fpBGA   | 256            | 160 | C     |
|         | LC4256V-5F256BC <sup>1</sup>  | 256        | 3.3     | 5               | fpBGA   | 256            | 160 | C     |
|         | LC4256V-75F256BC <sup>1</sup> | 256        | 3.3     | 7.5             | fpBGA   | 256            | 160 | C     |
|         | LC4256V-3T176C                | 256        | 3.3     | 3               | TQFP    | 176            | 128 | C     |
|         | LC4256V-5T176C                | 256        | 3.3     | 5               | TQFP    | 176            | 128 | C     |
|         | LC4256V-75T176C               | 256        | 3.3     | 7.5             | TQFP    | 176            | 128 | C     |
|         | LC4256V-3T144C                | 256        | 3.3     | 3               | TQFP    | 144            | 96  | C     |
|         | LC4256V-5T144C                | 256        | 3.3     | 5               | TQFP    | 144            | 96  | C     |
|         | LC4256V-75T144C               | 256        | 3.3     | 7.5             | TQFP    | 144            | 96  | C     |
|         | LC4256V-3T100C                | 256        | 3.3     | 3               | TQFP    | 100            | 64  | C     |
|         | LC4256V-5T100C                | 256        | 3.3     | 5               | TQFP    | 100            | 64  | C     |
|         | LC4256V-75T100C               | 256        | 3.3     | 7.5             | TQFP    | 100            | 64  | C     |
| LC4384V | LC4384V-35FT256C              | 384        | 3.3     | 3.5             | ftBGA   | 256            | 192 | C     |
|         | LC4384V-5FT256C               | 384        | 3.3     | 5               | ftBGA   | 256            | 192 | C     |
|         | LC4384V-75FT256C              | 384        | 3.3     | 7.5             | ftBGA   | 256            | 192 | C     |
|         | LC4384V-35F256C <sup>1</sup>  | 384        | 3.3     | 3.5             | fpBGA   | 256            | 192 | C     |
|         | LC4384V-5F256C <sup>1</sup>   | 384        | 3.3     | 5               | fpBGA   | 256            | 192 | C     |
|         | LC4384V-75F256C <sup>1</sup>  | 384        | 3.3     | 7.5             | fpBGA   | 256            | 192 | C     |
|         | LC4384V-35T176C               | 384        | 3.3     | 3.5             | TQFP    | 176            | 128 | C     |
|         | LC4384V-5T176C                | 384        | 3.3     | 5               | TQFP    | 176            | 128 | C     |
|         | LC4384V-75T176C               | 384        | 3.3     | 7.5             | TQFP    | 176            | 128 | C     |

## ispMACH 4000V (3.3V) Extended Temperature Devices

| Device  | Part Number     | Macrocells | Voltage | t <sub>PD</sub> | Package | Pin/Ball Count | I/O | Grade |
|---------|-----------------|------------|---------|-----------------|---------|----------------|-----|-------|
| LC4032V | LC4032V-75T48E  | 32         | 3.3     | 7.5             | TQFP    | 48             | 32  | E     |
|         | LC4032V-75T44E  | 32         | 3.3     | 7.5             | TQFP    | 44             | 30  | E     |
| LC4064V | LC4064V-75T100E | 64         | 3.3     | 7.5             | TQFP    | 100            | 64  | E     |
|         | LC4064V-75T48E  | 64         | 3.3     | 7.5             | TQFP    | 48             | 32  | E     |
|         | LC4064V-75T44E  | 64         | 3.3     | 7.5             | TQFP    | 44             | 30  | E     |
| LC4128V | LC4128V-75T144E | 128        | 3.3     | 7.5             | TQFP    | 144            | 96  | E     |
|         | LC4128V-75T128E | 128        | 3.3     | 7.5             | TQFP    | 128            | 92  | E     |
|         | LC4128V-75T100E | 128        | 3.3     | 7.5             | TQFP    | 100            | 64  | E     |
| LC4256V | LC4256V-75T176E | 256        | 3.3     | 7.5             | TQFP    | 176            | 128 | E     |
|         | LC4256V-75T144E | 256        | 3.3     | 7.5             | TQFP    | 144            | 96  | E     |
|         | LC4256V-75T100E | 256        | 3.3     | 7.5             | TQFP    | 100            | 64  | E     |

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

| Device  | Part Number                    | Macrocells | Voltage | t <sub>PD</sub> | Package         | Pin/Ball Count | I/O | Grade |
|---------|--------------------------------|------------|---------|-----------------|-----------------|----------------|-----|-------|
| LC4256V | LC4256V-5FTN256AI              | 256        | 3.3     | 5               | Lead-free ftBGA | 256            | 128 | I     |
|         | LC4256V-75FTN256AI             | 256        | 3.3     | 7.5             | Lead-free ftBGA | 256            | 128 | I     |
|         | LC4256V-10FTN256AI             | 256        | 3.3     | 10              | Lead-free ftBGA | 256            | 128 | I     |
|         | LC4256V-5FTN256BI              | 256        | 3.3     | 5               | Lead-free ftBGA | 256            | 160 | I     |
|         | LC4256V-75FTN256BI             | 256        | 3.3     | 7.5             | Lead-free ftBGA | 256            | 160 | I     |
|         | LC4256V-10FTN256BI             | 256        | 3.3     | 10              | Lead-free ftBGA | 256            | 160 | I     |
|         | LC4256V-5FN256AI <sup>1</sup>  | 256        | 3.3     | 5               | Lead-free fpBGA | 256            | 128 | I     |
|         | LC4256V-75FN256AI <sup>1</sup> | 256        | 3.3     | 7.5             | Lead-free fpBGA | 256            | 128 | I     |
|         | LC4256V-10FN256AI <sup>1</sup> | 256        | 3.3     | 10              | Lead-free fpBGA | 256            | 128 | I     |
|         | LC4256V-5FN256BI <sup>1</sup>  | 256        | 3.3     | 5               | Lead-free fpBGA | 256            | 160 | I     |
|         | LC4256V-75FN256BI <sup>1</sup> | 256        | 3.3     | 7.5             | Lead-free fpBGA | 256            | 160 | I     |
|         | LC4256V-10FN256BI <sup>1</sup> | 256        | 3.3     | 10              | Lead-free fpBGA | 256            | 160 | I     |
|         | LC4256V-5TN176I                | 256        | 3.3     | 5               | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4256V-75TN176I               | 256        | 3.3     | 7.5             | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4256V-10TN176I               | 256        | 3.3     | 10              | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4256V-5TN144I                | 256        | 3.3     | 5               | Lead-free TQFP  | 144            | 96  | I     |
|         | LC4256V-75TN144I               | 256        | 3.3     | 7.5             | Lead-free TQFP  | 144            | 96  | I     |
|         | LC4256V-10TN144I               | 256        | 3.3     | 10              | Lead-free TQFP  | 144            | 96  | I     |
|         | LC4256V-5TN100I                | 256        | 3.3     | 5               | Lead-free TQFP  | 100            | 64  | I     |
|         | LC4256V-75TN100I               | 256        | 3.3     | 7.5             | Lead-free TQFP  | 100            | 64  | I     |
|         | LC4256V-10TN100I               | 256        | 3.3     | 10              | Lead-free TQFP  | 100            | 64  | I     |
| LC4384V | LC4384V-5FTN256I               | 384        | 3.3     | 5               | Lead-free ftBGA | 256            | 192 | I     |
|         | LC4384V-75FTN256I              | 384        | 3.3     | 7.5             | Lead-free ftBGA | 256            | 192 | I     |
|         | LC4384V-10FTN256I              | 384        | 3.3     | 10              | Lead-free ftBGA | 256            | 192 | I     |
|         | LC4384V-5FN256I <sup>1</sup>   | 384        | 3.3     | 5               | Lead-free fpBGA | 256            | 192 | I     |
|         | LC4384V-75FN256I <sup>1</sup>  | 384        | 3.3     | 7.5             | Lead-free fpBGA | 256            | 192 | I     |
|         | LC4384V-10FN256I <sup>1</sup>  | 384        | 3.3     | 10              | Lead-free fpBGA | 256            | 192 | I     |
|         | LC4384V-5TN176I                | 384        | 3.3     | 5               | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4384V-75TN176I               | 384        | 3.3     | 7.5             | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4384V-10TN176I               | 384        | 3.3     | 10              | Lead-free TQFP  | 176            | 128 | I     |
| LC4512V | LC4512V-5FTN256I               | 512        | 3.3     | 5               | Lead-free ftBGA | 256            | 208 | I     |
|         | LC4512V-75FTN256I              | 512        | 3.3     | 7.5             | Lead-free ftBGA | 256            | 208 | I     |
|         | LC4512V-10FTN256I              | 512        | 3.3     | 10              | Lead-free ftBGA | 256            | 208 | I     |
|         | LC4512V-5FN256I <sup>1</sup>   | 512        | 3.3     | 5               | Lead-free fpBGA | 256            | 208 | I     |
|         | LC4512V-75FN256I <sup>1</sup>  | 512        | 3.3     | 7.5             | Lead-free fpBGA | 256            | 208 | I     |
|         | LC4512V-10FN256I <sup>1</sup>  | 512        | 3.3     | 10              | Lead-free fpBGA | 256            | 208 | I     |
|         | LC4512V-5TN176I                | 512        | 3.3     | 5               | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4512V-75TN176I               | 512        | 3.3     | 7.5             | Lead-free TQFP  | 176            | 128 | I     |
|         | LC4512V-10TN176I               | 512        | 3.3     | 10              | Lead-free TQFP  | 176            | 128 | I     |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.