



Welcome to [E-XFL.COM](http://E-XFL.COM)

## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

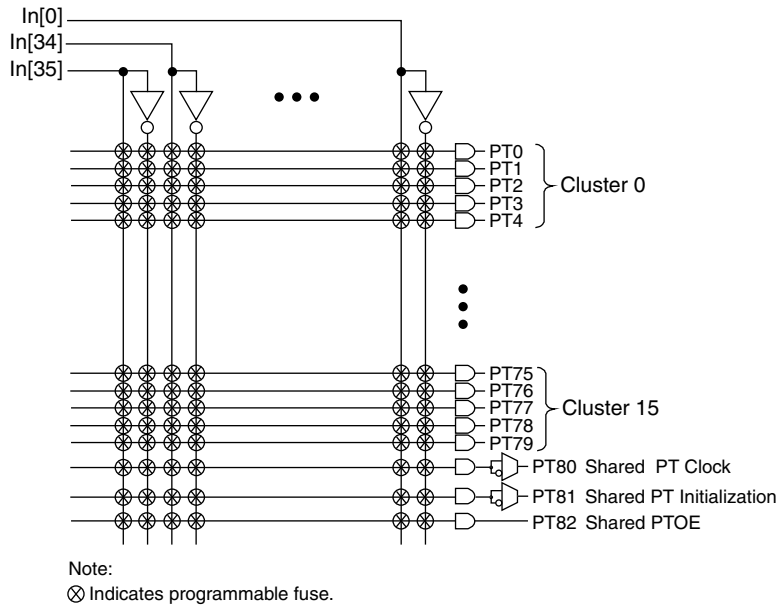
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256zc-75tn100c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256zc-75tn100c</a>

Figure 3. AND Array



### Enhanced Logic Allocator

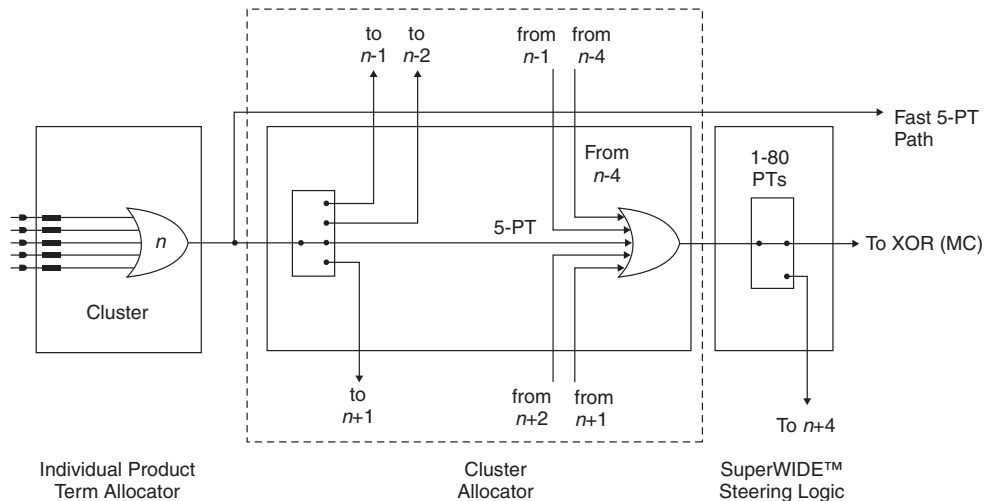
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



## IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

## User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E<sup>2</sup>CMOS memory. The ispMACH 4000 device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

## Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

## Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage ( $V_{CC}$ )	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage ( $V_{CCO}$ )	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied <sup>4, 5</sup>	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature ( $T_j$ ) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of ( $V_{IH}$  (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with  $V_{IN} > 3.6V$  is allowed.

### Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6 <sup>1, 2</sup>	1.9	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V	
	Supply Voltage for 3.3V Devices	3.0	3.6	V	
$T_j$	Junction Temperature (Commercial)	0	90	C	
	Junction Temperature (Industrial)	-40	105	C	
	Junction Temperature (Extended)	-40	130	C	

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

### Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

### Hot Socketing Characteristics<sup>1, 2, 3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DK}$	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$	—	±30	±200	µA

1. Insensitive to sequence of  $V_{CC}$  or  $V_{CCO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCO}$ , provided  $(V_{IN} - V_{CCO}) \leq 3.6V$ .
2.  $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}, I_{PD}$  or  $I_{BH}$ . Device defaults to pull-up until fuse circuitry is active.

## Supply Current, ispMACH 4000V/B/C (Cont.)

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{CC}^4$	Standby Power Supply Current	$V_{CC} = 3.3V$	—	13	—	mA
		$V_{CC} = 2.5V$	—	13	—	mA
		$V_{CC} = 1.8V$	—	3	—	mA

- $T_A = 25^\circ C$ , frequency = 1.0 MHz.
- Device configured with 16-bit counters.
- $I_{CC}$  varies with specific device configuration and operating frequency.
- $T_A = 25^\circ C$

## Supply Current, ispMACH 4000Z

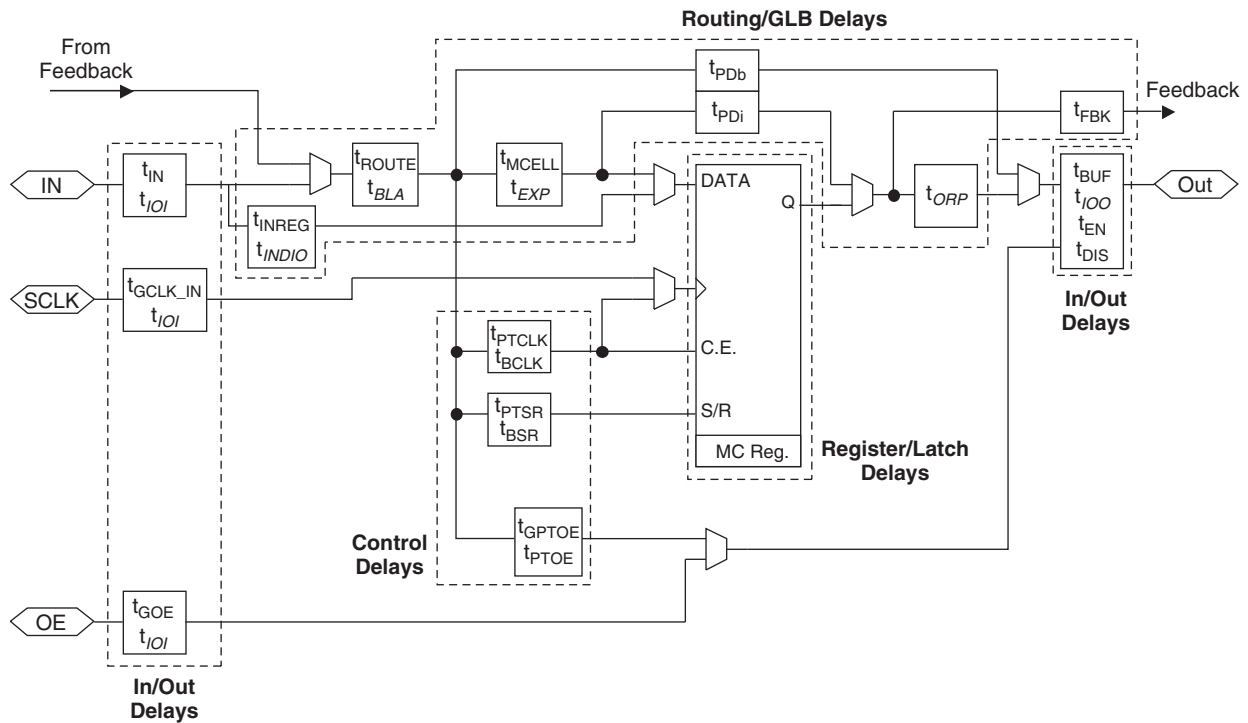
### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4032ZC</b>						
$ICC^{1,2,3,5}$	Operating Power Supply Current	$V_{CC} = 1.8V, T_A = 25^\circ C$	—	50	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 70^\circ C$	—	58	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 85^\circ C$	—	60	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 125^\circ C$	—	70	—	$\mu A$
$ICC^{4,5}$	Standby Power Supply Current	$V_{CC} = 1.8V, T_A = 25^\circ C$	—	10	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 70^\circ C$	—	13	20	$\mu A$
		$V_{CC} = 1.9V, T_A = 85^\circ C$	—	15	25	$\mu A$
		$V_{CC} = 1.9V, T_A = 125^\circ C$	—	22	—	$\mu A$
<b>ispMACH 4064ZC</b>						
$ICC^{1,2,3,5}$	Operating Power Supply Current	$V_{CC} = 1.8V, T_A = 25^\circ C$	—	80	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 70^\circ C$	—	89	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 85^\circ C$	—	92	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 125^\circ C$	—	109	—	$\mu A$
$ICC^{4,5}$	Standby Power Supply Current	$V_{CC} = 1.8V, T_A = 25^\circ C$	—	11	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 70^\circ C$	—	15	25	$\mu A$
		$V_{CC} = 1.9V, T_A = 85^\circ C$	—	18	35	$\mu A$
		$V_{CC} = 1.9V, T_A = 125^\circ C$	—	37	—	$\mu A$
<b>ispMACH 4128ZC</b>						
$ICC^{1,2,3,5}$	Operating Power Supply Current	$V_{CC} = 1.8V, T_A = 25^\circ C$	—	168	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 70^\circ C$	—	190	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 85^\circ C$	—	195	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 125^\circ C$	—	212	—	$\mu A$
$ICC^{4,5}$	Standby Power Supply Current	$V_{CC} = 1.8V, T_A = 25^\circ C$	—	12	—	$\mu A$
		$V_{CC} = 1.9V, T_A = 70^\circ C$	—	16	35	$\mu A$
		$V_{CC} = 1.9V, T_A = 85^\circ C$	—	19	50	$\mu A$
		$V_{CC} = 1.9V, T_A = 125^\circ C$	—	42	—	$\mu A$

## Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#).

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

**ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
$t_{PDLi}$	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
$t_{SRi}$	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
$t_{SRR}$	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
<b>Control Delays</b>										
$t_{BCLK}$	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
$t_{PTCLK}$	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
$t_{BSR}$	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
$t_{PTSR}$	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
$t_{GPtoE}$	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
$t_{PtoE}$	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

## ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

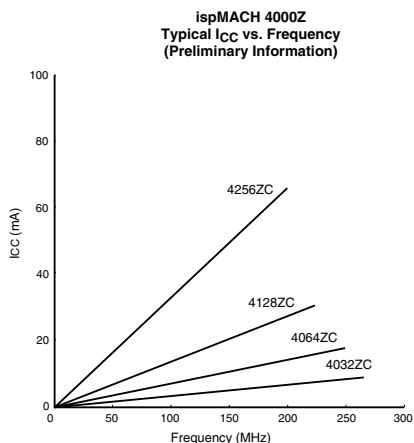
Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>GP</sub> TOE	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t <sub>P</sub> TOE	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

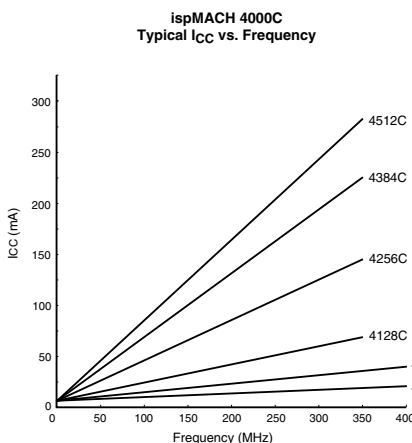
Timing v.2.2



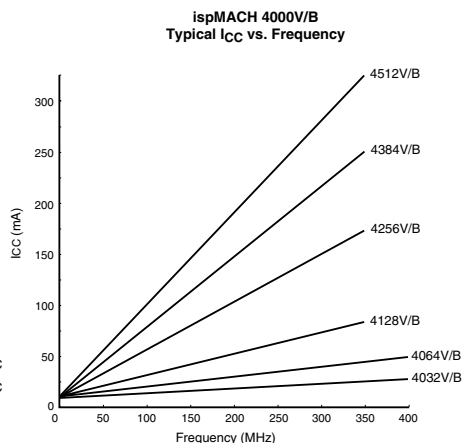
## Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

## Power Estimation Coefficients<sup>1</sup>

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:  
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B <sup>^</sup> 10	D4	D <sup>^</sup> 2	D10	D <sup>^</sup> 5
34	1	B11	B <sup>^</sup> 11	D6	D <sup>^</sup> 3	D8	D <sup>^</sup> 4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B <sup>^</sup> 12	D8	D <sup>^</sup> 4	D6	D <sup>^</sup> 3
39	1	B13	B <sup>^</sup> 13	D10	D <sup>^</sup> 5	D4	D <sup>^</sup> 2
40	1	B14	B <sup>^</sup> 14	D12	D <sup>^</sup> 6	D2	D <sup>^</sup> 1
41	1	B15/GOE1	B <sup>^</sup> 15	D14/GOE1	D <sup>^</sup> 7	D0/GOE1	D <sup>^</sup> 0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A <sup>^</sup> 0	A0/GOE0	A <sup>^</sup> 0	A0/GOE0	A <sup>^</sup> 0
45	0	A1	A <sup>^</sup> 1	A2	A <sup>^</sup> 1	A1	A <sup>^</sup> 1
46	0	A2	A <sup>^</sup> 2	A4	A <sup>^</sup> 2	A2	A <sup>^</sup> 2
47	0	A3	A <sup>^</sup> 3	A6	A <sup>^</sup> 3	A4	A <sup>^</sup> 3
48	0	A4	A <sup>^</sup> 4	A8	A <sup>^</sup> 4	A6	A <sup>^</sup> 4

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A <sup>^</sup> 5	A8	A <sup>^</sup> 5
C1	0	A6	A <sup>^</sup> 6	A10	A <sup>^</sup> 6
D1	0	A7	A <sup>^</sup> 7	A11	A <sup>^</sup> 7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
E1	0	NC <sup>1</sup>	-	I <sup>1</sup>	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A <sup>^</sup> 8	B15	B <sup>^</sup> 7
G3	0	A9	A <sup>^</sup> 9	B12	B <sup>^</sup> 6
G1	0	A10	A <sup>^</sup> 10	B10	B <sup>^</sup> 5
H1	0	A11	A <sup>^</sup> 11	B8	B <sup>^</sup> 4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC <sup>1</sup>	-	I <sup>1</sup>	-
K4	0	A12	A <sup>^</sup> 12	B6	B <sup>^</sup> 3
H4	0	A13	A <sup>^</sup> 13	B4	B <sup>^</sup> 2
H5	0	A14	A <sup>^</sup> 14	B2	B <sup>^</sup> 1

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D <sup>3</sup>	H6	H <sup>3</sup>	P12	P <sup>3</sup>
85	1	D2	D <sup>2</sup>	H4	H <sup>2</sup>	P10	P <sup>2</sup>
86	1	D1	D <sup>1</sup>	H2	H <sup>1</sup>	P6	P <sup>1</sup>
87	1	D0/GOE1	D <sup>0</sup>	H0/GOE1	H <sup>0</sup>	P2/OE1	P <sup>0</sup>
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>	A2/GOE0	A <sup>0</sup>
92	0	A1	A <sup>1</sup>	A2	A <sup>1</sup>	A6	A <sup>1</sup>
93	0	A2	A <sup>2</sup>	A4	A <sup>2</sup>	A10	A <sup>2</sup>
94	0	A3	A <sup>3</sup>	A6	A <sup>3</sup>	A12	A <sup>3</sup>
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A <sup>4</sup>	A8	A <sup>4</sup>	B2	B <sup>0</sup>
98	0	A5	A <sup>5</sup>	A10	A <sup>5</sup>	B6	B <sup>1</sup>
99	0	A6	A <sup>6</sup>	A12	A <sup>6</sup>	B10	B <sup>2</sup>
100	0	A7	A <sup>7</sup>	A14	A <sup>7</sup>	B12	B <sup>3</sup>

\*This pin is input only.

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B <sup>0</sup>
5	0	B1	B <sup>1</sup>
6	0	B2	B <sup>2</sup>
7	0	B4	B <sup>3</sup>
8	0	B5	B <sup>4</sup>
9	0	B6	B <sup>5</sup>
10	0	GND (Bank 0)	-
11	0	B8	B <sup>6</sup>
12	0	B9	B <sup>7</sup>
13	0	B10	B <sup>8</sup>
14	0	B12	B <sup>9</sup>
15	0	B13	B <sup>10</sup>
16	0	B14	B <sup>11</sup>
17	0	VCCO (Bank 0)	-
18	0	C14	C <sup>11</sup>

**ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D <sup>^</sup> 7	G4	G <sup>^</sup> 2
44	0	D8	D <sup>^</sup> 6	G2	G <sup>^</sup> 1
45	0	NC <sup>2</sup>	-	I <sup>2</sup>	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D <sup>^</sup> 5	H12	H <sup>^</sup> 6
49	0	D5	D <sup>^</sup> 4	H10	H <sup>^</sup> 5
50	0	D4	D <sup>^</sup> 3	H8	H <sup>^</sup> 4
51	0	D2	D <sup>^</sup> 2	H6	H <sup>^</sup> 3
52	0	D1	D <sup>^</sup> 1	H4	H <sup>^</sup> 2
53	0	D0	D <sup>^</sup> 0	H2	H <sup>^</sup> 1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E <sup>^</sup> 0	I2	I <sup>^</sup> 1
59	1	E1	E <sup>^</sup> 1	I4	I <sup>^</sup> 2
60	1	E2	E <sup>^</sup> 2	I6	I <sup>^</sup> 3
61	1	E4	E <sup>^</sup> 3	I8	I <sup>^</sup> 4
62	1	E5	E <sup>^</sup> 4	I10	I <sup>^</sup> 5
63	1	E6	E <sup>^</sup> 5	I12	I <sup>^</sup> 6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E <sup>^</sup> 6	J2	J <sup>^</sup> 1
67	1	E9	E <sup>^</sup> 7	J4	J <sup>^</sup> 2
68	1	E10	E <sup>^</sup> 8	J6	J <sup>^</sup> 3
69	1	E12	E <sup>^</sup> 9	J8	J <sup>^</sup> 4
70	1	E13	E <sup>^</sup> 10	J10	J <sup>^</sup> 5
71	1	E14	E <sup>^</sup> 11	J12	J <sup>^</sup> 6
72	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F <sup>^</sup> 0	K12	K <sup>^</sup> 6
77	1	F1	F <sup>^</sup> 1	K10	K <sup>^</sup> 5
78	1	F2	F <sup>^</sup> 2	K8	K <sup>^</sup> 4
79	1	F4	F <sup>^</sup> 3	K6	K <sup>^</sup> 3
80	1	F5	F <sup>^</sup> 4	K4	K <sup>^</sup> 2
81	1	F6	F <sup>^</sup> 5	K2	K <sup>^</sup> 1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F <sup>^</sup> 6	L14	L <sup>^</sup> 7
84	1	F9	F <sup>^</sup> 7	L12	L <sup>^</sup> 6
85	1	F10	F <sup>^</sup> 8	L10	L <sup>^</sup> 5

**ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC <sup>2</sup>	-	I <sup>2</sup>	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D <sup>2</sup>	E4	E <sup>2</sup>	G4	G <sup>2</sup>
20	0	D2	D <sup>1</sup>	E2	E <sup>1</sup>	G2	G <sup>1</sup>
21	0	D0	D <sup>0</sup>	E0	E <sup>0</sup>	G0	G <sup>0</sup>
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E <sup>0</sup>	H0	H <sup>0</sup>	J0	J <sup>0</sup>
24	0	E2	E <sup>1</sup>	H2	H <sup>1</sup>	J2	J <sup>1</sup>
25	0	E4	E <sup>2</sup>	H4	H <sup>2</sup>	J4	J <sup>2</sup>
26	0	E6	E <sup>3</sup>	H6	H <sup>3</sup>	J6	J <sup>3</sup>
27	0	E8	E <sup>4</sup>	H8	H <sup>4</sup>	J8	J <sup>4</sup>
28	0	E10	E <sup>5</sup>	H10	H <sup>5</sup>	J10	J <sup>5</sup>
29	0	E12	E <sup>6</sup>	H12	H <sup>6</sup>	J12	J <sup>6</sup>
30	0	E14	E <sup>7</sup>	H14	H <sup>7</sup>	J14	J <sup>7</sup>
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F <sup>0</sup>	J0	J <sup>0</sup>	N0	N <sup>0</sup>
33	0	F2	F <sup>1</sup>	J2	J <sup>1</sup>	N2	N <sup>1</sup>
34	0	F4	F <sup>2</sup>	J4	J <sup>2</sup>	N4	N <sup>2</sup>
35	0	F6	F <sup>3</sup>	J6	J <sup>3</sup>	N6	N <sup>3</sup>
36	0	F8	F <sup>4</sup>	J8	J <sup>4</sup>	N8	N <sup>4</sup>
37	0	F10	F <sup>5</sup>	J10	J <sup>5</sup>	N10	N <sup>5</sup>
38	0	F12	F <sup>6</sup>	J12	J <sup>6</sup>	N12	N <sup>6</sup>
39	0	F14	F <sup>7</sup>	J14	J <sup>7</sup>	N14	N <sup>7</sup>
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G <sup>7</sup>	K14	K <sup>7</sup>	O14	O <sup>7</sup>
48	0	G12	G <sup>6</sup>	K12	K <sup>6</sup>	O12	O <sup>6</sup>
49	0	G10	G <sup>5</sup>	K10	K <sup>5</sup>	O10	O <sup>5</sup>
50	0	G8	G <sup>4</sup>	K8	K <sup>4</sup>	O8	O <sup>4</sup>
51	0	G6	G <sup>3</sup>	K6	K <sup>3</sup>	O6	O <sup>3</sup>
52	0	G4	G <sup>2</sup>	K4	K <sup>2</sup>	O4	O <sup>2</sup>
53	0	G2	G <sup>1</sup>	K2	K <sup>1</sup>	O2	O <sup>1</sup>
54	0	G0	G <sup>0</sup>	K0	K <sup>0</sup>	O0	O <sup>0</sup>
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H <sup>7</sup>	L14	L <sup>7</sup>	P14	P <sup>7</sup>
58	0	H12	H <sup>6</sup>	L12	L <sup>6</sup>	P12	P <sup>6</sup>
59	0	H10	H <sup>5</sup>	L10	L <sup>5</sup>	P10	P <sup>5</sup>

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B^1	F8	F^4	D12	D^3
A3	0	B0	B^0	B2	B^2	B0	B^0	B0	B^0
F7	0	B2	B^1	B4	B^3	B2	B^1	B2	B^1
B4	0	B4	B^2	B6	B^4	B4	B^2	B4	B^2
C5	0	B6	B^3	B8	B^5	B6	B^3	B6	B^3
A2	0	B8	B^4	B9	B^6	B8	B^4	B8	B^4
E6	0	B10	B^5	B10	B^7	B10	B^5	B10	B^5
B3	0	B12	B^6	B12	B^8	B12	B^6	B12	B^6
C4	0	B14	B^7	B14	B^9	B14	B^7	B14	B^7
D4	0	NC	-	NC	-	D10	D^5	F0	F^0
E5	0	NC	-	NC	-	D8	D^4	F2	F^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

## ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC <sup>1</sup>	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC <sup>1</sup>	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC <sup>1</sup>	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC <sup>1</sup>	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC <sup>1</sup>	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC <sup>1</sup>	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
LC4256B-5T100C	256	2.5	5	TQFP	100	64	C	
LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C	
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C <sup>1</sup>	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C <sup>1</sup>	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C <sup>1</sup>	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C <sup>1</sup>	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C <sup>1</sup>	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C <sup>1</sup>	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.



## ispMACH 4000V (3.3V) Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75T48E	32	3.3	7.5	TQFP	48	32	E
	LC4032V-75T44E	32	3.3	7.5	TQFP	44	30	E
LC4064V	LC4064V-75T100E	64	3.3	7.5	TQFP	100	64	E
	LC4064V-75T48E	64	3.3	7.5	TQFP	48	32	E
	LC4064V-75T44E	64	3.3	7.5	TQFP	44	30	E
LC4128V	LC4128V-75T144E	128	3.3	7.5	TQFP	144	96	E
	LC4128V-75T128E	128	3.3	7.5	TQFP	128	92	E
	LC4128V-75T100E	128	3.3	7.5	TQFP	100	64	E
LC4256V	LC4256V-75T176E	256	3.3	7.5	TQFP	176	128	E
	LC4256V-75T144E	256	3.3	7.5	TQFP	144	96	E
	LC4256V-75T100E	256	3.3	7.5	TQFP	100	64	E

## ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4064C	LC4064C-25TN100C	64	1.8	2.5	Lead-free TQFP	100	64	C
	LC4064C-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064C-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064C-25TN48C	64	1.8	2.5	Lead-free TQFP	48	32	C
	LC4064C-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064C-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
	LC4064C-25TN44C	64	1.8	2.5	Lead-free TQFP	44	30	C
	LC4064C-5TN44C	64	1.8	5	Lead-free TQFP	44	30	C
LC4128C	LC4128C-27TN128C	128	1.8	2.7	Lead-free TQFP	128	92	C
	LC4128C-5TN128C	128	1.8	5	Lead-free TQFP	128	92	C
	LC4128C-75TN128C	128	1.8	7.5	Lead-free TQFP	128	92	C
	LC4128C-27TN100C	128	1.8	2.7	Lead-free TQFP	100	64	C
	LC4128C-5TN100C	128	1.8	5	Lead-free TQFP	100	64	C
	LC4128C-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256C	LC4256C-3FTN256AC	256	1.8	3	Lead-free ftBGA	256	128	C
	LC4256C-5FTN256AC	256	1.8	5	Lead-free ftBGA	256	128	C
	LC4256C-75FTN256AC	256	1.8	7.5	Lead-free ftBGA	256	128	C
	LC4256C-3FTN256BC	256	1.8	3	Lead-free ftBGA	256	160	C
	LC4256C-5FTN256BC	256	1.8	5	Lead-free ftBGA	256	160	C
	LC4256C-75FTN256BC	256	1.8	7.5	Lead-free ftBGA	256	160	C
	LC4256C-3FN256AC <sup>1</sup>	256	1.8	3	Lead-free fpBGA	256	128	C
	LC4256C-5FN256AC <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	128	C
	LC4256C-75FN256AC <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	128	C
	LC4256C-3FN256BC <sup>1</sup>	256	1.8	3	Lead-free fpBGA	256	160	C
	LC4256C-5FN256BC <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	160	C
	LC4256C-75FN256BC <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	160	C
	LC4256C-3TN176C	256	1.8	3	Lead-free TQFP	176	128	C
	LC4256C-5TN176C	256	1.8	5	Lead-free TQFP	176	128	C
	LC4256C-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256C-3TN100C	256	1.8	3	Lead-free TQFP	100	64	C
LC4256C-5TN100C	256	1.8	5	Lead-free TQFP	100	64	C	
LC4256C-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C	
LC4384C	LC4384C-35FTN256C	384	1.8	3.5	Lead-free ftBGA	256	192	C
	LC4384C-5FTN256C	384	1.8	5	Lead-free ftBGA	256	192	C
	LC4384C-75FTN256C	384	1.8	7.5	Lead-free ftBGA	256	192	C
	LC4384C-35FN256C <sup>1</sup>	384	1.8	3.5	Lead-free fpBGA	256	192	C
	LC4384C-5FN256C <sup>1</sup>	384	1.8	5	Lead-free fpBGA	256	192	C
	LC4384C-75FN256C <sup>1</sup>	384	1.8	7.5	Lead-free fpBGA	256	192	C
	LC4384C-35TN176C	384	1.8	3.5	Lead-free TQFP	176	128	C
	LC4384C-5TN176C	384	1.8	5	Lead-free TQFP	176	128	C
LC4384C-75TN176C	384	1.8	7.5	Lead-free TQFP	176	128	C	

## ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC <sup>1</sup>	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC <sup>1</sup>	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C	
LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C	

## ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C <sup>1</sup>	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C <sup>1</sup>	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C <sup>1</sup>	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C <sup>1</sup>	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C <sup>1</sup>	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C <sup>1</sup>	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FTN256AI	256	3.3	5	Lead-free ftBGA	256	128	I
	LC4256V-75FTN256AI	256	3.3	7.5	Lead-free ftBGA	256	128	I
	LC4256V-10FTN256AI	256	3.3	10	Lead-free ftBGA	256	128	I
	LC4256V-5FTN256BI	256	3.3	5	Lead-free ftBGA	256	160	I
	LC4256V-75FTN256BI	256	3.3	7.5	Lead-free ftBGA	256	160	I
	LC4256V-10FTN256BI	256	3.3	10	Lead-free ftBGA	256	160	I
	LC4256V-5FN256AI <sup>1</sup>	256	3.3	5	Lead-free fpBGA	256	128	I
	LC4256V-75FN256AI <sup>1</sup>	256	3.3	7.5	Lead-free fpBGA	256	128	I
	LC4256V-10FN256AI <sup>1</sup>	256	3.3	10	Lead-free fpBGA	256	128	I
	LC4256V-5FN256BI <sup>1</sup>	256	3.3	5	Lead-free fpBGA	256	160	I
	LC4256V-75FN256BI <sup>1</sup>	256	3.3	7.5	Lead-free fpBGA	256	160	I
	LC4256V-10FN256BI <sup>1</sup>	256	3.3	10	Lead-free fpBGA	256	160	I
	LC4256V-5TN176I	256	3.3	5	Lead-free TQFP	176	128	I
	LC4256V-75TN176I	256	3.3	7.5	Lead-free TQFP	176	128	I
	LC4256V-10TN176I	256	3.3	10	Lead-free TQFP	176	128	I
	LC4256V-5TN144I	256	3.3	5	Lead-free TQFP	144	96	I
	LC4256V-75TN144I	256	3.3	7.5	Lead-free TQFP	144	96	I
	LC4256V-10TN144I	256	3.3	10	Lead-free TQFP	144	96	I
	LC4256V-5TN100I	256	3.3	5	Lead-free TQFP	100	64	I
	LC4256V-75TN100I	256	3.3	7.5	Lead-free TQFP	100	64	I
LC4256V-10TN100I	256	3.3	10	Lead-free TQFP	100	64	I	
LC4384V	LC4384V-5FTN256I	384	3.3	5	Lead-free ftBGA	256	192	I
	LC4384V-75FTN256I	384	3.3	7.5	Lead-free ftBGA	256	192	I
	LC4384V-10FTN256I	384	3.3	10	Lead-free ftBGA	256	192	I
	LC4384V-5FN256I <sup>1</sup>	384	3.3	5	Lead-free fpBGA	256	192	I
	LC4384V-75FN256I <sup>1</sup>	384	3.3	7.5	Lead-free fpBGA	256	192	I
	LC4384V-10FN256I <sup>1</sup>	384	3.3	10	Lead-free fpBGA	256	192	I
	LC4384V-5TN176I	384	3.3	5	Lead-free TQFP	176	128	I
	LC4384V-75TN176I	384	3.3	7.5	Lead-free TQFP	176	128	I
LC4384V-10TN176I	384	3.3	10	Lead-free TQFP	176	128	I	
LC4512V	LC4512V-5FTN256I	512	3.3	5	Lead-free ftBGA	256	208	I
	LC4512V-75FTN256I	512	3.3	7.5	Lead-free ftBGA	256	208	I
	LC4512V-10FTN256I	512	3.3	10	Lead-free ftBGA	256	208	I
	LC4512V-5FN256I <sup>1</sup>	512	3.3	5	Lead-free fpBGA	256	208	I
	LC4512V-75FN256I <sup>1</sup>	512	3.3	7.5	Lead-free fpBGA	256	208	I
	LC4512V-10FN256I <sup>1</sup>	512	3.3	10	Lead-free fpBGA	256	208	I
	LC4512V-5TN176I	512	3.3	5	Lead-free TQFP	176	128	I
	LC4512V-75TN176I	512	3.3	7.5	Lead-free TQFP	176	128	I
	LC4512V-10TN176I	512	3.3	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.