



Welcome to [E-XFL.COM](#)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	128
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384b-10t176i

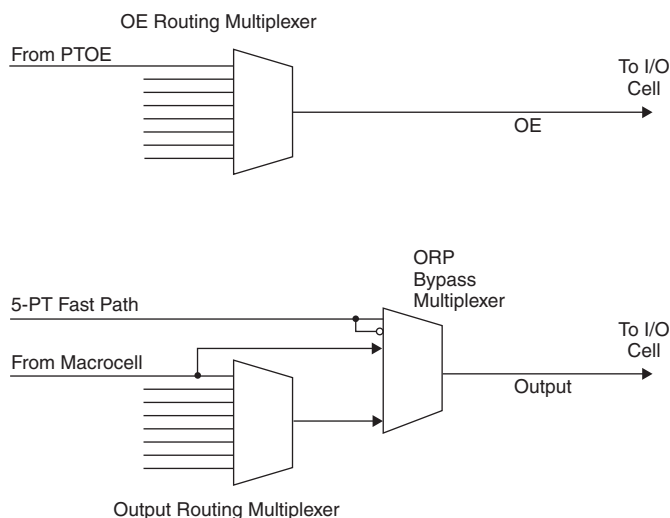
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

ispMACH 4000V/B/C External Switching Characteristics (Cont.)**Over Recommended Operating Conditions**

Parameter	Description ^{1, 2, 3}	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t_R	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t_{CW}	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t_{WIR}	Input register clock width, high or low	2.2	—	2.8	—	4.0	—	ns
f_{MAX}^4	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
$f_{MAX} (Ext.)$	Clock frequency with external feedback, $[1/(t_S + t_{CO})]$	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.3.2

2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C Timing Adders¹ (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.00	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t _{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t _{BLA}	t _{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

Signal Descriptions

Signal Names	Description
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.
GND	Ground
NC	Not Connected
V _{CC}	The power supply pins for logic core and JTAG port.
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.
V _{CC00} , V _{CC01}	The power supply pins for each I/O bank.
yzz	Input/Output ¹ – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.
	ispMACH 4032 y: A-B
	ispMACH 4064 y: A-D
	ispMACH 4128 y: A-H
	ispMACH 4256 y: A-P
	ispMACH 4384 y: A-P, AX-HX
	ispMACH 4512 y: A-P, AX-PX

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

ispMACH 4000V/B/C ORP Reference Table

	4032V/B/C		4064V/B/C			4128V/B/C			4256V/B/C				4384V/B/C		4512V/B/C	
Number of I/Os	30 ¹	32	30 ²	32	64	64	92 ³	96	64	96 ⁴	128	160	128	192	128	208
Number of GLBs	2	2	4	4	4	8	8	8	16	16	16	16	16	16	16	16
Number of I/Os / GLB	16	16	8	8	16	8	12	12	4	8	8	10	8	8	8	Mixture of 8 & 4 ⁵
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	10 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB 4 I/Os / GLB	

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.

2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.

3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os

4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per

5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

ispMACH 4000Z ORP Reference Table

	4032Z	4064Z		4128Z		4256Z		
Number of I/Os	32	32	64	64	96	64	96 ¹	128
Number of GLBs	2	4	4	8	8	16	16	16
Number of I/Os / GLB	16	8	16	8	12	4	8	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B ¹⁰	D4	D ²	D10	D ⁵
34	1	B11	B ¹¹	D6	D ³	D8	D ⁴
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B ¹²	D8	D ⁴	D6	D ³
39	1	B13	B ¹³	D10	D ⁵	D4	D ²
40	1	B14	B ¹⁴	D12	D ⁶	D2	D ¹
41	1	B15/GOE1	B ¹⁵	D14/GOE1	D ⁷	D0/GOE1	D ⁰
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰	A0/GOE0	A ⁰
45	0	A1	A ¹	A2	A ¹	A1	A ¹
46	0	A2	A ²	A4	A ²	A2	A ²
47	0	A3	A ³	A6	A ³	A4	A ³
48	0	A4	A ⁴	A8	A ⁴	A6	A ⁴

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A ⁵	A8	A ⁵
C1	0	A6	A ⁶	A10	A ⁶
D1	0	A7	A ⁷	A11	A ⁷
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC ¹	-	I ¹	-
E1	0	NC ¹	-	I ¹	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A ⁸	B15	B ⁷
G3	0	A9	A ⁹	B12	B ⁶
G1	0	A10	A ¹⁰	B10	B ⁵
H1	0	A11	A ¹¹	B8	B ⁴
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC ¹	-	I ¹	-
K4	0	A12	A ¹²	B6	B ³
H4	0	A13	A ¹³	B4	B ²
H5	0	A14	A ¹⁴	B2	B ¹

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
P8	1	NC ¹	-	NC ¹	-	I ¹	-
M8	1	NC	-	E0	E ⁰	I2	I ¹
P9	1	C0	C ⁰	E1	E ¹	I4	I ²
N9	1	C1	C ¹	E2	E ²	I6	I ³
M9	1	C2	C ²	E4	E ³	I8	I ⁴
N10	1	C3	C ³	E5	E ⁴	I10	I ⁵
P10	1	NC	-	E6	E ⁵	I12	I ⁶
M10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
N11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P11	1	NC	-	E8	E ⁶	J2	J ¹
M11	1	C4	C ⁴	E9	E ⁷	J4	J ²
P12	1	C5	C ⁵	E10	E ⁸	J6	J ³
N12	1	C6	C ⁶	E12	E ⁹	J8	J ⁴
P13	1	C7	C ⁷	E13	E ¹⁰	J10	J ⁵
P14	1	NC	-	E14	E ¹¹	J12	J ⁶
N14	-	GND	-	GND	-	GND	-
N13	-	TMS	-	TMS	-	TMS	-
M14	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
M12	1	NC	-	F0	F ⁰	K12	K ⁶
M13	1	C8	C ⁸	F1	F ¹	K10	K ⁵
L14	1	C9	C ⁹	F2	F ²	K8	K ⁴
L12	1	C10	C ¹⁰	F4	F ³	K6	K ³
L13	1	C11	C ¹¹	F5	F ⁴	K4	K ²
K14	1	NC	-	F6	F ⁵	K2	K ¹
K13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
K12	1	NC	-	F8	F ⁶	L12	L ⁶
J13	1	C12	C ¹²	F9	F ⁷	L10	L ⁵
J14	1	C13	C ¹³	F10	F ⁸	L8	L ⁴
J12	1	C14	C ¹⁴	F12	F ⁹	L6	L ³
H14	1	C15	C ¹⁵	F13	F ¹⁰	L4	L ²
H13	1	I	-	F14	F ¹¹	L2	L ¹
H12	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
G13	1	NC	-	G14	G ¹¹	M2	M ¹
G14	1	NC	-	G13	G ¹⁰	M4	M ²
G12	1	D15	D ¹⁵	G12	G ⁹	M6	M ³
F14	1	D14	D ¹⁴	G10	G ⁸	M8	M ⁴
F13	1	D13	D ¹³	G9	G ⁷	M10	M ⁵
F12	1	D12	D ¹²	G8	G ⁶	M12	M ⁶
E13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
E14	1	NC	-	G6	G ⁵	N2	N ¹
E12	1	D11	D ¹¹	G5	G ⁴	N4	N ²

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
D13	1	D10	D [^] 10	G4	G [^] 3	N6	N [^] 3
D14	1	D9	D [^] 9	G2	G [^] 2	N8	N [^] 4
D12	1	D8	D [^] 8	G1	G [^] 1	N10	N [^] 5
C14	1	I	-	G0	G [^] 0	N12	N [^] 6
C13	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B14	-	TDO	-	TDO	-	TDO	-
A14	-	VCC	-	VCC	-	VCC	-
A13	-	GND	-	GND	-	GND	-
B13	1	NC	-	H14	H [^] 11	O12	O [^] 6
A12	1	I	-	H13	H [^] 10	O10	O [^] 5
C12	1	D7	D [^] 7	H12	H [^] 9	O8	O [^] 4
B12	1	D6	D [^] 6	H10	H [^] 8	O6	O [^] 3
A11	1	D5	D [^] 5	H9	H [^] 7	O4	O [^] 2
C11	1	D4	D [^] 4	H8	H [^] 6	O2	O [^] 1
B11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B10	1	NC	-	H6	H [^] 5	P12	P [^] 6
C10	1	NC	-	H5	H [^] 4	P10	P [^] 5
B9	1	D3	D [^] 3	H4	H [^] 3	P8	P [^] 4
A9	1	D2	D [^] 2	H2	H [^] 2	P6	P [^] 3
C9	1	D1	D [^] 1	H1	H [^] 1	P4	P [^] 2
A8	1	D0/GOE1	D [^] 0	H0/GOE1	H [^] 0	P2/GOE1	P [^] 1
B8	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
C8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
B7	-	VCC	-	VCC	-	VCC	-
A7	0	NC ¹	-	NC ¹	-	I ¹	-
C7	0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0	A2/GOE0	A [^] 1
A6	0	A1	A [^] 1	A1	A [^] 1	A4	A [^] 2
B6	0	A2	A [^] 2	A2	A [^] 2	A6	A [^] 3
C6	0	A3	A [^] 3	A4	A [^] 3	A8	A [^] 4
B5	0	NC	-	A5	A [^] 4	A10	A [^] 5
A5	0	NC	-	A6	A [^] 5	A12	A [^] 6
C5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
A4	0	NC	-	A8	A [^] 6	B2	B [^] 1
C4	0	A4	A [^] 4	A9	A [^] 7	B4	B [^] 2
A3	0	A5	A [^] 5	A10	A [^] 8	B6	B [^] 3
B3	0	A6	A [^] 6	A12	A [^] 9	B8	B [^] 4
A2	0	A7	A [^] 7	A13	A [^] 10	B10	B [^] 5
A1	0	NC	-	A14	A [^] 11	B12	B [^] 6

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
4	0	B0	B [^] 0	C12	C [^] 6
5	0	B1	B [^] 1	C10	C [^] 5
6	0	B2	B [^] 2	C8	C [^] 4
7	0	B4	B [^] 3	C6	C [^] 3
8	0	B5	B [^] 4	C4	C [^] 2
9	0	B6	B [^] 5	C2	C [^] 1
10	0	GND (Bank 0)	-	GND (Bank 0)	-
11	0	B8	B [^] 6	D14	D [^] 7
12	0	B9	B [^] 7	D12	D [^] 6
13	0	B10	B [^] 8	D10	D [^] 5
14	0	B12	B [^] 9	D8	D [^] 4
15	0	B13	B [^] 10	D6	D [^] 3
16	0	B14	B [^] 11	D4	D [^] 2
17	-	NC ²	-	I ²	-
18	0	GND (Bank 0) ¹	-	NC ¹	-
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
20	0	NC ²	-	I ²	-
21	0	C14	C [^] 11	E2	E [^] 1
22	0	C13	C [^] 10	E4	E [^] 2
23	0	C12	C [^] 9	E6	E [^] 3
24	0	C10	C [^] 8	E8	E [^] 4
25	0	C9	C [^] 7	E10	E [^] 5
26	0	C8	C [^] 6	E12	E [^] 6
27	0	GND (Bank 0)	-	GND (Bank 0)	-
28	0	C6	C [^] 5	F2	F [^] 1
29	0	C5	C [^] 4	F4	F [^] 2
30	0	C4	C [^] 3	F6	F [^] 3
31	0	C2	C [^] 2	F8	F [^] 4
32	0	C1	C [^] 1	F10	F [^] 5
33	0	C0	C [^] 0	F12	F [^] 6
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
35	-	TCK	-	TCK	-
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	0	NC ²	-	I ²	-
39	0	D14	D [^] 11	G12	G [^] 6
40	0	D13	D [^] 10	G10	G [^] 5
41	0	D12	D [^] 9	G8	G [^] 4
42	0	D10	D [^] 8	G6	G [^] 3

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
101	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
102	1	L14	L ¹⁴	AX14	AX ¹⁴	GX14	GX ¹⁴
103	1	L12	L ¹²	AX12	AX ¹²	GX12	GX ¹²
104	1	L10	L ¹⁰	AX10	AX ¹⁰	GX10	GX ¹⁰
105	1	L8	L ⁸	AX8	AX ⁸	GX8	GX ⁸
106	1	L6	L ⁶	AX6	AX ⁶	GX6	GX ⁶
107	1	L4	L ⁴	AX4	AX ⁴	GX4	GX ⁴
108	1	L2	L ²	AX2	AX ²	GX2	GX ²
109	1	L0	L ⁰	AX0	AX ⁰	GX0	GX ⁰
110	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
111	1	M0	M ⁰	DX0	DX ⁰	JX0	JX ⁰
112	1	M2	M ²	DX2	DX ²	JX2	JX ²
113	1	M4	M ⁴	DX4	DX ⁴	JX4	JX ⁴
114	1	M6	M ⁶	DX6	DX ⁶	JX6	JX ⁶
115	1	M8	M ⁸	DX8	DX ⁸	JX8	JX ⁸
116	1	M10	M ¹⁰	DX10	DX ¹⁰	JX10	JX ¹⁰
117	1	M12	M ¹²	DX12	DX ¹²	JX12	JX ¹²
118	1	M14	M ¹⁴	DX14	DX ¹⁴	JX14	JX ¹⁴
119	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
120	1	N0	N ⁰	FX0	FX ⁰	NX0	NX ⁰
121	1	N2	N ²	FX2	FX ²	NX2	NX ²
122	1	N4	N ⁴	FX4	FX ⁴	NX4	NX ⁴
123	1	N6	N ⁶	FX6	FX ⁶	NX6	NX ⁶
124	1	N8	N ⁸	FX8	FX ⁸	NX8	NX ⁸
125	1	N10	N ¹⁰	FX10	FX ¹⁰	NX10	NX ¹⁰
126	1	N12	N ¹²	FX12	FX ¹²	NX12	NX ¹²
127	1	N14	N ¹⁴	FX14	FX ¹⁴	NX14	NX ¹⁴
128	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
129	-	TDO	-	TDO	-	TDO	-
130	-	VCC	-	VCC	-	VCC	-
131	-	NC	-	NC	-	NC	-
132	-	NC	-	NC	-	NC	-
133	-	NC	-	NC	-	NC	-
134	-	GND	-	GND	-	GND	-
135	1	O14	O ¹⁴	GX14	GX ¹⁴	OX14	OX ¹⁴
136	1	O12	O ¹²	GX12	GX ¹²	OX12	OX ¹²
137	1	O10	O ¹⁰	GX10	GX ¹⁰	OX10	OX ¹⁰
138	1	O8	O ⁸	GX8	GX ⁸	OX8	OX ⁸
139	1	O6	O ⁶	GX6	GX ⁶	OX6	OX ⁶
140	1	O4	O ⁴	GX4	GX ⁴	OX4	OX ⁴
141	1	O2	O ²	GX2	GX ²	OX2	OX ²

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
142	1	O0	O ⁰	GX0	GX ⁰	OX0	OX ⁰
143	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
145	1	P14	P ⁷	HX14	HX ⁷	PX14	PX ⁷
146	1	P12	P ⁶	HX12	HX ⁶	PX12	PX ⁶
147	1	P10	P ⁵	HX10	HX ⁵	PX10	PX ⁵
148	1	P8	P ⁴	HX8	HX ⁴	PX8	PX ⁴
149	1	P6	P ³	HX6	HX ³	PX6	PX ³
150	1	P4	P ²	HX4	HX ²	PX4	PX ²
151	1	P2/GOE1	P ¹	HX2/GOE1	HX ¹	PX2/GOE1	PX ¹
152	1	P0	P ⁰	HX0	HX ⁰	PX0	PX ⁰
153	-	GND	-	GND	-	GND	-
154	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
155	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
156	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
157	-	VCC	-	VCC	-	VCC	-
158	0	A0	A ⁰	A0	A ⁰	A0	A ⁰
159	0	A2/GOE0	A ¹	A2/GOE0	A ¹	A2/GOE0	A ¹
160	0	A4	A ²	A4	A ²	A4	A ²
161	0	A6	A ³	A6	A ³	A6	A ³
162	0	A8	A ⁴	A8	A ⁴	A8	A ⁴
163	0	A10	A ⁵	A10	A ⁵	A10	A ⁵
164	0	A12	A ⁶	A12	A ⁶	A12	A ⁶
165	0	A14	A ⁷	A14	A ⁷	A14	A ⁷
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
167	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
168	0	B0	B ⁰	B0	B ⁰	B0	B ⁰
169	0	B2	B ¹	B2	B ¹	B2	B ¹
170	0	B4	B ²	B4	B ²	B4	B ²
171	0	B6	B ³	B6	B ³	B6	B ³
172	0	B8	B ⁴	B8	B ⁴	B8	B ⁴
173	0	B10	B ⁵	B10	B ⁵	B10	B ⁵
174	0	B12	B ⁶	B12	B ⁶	B12	B ⁶
175	0	B14	B ⁷	B14	B ⁷	B14	B ⁷
176	-	VCC	-	VCC	-	VCC	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C ⁷	C14	C ⁹	C14	C ⁷	C14	C ⁷
F5	0	C12	C ⁶	C12	C ⁸	C12	C ⁶	C12	C ⁶
D3	0	C10	C ⁵	C10	C ⁷	C10	C ⁵	C10	C ⁵
C1	0	C8	C ⁴	C9	C ⁶	C8	C ⁴	C8	C ⁴
C2	0	C6	C ³	C8	C ⁵	C6	C ³	C6	C ³
E3	0	C4	C ²	C6	C ⁴	C4	C ²	C4	C ²
D2	0	C2	C ¹	C4	C ³	C2	C ¹	C2	C ¹
F6	0	C0	C ⁰	C2	C ²	C0	C ⁰	C0	C ⁰
D1	0	NC	-	C1	C ¹	F6	F ³	H0	H ⁰
E2	0	NC	-	C0	C ⁰	F4	F ²	H4	H ¹
E4	0	NC	-	NC	-	D6	D ³	F4	F ²
G5	0	NC	-	NC	-	D4	D ²	F6	F ³
E1	0	NC	-	NC	-	NC	-	F8	F ⁴
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F ⁵
F1	0	NC	-	NC	-	D2	D ¹	F12	F ⁶
G1	0	NC	-	NC	-	D0	D ⁰	F14	F ⁷
G6	0	NC	-	D14	D ⁹	F2	F ¹	H8	H ²
G4	0	NC	-	D12	D ⁸	F0	F ⁰	H12	H ³
H6	0	D14	D ⁷	D10	D ⁷	E14	E ⁷	G14	G ⁷
G3	0	D12	D ⁶	D9	D ⁶	E12	E ⁶	G12	G ⁶
H5	0	D10	D ⁵	D8	D ⁵	E10	E ⁵	G10	G ⁵
G2	0	D8	D ⁴	D6	D ⁴	E8	E ⁴	G8	G ⁴
H1	0	D6	D ³	D4	D ³	E6	E ³	G6	G ³
H2	0	D4	D ²	D2	D ²	E4	E ²	G4	G ²
H3	0	D2	D ¹	D1	D ¹	E2	E ¹	G2	G ¹
H4	0	D0	D ⁰	D0	D ⁰	E0	E ⁰	G0	G ⁰
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E ⁰	E0	E ⁰	H0	H ⁰	J0	J ⁰
J3	0	E2	E ¹	E1	E ¹	H2	H ¹	J2	J ¹
J2	0	E4	E ²	E2	E ²	H4	H ²	J4	J ²
J1	0	E6	E ³	E4	E ³	H6	H ³	J6	J ³
K1	0	E8	E ⁴	E6	E ⁴	H8	H ⁴	J8	J ⁴
J5	0	E10	E ⁵	E8	E ⁵	H10	H ⁵	J10	J ⁵
K2	0	E12	E ⁶	E9	E ⁶	H12	H ⁶	J12	J ⁶

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B ¹	F8	F ⁴	D12	D ³
A3	0	B0	B ⁰	B2	B ²	B0	B ⁰	B0	B ⁰
F7	0	B2	B ¹	B4	B ³	B2	B ¹	B2	B ¹
B4	0	B4	B ²	B6	B ⁴	B4	B ²	B4	B ²
C5	0	B6	B ³	B8	B ⁵	B6	B ³	B6	B ³
A2	0	B8	B ⁴	B9	B ⁶	B8	B ⁴	B8	B ⁴
E6	0	B10	B ⁵	B10	B ⁷	B10	B ⁵	B10	B ⁵
B3	0	B12	B ⁶	B12	B ⁸	B12	B ⁶	B12	B ⁶
C4	0	B14	B ⁷	B14	B ⁹	B14	B ⁷	B14	B ⁷
D4	0	NC	-	NC	-	D10	D ⁵	F0	F ⁰
E5	0	NC	-	NC	-	D8	D ⁴	F2	F ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5M132I	64	1.8	5	csBGA	132	64	I
	LC4064ZC-75M132I	64	1.8	7.5	csBGA	132	64	I
	LC4064ZC-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064ZC-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064ZC-5M56I	64	1.8	5	csBGA	56	34	I
	LC4064ZC-75M56I	64	1.8	7.5	csBGA	56	34	I
	LC4064ZC-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064ZC-75T48I	64	1.8	7.5	TQFP	48	32	I
LC4128ZC	LC4128ZC-75M132I	128	1.8	7.5	csBGA	132	96	I
	LC4128ZC-75T100I	128	1.8	7.5	TQFP	100	64	I
LC4256ZC	LC4256ZC-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256ZC-75M132I	256	1.8	7.5	csBGA	132	96	I
	LC4256ZC-75T100I	256	1.8	7.5	TQFP	100	64	I

ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75T48E	32	1.8	7.5	TQFP	48	32	E
LC4064ZC	LC4064ZC-75T100E	64	1.8	7.5	TQFP	100	64	E
	LC4064ZC-75T48E	64	1.8	7.5	TQFP	48	32	E
LC4128ZC	LC4128ZC-75T100E	128	1.8	7.5	TQFP	100	64	E
LC4256ZC	LC4256ZC-75T176E	256	1.8	7.5	TQFP	176	128	E
	LC4256ZC-75T100E	256	1.8	7.5	TQFP	100	64	E

ispMACH 4000C (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25T48C	32	1.8	2.5	TQFP	48	32	C
	LC4032C-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032C-75T48C	32	1.8	7.5	TQFP	48	32	C
	LC4032C-25T44C	32	1.8	2.5	TQFP	44	30	C
	LC4032C-5T44C	32	1.8	5	TQFP	44	30	C
	LC4032C-75T44C	32	1.8	7.5	TQFP	44	30	C
LC4064C	LC4064C-25T100C	64	1.8	2.5	TQFP	100	64	C
	LC4064C-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064C-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064C-25T48C	64	1.8	2.5	TQFP	48	32	C
	LC4064C-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064C-75T48C	64	1.8	7.5	TQFP	48	32	C
	LC4064C-25T44C	64	1.8	2.5	TQFP	44	30	C
	LC4064C-5T44C	64	1.8	5	TQFP	44	30	C
	LC4064C-75T44C	64	1.8	7.5	TQFP	44	30	C

ispMACH 4000C (1.8V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92	C
	LC4128C-5T128C	128	1.8	5	TQFP	128	92	C
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92	C
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64	C
	LC4128C-5T100C	128	1.8	5	TQFP	100	64	C
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256C	LC4256C-3FT256AC	256	1.8	3	ftBGA	256	128	C
	LC4256C-5FT256AC	256	1.8	5	ftBGA	256	128	C
	LC4256C-75FT256AC	256	1.8	7.5	ftBGA	256	128	C
	LC4256C-3FT256BC	256	1.8	3	ftBGA	256	160	C
	LC4256C-5FT256BC	256	1.8	5	ftBGA	256	160	C
	LC4256C-75FT256BC	256	1.8	7.5	ftBGA	256	160	C
	LC4256C-3F256AC ¹	256	1.8	3	fpBGA	256	128	C
	LC4256C-5F256AC ¹	256	1.8	5	fpBGA	256	128	C
	LC4256C-75F256AC ¹	256	1.8	7.5	fpBGA	256	128	C
	LC4256C-3F256BC ¹	256	1.8	3	fpBGA	256	160	C
	LC4256C-5F256BC ¹	256	1.8	5	fpBGA	256	160	C
	LC4256C-75F256BC ¹	256	1.8	7.5	fpBGA	256	160	C
	LC4256C-3T176C	256	1.8	3	TQFP	176	128	C
	LC4256C-5T176C	256	1.8	5	TQFP	176	128	C
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256C-3T100C	256	1.8	3	TQFP	100	64	C
	LC4256C-5T100C	256	1.8	5	TQFP	100	64	C
	LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C
LC4384C	LC4384C-35FT256C	384	1.8	3.5	ftBGA	256	192	C
	LC4384C-5FT256C	384	1.8	5	ftBGA	256	192	C
	LC4384C-75FT256C	384	1.8	7.5	ftBGA	256	192	C
	LC4384C-35F256C ¹	384	1.8	3.5	fpBGA	256	192	C
	LC4384C-5F256C ¹	384	1.8	5	fpBGA	256	192	C
	LC4384C-75F256C ¹	384	1.8	7.5	fpBGA	256	192	C
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128	C
	LC4384C-5T176C	384	1.8	5	TQFP	176	128	C
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128	C
LC4512C	LC4512C-35FT256C	512	1.8	3.5	ftBGA	256	208	C
	LC4512C-5FT256C	512	1.8	5	ftBGA	256	208	C
	LC4512C-75FT256C	512	1.8	7.5	ftBGA	256	208	C
	LC4512C-35F256C ¹	512	1.8	3.5	fpBGA	256	208	C
	LC4512C-5F256C ¹	512	1.8	5	fpBGA	256	208	C
	LC4512C-75F256C ¹	512	1.8	7.5	fpBGA	256	208	C
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
	LC4512C-5T176C	512	1.8	5	TQFP	176	128	C
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI ¹	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI ¹	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI ¹	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI ¹	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI ¹	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI ¹	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI ¹	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI ¹	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI ¹	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI ¹	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI ¹	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI ¹	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
	LC4256V-10T100I	256	3.3	10	TQFP	100	64	I
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I ¹	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I ¹	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I ¹	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I ¹	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I ¹	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I ¹	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75T48E	32	3.3	7.5	TQFP	48	32	E
	LC4032V-75T44E	32	3.3	7.5	TQFP	44	30	E
LC4064V	LC4064V-75T100E	64	3.3	7.5	TQFP	100	64	E
	LC4064V-75T48E	64	3.3	7.5	TQFP	48	32	E
	LC4064V-75T44E	64	3.3	7.5	TQFP	44	30	E
LC4128V	LC4128V-75T144E	128	3.3	7.5	TQFP	144	96	E
	LC4128V-75T128E	128	3.3	7.5	TQFP	128	92	E
	LC4128V-75T100E	128	3.3	7.5	TQFP	100	64	E
LC4256V	LC4256V-75T176E	256	3.3	7.5	TQFP	176	128	E
	LC4256V-75T144E	256	3.3	7.5	TQFP	144	96	E
	LC4256V-75T100E	256	3.3	7.5	TQFP	100	64	E

ispMACH 4000V (3.3V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-3FTN256AC	256	3.3	3	Lead-free ftBGA	256	128	C
	LC4256V-5FTN256AC	256	3.3	5	Lead-free ftBGA	256	128	C
	LC4256V-75FTN256AC	256	3.3	7.5	Lead-free ftBGA	256	128	C
	LC4256V-3FTN256BC	256	3.3	3	Lead-free ftBGA	256	160	C
	LC4256V-5FTN256BC	256	3.3	5	Lead-free ftBGA	256	160	C
	LC4256V-75FTN256BC	256	3.3	7.5	Lead-free ftBGA	256	160	C
	LC4256V-3FN256AC ¹	256	3.3	3	Lead-free fpBGA	256	128	C
	LC4256V-5FN256AC ¹	256	3.3	5	Lead-free fpBGA	256	128	C
	LC4256V-75FN256AC ¹	256	3.3	7.5	Lead-free fpBGA	256	128	C
	LC4256V-3FN256BC ¹	256	3.3	3	Lead-free fpBGA	256	160	C
	LC4256V-5FN256BC ¹	256	3.3	5	Lead-free fpBGA	256	160	C
	LC4256V-75FN256BC ¹	256	3.3	7.5	Lead-free fpBGA	256	160	C
	LC4256V-3TN176C	256	3.3	3	Lead-free TQFP	176	128	C
	LC4256V-5TN176C	256	3.3	5	Lead-free TQFP	176	128	C
	LC4256V-75TN176C	256	3.3	7.5	Lead-free TQFP	176	128	C
	LC4256V-3TN144C	256	3.3	3	Lead-free TQFP	144	96	C
	LC4256V-5TN144C	256	3.3	5	Lead-free TQFP	144	96	C
	LC4256V-75TN144C	256	3.3	7.5	Lead-free TQFP	144	96	C
	LC4256V-3TN100C	256	3.3	3	Lead-free TQFP	100	64	C
	LC4256V-5TN100C	256	3.3	5	Lead-free TQFP	100	64	C
	LC4256V-75TN100C	256	3.3	7.5	Lead-free TQFP	100	64	C
LC4384V	LC4384V-35FTN256C	384	3.3	3.5	Lead-free ftBGA	256	192	C
	LC4384V-5FTN256C	384	3.3	5	Lead-free ftBGA	256	192	C
	LC4384V-75FTN256C	384	3.3	7.5	Lead-free ftBGA	256	192	C
	LC4384V-35FN256C ¹	384	3.3	3.5	Lead-free fpBGA	256	192	C
	LC4384V-5FN256C ¹	384	3.3	5	Lead-free fpBGA	256	192	C
	LC4384V-75FN256C ¹	384	3.3	7.5	Lead-free fpBGA	256	192	C
	LC4384V-35TN176C	384	3.3	3.5	Lead-free TQFP	176	128	C
	LC4384V-5TN176C	384	3.3	5	Lead-free TQFP	176	128	C
	LC4384V-75TN176C	384	3.3	7.5	Lead-free TQFP	176	128	C
LC4512V	LC4512V-35FTN256C	512	3.3	3.5	Lead-free ftBGA	256	208	C
	LC4512V-5FTN256C	512	3.3	5	Lead-free ftBGA	256	208	C
	LC4512V-75FTN256C	512	3.3	7.5	Lead-free ftBGA	256	208	C
	LC4512V-35FN256C ¹	512	3.3	3.5	Lead-free fpBGA	256	208	C
	LC4512V-5FN256C ¹	512	3.3	5	Lead-free fpBGA	256	208	C
	LC4512V-75FN256C ¹	512	3.3	7.5	Lead-free fpBGA	256	208	C
	LC4512V-35TN176C	512	3.3	3.5	Lead-free TQFP	176	128	C
	LC4512V-5TN176C	512	3.3	5	Lead-free TQFP	176	128	C
	LC4512V-75TN176C	512	3.3	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 μ A to -200 μ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.