



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	3.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	192
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384b-35f256c

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

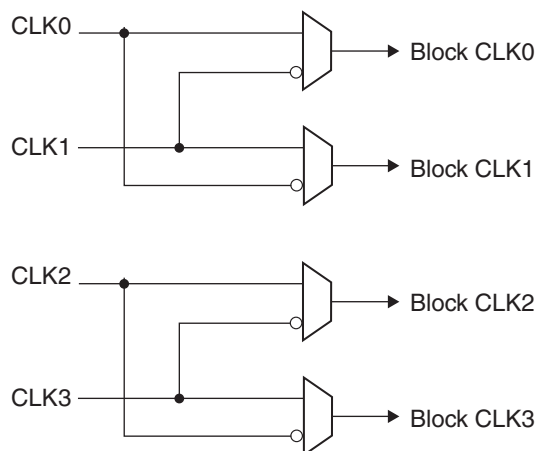
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}^{4}	Standby Power Supply Current	$V_{CC} = 3.3V$	—	13	—	mA
		$V_{CC} = 2.5V$	—	13	—	mA
		$V_{CC} = 1.8V$	—	3	—	mA

1. $T_A = 25^{\circ}C$, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. $T_A = 25^{\circ}C$

Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	Vcc = 1.8V, T _A = 25°C	—	50	—	μA
		Vcc = 1.9V, T _A = 70°C	—	58	—	μA
		Vcc = 1.9V, T _A = 85°C	—	60	—	μA
		Vcc = 1.9V, T _A = 125°C	—	70	—	μA
ICC ^{4, 5}	Standby Power Supply Current	Vcc = 1.8V, T _A = 25°C	—	10	—	μA
		Vcc = 1.9V, T _A = 70°C	—	13	20	μA
		Vcc = 1.9V, T _A = 85°C	—	15	25	μA
		Vcc = 1.9V, T _A = 125°C	—	22	—	μA
ispMACH 4064ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	Vcc = 1.8V, T _A = 25°C	—	80	—	μA
		Vcc = 1.9V, T _A = 70°C	—	89	—	μA
		Vcc = 1.9V, T _A = 85°C	—	92	—	μA
		Vcc = 1.9V, T _A = 125°C	—	109	—	μA
ICC ^{4, 5}	Standby Power Supply Current	Vcc = 1.8V, T _A = 25°C	—	11	—	μA
		Vcc = 1.9V, T _A = 70°C	—	15	25	μA
		Vcc = 1.9V, T _A = 85°C	—	18	35	μA
		Vcc = 1.9V, T _A = 125°C	—	37	—	μA
ispMACH 4128ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	Vcc = 1.8V, T _A = 25°C	—	168	—	μA
		Vcc = 1.9V, T _A = 70°C	—	190	—	μA
		Vcc = 1.9V, T _A = 85°C	—	195	—	μA
		Vcc = 1.9V, T _A = 125°C	—	212	—	μA
ICC ^{4, 5}	Standby Power Supply Current	Vcc = 1.8V, T _A = 25°C	—	12	—	μA
		Vcc = 1.9V, T _A = 70°C	—	16	35	μA
		Vcc = 1.9V, T _A = 85°C	—	19	50	μA
		Vcc = 1.9V, T _A = 125°C	—	42	—	μA

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{GPTOE}	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
t _{PTOE}	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t _{GOE}	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t _{BUF}	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t _{EN}	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t _{DIS}	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t _{MCELL}	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t _{FBK}	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t _{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t _{ST_PT}	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t _H	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{HT}	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t _{CES}	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t _{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t _{SL}	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t _{HL}	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t _{SRI}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

ispMACH 4000Z Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{P_{TOE}}	Macrocell PT OE Delay	—	2.50	—	2.70	—	2.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4000Z Timing Adders¹

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block load-ing adder	—	0.04	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

ispMACH 4000Z Timing Adders (Cont.)¹

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.30	—	1.30	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block load-ing adder	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

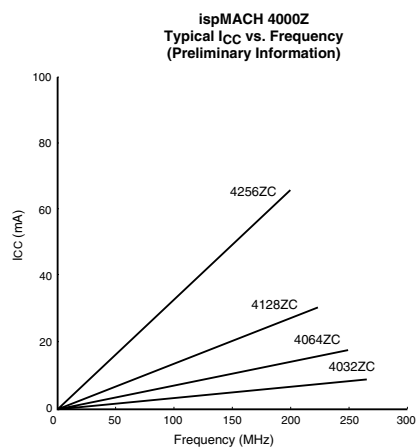
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

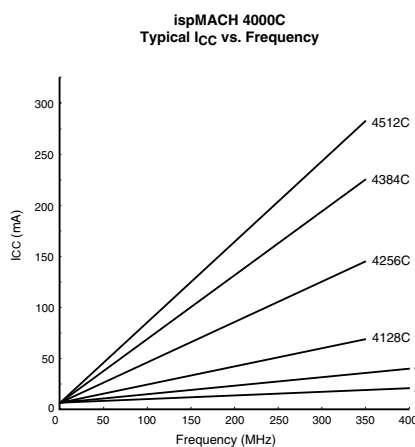
Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

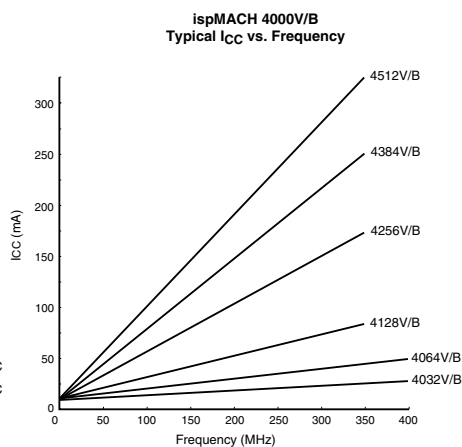
Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

Power Estimation Coefficients¹

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

Signal Descriptions

Signal Names	Description
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.
GND	Ground
NC	Not Connected
V _{CC}	The power supply pins for logic core and JTAG port.
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.
V _{CC00} , V _{CC01}	The power supply pins for each I/O bank.
yzz	Input/Output ¹ – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.
	ispMACH 4032 y: A-B
	ispMACH 4064 y: A-D
	ispMACH 4128 y: A-H
	ispMACH 4256 y: A-P
	ispMACH 4384 y: A-P, AX-HX
	ispMACH 4512 y: A-P, AX-PX

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

ispMACH 4000V/B/C ORP Reference Table

	4032V/B/C		4064V/B/C			4128V/B/C			4256V/B/C				4384V/B/C		4512V/B/C	
Number of I/Os	30 ¹	32	30 ²	32	64	64	92 ³	96	64	96 ⁴	128	160	128	192	128	208
Number of GLBs	2	2	4	4	4	8	8	8	16	16	16	16	16	16	16	16
Number of I/Os / GLB	16	16	8	8	16	8	12	12	4	8	8	10	8	8	8	Mixture of 8 & 4 ⁵
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	10 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB 4 I/Os / GLB	

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.

2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.

3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os

4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per

5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

ispMACH 4000Z ORP Reference Table

	4032Z	4064Z		4128Z		4256Z		
Number of I/Os	32	32	64	64	96	64	96 ¹	128
Number of GLBs	2	4	4	8	8	16	16	16
Number of I/Os / GLB	16	8	16	8	12	4	8	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E3	0	NC	-	B8	B ⁶	D12	D ⁶
F2	0	A12	A ¹²	B9	B ⁷	D10	D ⁵
F1	0	A13	A ¹³	B10	B ⁸	D8	D ⁴
F3	0	A14	A ¹⁴	B12	B ⁹	D6	D ³
G1	0	A15	A ¹⁵	B13	B ¹⁰	D4	D ²
G2	0	I	-	B14	B ¹¹	D2	D ¹
G3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
H2	0	NC	-	C14	C ¹¹	E2	E ¹
H1	0	B15	B ¹⁵	C13	C ¹⁰	E4	E ²
H3	0	B14	B ¹⁴	C12	C ⁹	E6	E ³
J1	0	B13	B ¹³	C10	C ⁸	E8	E ⁴
J2	0	B12	B ¹²	C9	C ⁷	E10	E ⁵
J3	0	NC	-	C8	C ⁶	E12	E ⁶
K2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
K1	0	NC	-	C6	C ⁵	F2	F ¹
K3	0	B11	B ¹¹	C5	C ⁴	F4	F ²
L2	0	B10	B ¹⁰	C4	C ³	F6	F ³
L1	0	B9	B ⁹	C2	C ²	F8	F ⁴
L3	0	B8	B ⁸	C1	C ¹	F10	F ⁵
M1	0	I	-	C0	C ⁰	F12	F ⁶
M2	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N1	-	TCK	-	TCK	-	TCK	-
P1	-	VCC	-	VCC	-	VCC	-
P2	-	GND	-	GND	-	GND	-
N2	0	I	-	D14	D ¹¹	G12	G ⁶
P3	0	B7	B ⁷	D13	D ¹⁰	G10	G ⁵
M3	0	B6	B ⁶	D12	D ⁹	G8	G ⁴
N3	0	B5	B ⁵	D10	D ⁸	G6	G ³
P4	0	B4	B ⁴	D9	D ⁷	G4	G ²
M4	0	NC	-	D8	D ⁶	G2	G ¹
N4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
P5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N5	0	NC	-	D6	D ⁵	H12	H ⁶
M5	0	B3	B ³	D5	D ⁴	H10	H ⁵
N6	0	B2	B ²	D4	D ³	H8	H ⁴
P6	0	B1	B ¹	D2	D ²	H6	H ³
M6	0	B0	B ⁰	D1	D ¹	H4	H ²
P7	0	NC	-	D0	D ⁰	H2	H ¹
N7	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
M7	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
N8	-	VCC	-	VCC	-	VCC	-

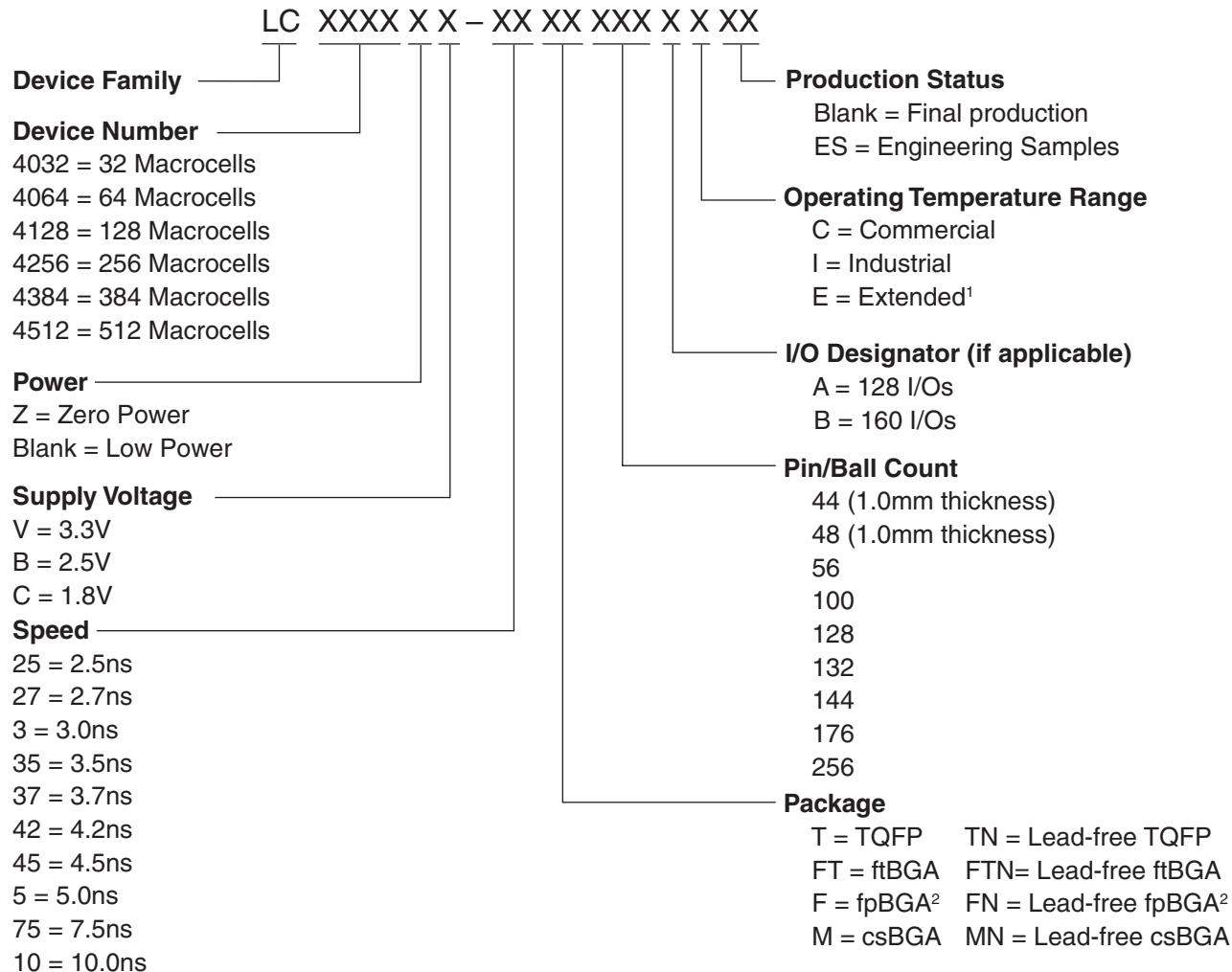
ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F ⁹	L8	L ⁴
87	1	F13	F ¹⁰	L6	L ³
88	1	F14	F ¹¹	L4	L ²
89	1	NC ²	-	I ²	-
90	1	GND (Bank 1) ¹	-	NC ¹	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC ²	-	I ²	-
93	1	G14	G ¹¹	M2	M ¹
94	1	G13	G ¹⁰	M4	M ²
95	1	G12	G ⁹	M6	M ³
96	1	G10	G ⁸	M8	M ⁴
97	1	G9	G ⁷	M10	M ⁵
98	1	G8	G ⁶	M12	M ⁶
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G ⁵	N2	N ¹
101	1	G5	G ⁴	N4	N ²
102	1	G4	G ³	N6	N ³
103	1	G2	G ²	N8	N ⁴
104	1	G1	G ¹	N10	N ⁵
105	1	G0	G ⁰	N12	N ⁶
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC ²	-	I ²	-
111	1	H14	H ¹¹	O12	O ⁶
112	1	H13	H ¹⁰	O10	O ⁵
113	1	H12	H ⁹	O8	O ⁴
114	1	H10	H ⁸	O6	O ³
115	1	H9	H ⁷	O4	O ²
116	1	H8	H ⁶	O2	O ¹
117	1	NC ²	-	I ²	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H ⁵	P12	P ⁶
121	1	H5	H ⁴	P10	P ⁵
122	1	H4	H ³	P8	P ⁴
123	1	H2	H ²	P6	P ³
124	1	H1	H ¹	P4	P ²
125	1	H0/GOE1	H ⁰	P2/GOE1	P ¹
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
60	0	H8	H ⁴	L8	L ⁴	P8	P ⁴
61	0	H6	H ³	L6	L ³	P6	P ³
62	0	H4	H ²	L4	L ²	P4	P ²
63	0	H2	H ¹	L2	L ¹	P2	P ¹
64	0	H0	H ⁰	L0	L ⁰	P0	P ⁰
65	-	GND	-	GND	-	GND	-
66	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
67	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
68	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
69	-	VCC	-	VCC	-	VCC	-
70	1	I0	I ⁰	M0	M ⁰	AX0	AX ⁰
71	1	I2	I ¹	M2	M ¹	AX2	AX ¹
72	1	I4	I ²	M4	M ²	AX4	AX ²
73	1	I6	I ³	M6	M ³	AX6	AX ³
74	1	I8	I ⁴	M8	M ⁴	AX8	AX ⁴
75	1	I10	I ⁵	M10	M ⁵	AX10	AX ⁵
76	1	I12	I ⁶	M12	M ⁶	AX12	AX ⁶
77	1	I14	I ⁷	M14	M ⁷	AX14	AX ⁷
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
79	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
80	1	J0	J ⁰	N0	N ⁰	BX0	BX ⁰
81	1	J2	J ¹	N2	N ¹	BX2	BX ¹
82	1	J4	J ²	N4	N ²	BX4	BX ²
83	1	J6	J ³	N6	N ³	BX6	BX ³
84	1	J8	J ⁴	N8	N ⁴	BX8	BX ⁴
85	1	J10	J ⁵	N10	N ⁵	BX10	BX ⁵
86	1	J12	J ⁶	N12	N ⁶	BX12	BX ⁶
87	1	J14	J ⁷	N14	N ⁷	BX14	BX ⁷
88	-	VCC	-	VCC	-	VCC	-
89	-	NC	-	NC	-	NC	-
90	-	GND	-	GND	-	GND	-
91	-	TMS	-	TMS	-	TMS	-
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
93	1	K14	K ⁷	O14	O ⁷	CX14	CX ⁷
94	1	K12	K ⁶	O12	O ⁶	CX12	CX ⁶
95	1	K10	K ⁵	O10	O ⁵	CX10	CX ⁵
96	1	K8	K ⁴	O8	O ⁴	CX8	CX ⁴
97	1	K6	K ³	O6	O ³	CX6	CX ³
98	1	K4	K ²	O4	O ²	CX4	CX ²
99	1	K2	K ¹	O2	O ¹	CX2	CX ¹
100	1	K0	K ⁰	O0	O ⁰	CX0	CX ⁰

Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I ¹	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I ¹	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I ¹	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I ¹	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I ¹	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I ¹	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C

ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064C	LC4064C-25TN100C	64	1.8	2.5	Lead-free TQFP	100	64	C
	LC4064C-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064C-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064C-25TN48C	64	1.8	2.5	Lead-free TQFP	48	32	C
	LC4064C-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064C-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
	LC4064C-25TN44C	64	1.8	2.5	Lead-free TQFP	44	30	C
	LC4064C-5TN44C	64	1.8	5	Lead-free TQFP	44	30	C
	LC4064C-75TN44C	64	1.8	7.5	Lead-free TQFP	44	30	C
LC4128C	LC4128C-27TN128C	128	1.8	2.7	Lead-free TQFP	128	92	C
	LC4128C-5TN128C	128	1.8	5	Lead-free TQFP	128	92	C
	LC4128C-75TN128C	128	1.8	7.5	Lead-free TQFP	128	92	C
	LC4128C-27TN100C	128	1.8	2.7	Lead-free TQFP	100	64	C
	LC4128C-5TN100C	128	1.8	5	Lead-free TQFP	100	64	C
	LC4128C-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256C	LC4256C-3FTN256AC	256	1.8	3	Lead-free ftBGA	256	128	C
	LC4256C-5FTN256AC	256	1.8	5	Lead-free ftBGA	256	128	C
	LC4256C-75FTN256AC	256	1.8	7.5	Lead-free ftBGA	256	128	C
	LC4256C-3FTN256BC	256	1.8	3	Lead-free ftBGA	256	160	C
	LC4256C-5FTN256BC	256	1.8	5	Lead-free ftBGA	256	160	C
	LC4256C-75FTN256BC	256	1.8	7.5	Lead-free ftBGA	256	160	C
	LC4256C-3FN256AC ¹	256	1.8	3	Lead-free fpBGA	256	128	C
	LC4256C-5FN256AC ¹	256	1.8	5	Lead-free fpBGA	256	128	C
	LC4256C-75FN256AC ¹	256	1.8	7.5	Lead-free fpBGA	256	128	C
	LC4256C-3FN256BC ¹	256	1.8	3	Lead-free fpBGA	256	160	C
	LC4256C-5FN256BC ¹	256	1.8	5	Lead-free fpBGA	256	160	C
	LC4256C-75FN256BC ¹	256	1.8	7.5	Lead-free fpBGA	256	160	C
	LC4256C-3TN176C	256	1.8	3	Lead-free TQFP	176	128	C
	LC4256C-5TN176C	256	1.8	5	Lead-free TQFP	176	128	C
	LC4256C-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256C-3TN100C	256	1.8	3	Lead-free TQFP	100	64	C
	LC4256C-5TN100C	256	1.8	5	Lead-free TQFP	100	64	C
	LC4256C-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C
LC4384C	LC4384C-35FTN256C	384	1.8	3.5	Lead-free ftBGA	256	192	C
	LC4384C-5FTN256C	384	1.8	5	Lead-free ftBGA	256	192	C
	LC4384C-75FTN256C	384	1.8	7.5	Lead-free ftBGA	256	192	C
	LC4384C-35FN256C ¹	384	1.8	3.5	Lead-free fpBGA	256	192	C
	LC4384C-5FN256C ¹	384	1.8	5	Lead-free fpBGA	256	192	C
	LC4384C-75FN256C ¹	384	1.8	7.5	Lead-free fpBGA	256	192	C
	LC4384C-35TN176C	384	1.8	3.5	Lead-free TQFP	176	128	C
	LC4384C-5TN176C	384	1.8	5	Lead-free TQFP	176	128	C
	LC4384C-75TN176C	384	1.8	7.5	Lead-free TQFP	176	128	C

ispMACH 4000V (3.3V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-3FTN256AC	256	3.3	3	Lead-free ftBGA	256	128	C
	LC4256V-5FTN256AC	256	3.3	5	Lead-free ftBGA	256	128	C
	LC4256V-75FTN256AC	256	3.3	7.5	Lead-free ftBGA	256	128	C
	LC4256V-3FTN256BC	256	3.3	3	Lead-free ftBGA	256	160	C
	LC4256V-5FTN256BC	256	3.3	5	Lead-free ftBGA	256	160	C
	LC4256V-75FTN256BC	256	3.3	7.5	Lead-free ftBGA	256	160	C
	LC4256V-3FN256AC ¹	256	3.3	3	Lead-free fpBGA	256	128	C
	LC4256V-5FN256AC ¹	256	3.3	5	Lead-free fpBGA	256	128	C
	LC4256V-75FN256AC ¹	256	3.3	7.5	Lead-free fpBGA	256	128	C
	LC4256V-3FN256BC ¹	256	3.3	3	Lead-free fpBGA	256	160	C
	LC4256V-5FN256BC ¹	256	3.3	5	Lead-free fpBGA	256	160	C
	LC4256V-75FN256BC ¹	256	3.3	7.5	Lead-free fpBGA	256	160	C
	LC4256V-3TN176C	256	3.3	3	Lead-free TQFP	176	128	C
	LC4256V-5TN176C	256	3.3	5	Lead-free TQFP	176	128	C
	LC4256V-75TN176C	256	3.3	7.5	Lead-free TQFP	176	128	C
	LC4256V-3TN144C	256	3.3	3	Lead-free TQFP	144	96	C
	LC4256V-5TN144C	256	3.3	5	Lead-free TQFP	144	96	C
	LC4256V-75TN144C	256	3.3	7.5	Lead-free TQFP	144	96	C
	LC4256V-3TN100C	256	3.3	3	Lead-free TQFP	100	64	C
	LC4256V-5TN100C	256	3.3	5	Lead-free TQFP	100	64	C
	LC4256V-75TN100C	256	3.3	7.5	Lead-free TQFP	100	64	C
LC4384V	LC4384V-35FTN256C	384	3.3	3.5	Lead-free ftBGA	256	192	C
	LC4384V-5FTN256C	384	3.3	5	Lead-free ftBGA	256	192	C
	LC4384V-75FTN256C	384	3.3	7.5	Lead-free ftBGA	256	192	C
	LC4384V-35FN256C ¹	384	3.3	3.5	Lead-free fpBGA	256	192	C
	LC4384V-5FN256C ¹	384	3.3	5	Lead-free fpBGA	256	192	C
	LC4384V-75FN256C ¹	384	3.3	7.5	Lead-free fpBGA	256	192	C
	LC4384V-35TN176C	384	3.3	3.5	Lead-free TQFP	176	128	C
	LC4384V-5TN176C	384	3.3	5	Lead-free TQFP	176	128	C
	LC4384V-75TN176C	384	3.3	7.5	Lead-free TQFP	176	128	C
LC4512V	LC4512V-35FTN256C	512	3.3	3.5	Lead-free ftBGA	256	208	C
	LC4512V-5FTN256C	512	3.3	5	Lead-free ftBGA	256	208	C
	LC4512V-75FTN256C	512	3.3	7.5	Lead-free ftBGA	256	208	C
	LC4512V-35FN256C ¹	512	3.3	3.5	Lead-free fpBGA	256	208	C
	LC4512V-5FN256C ¹	512	3.3	5	Lead-free fpBGA	256	208	C
	LC4512V-75FN256C ¹	512	3.3	7.5	Lead-free fpBGA	256	208	C
	LC4512V-35TN176C	512	3.3	3.5	Lead-free TQFP	176	128	C
	LC4512V-5TN176C	512	3.3	5	Lead-free TQFP	176	128	C
	LC4512V-75TN176C	512	3.3	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.