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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	192
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384b-5ft256i

Table 5. Product Term Expansion Capability

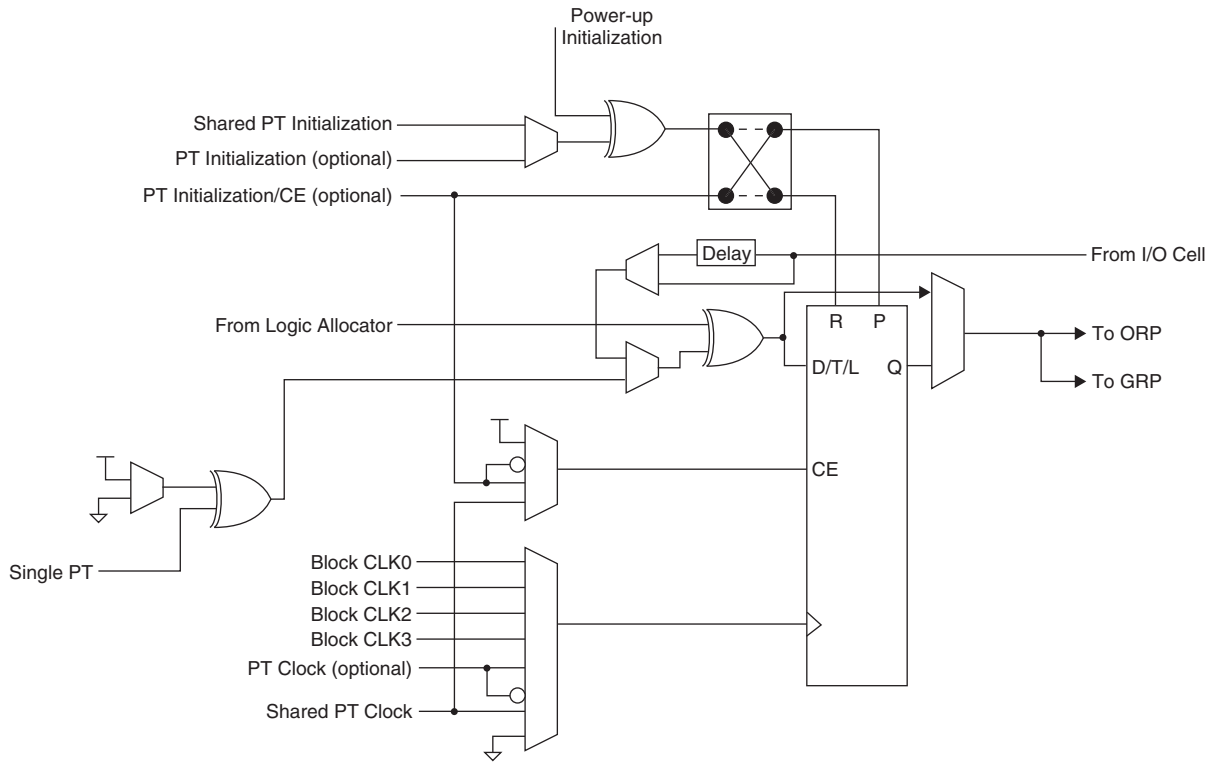
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The ispMACH 4000 device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	341	—	µA
		Vcc = 1.9V, T_A = 70°C	—	361	—	µA
		Vcc = 1.9V, T_A = 85°C	—	372	—	µA
		Vcc = 1.9V, T_A = 125°C	—	468	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	13	—	µA
		Vcc = 1.9V, T_A = 70°C	—	32	55	µA
		Vcc = 1.9V, T_A = 85°C	—	43	90	µA
		Vcc = 1.9V, T_A = 125°C	—	135	—	µA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t_S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t_{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t_R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t_{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t_{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$	—	250	—	222	—	212	—	212	MHz

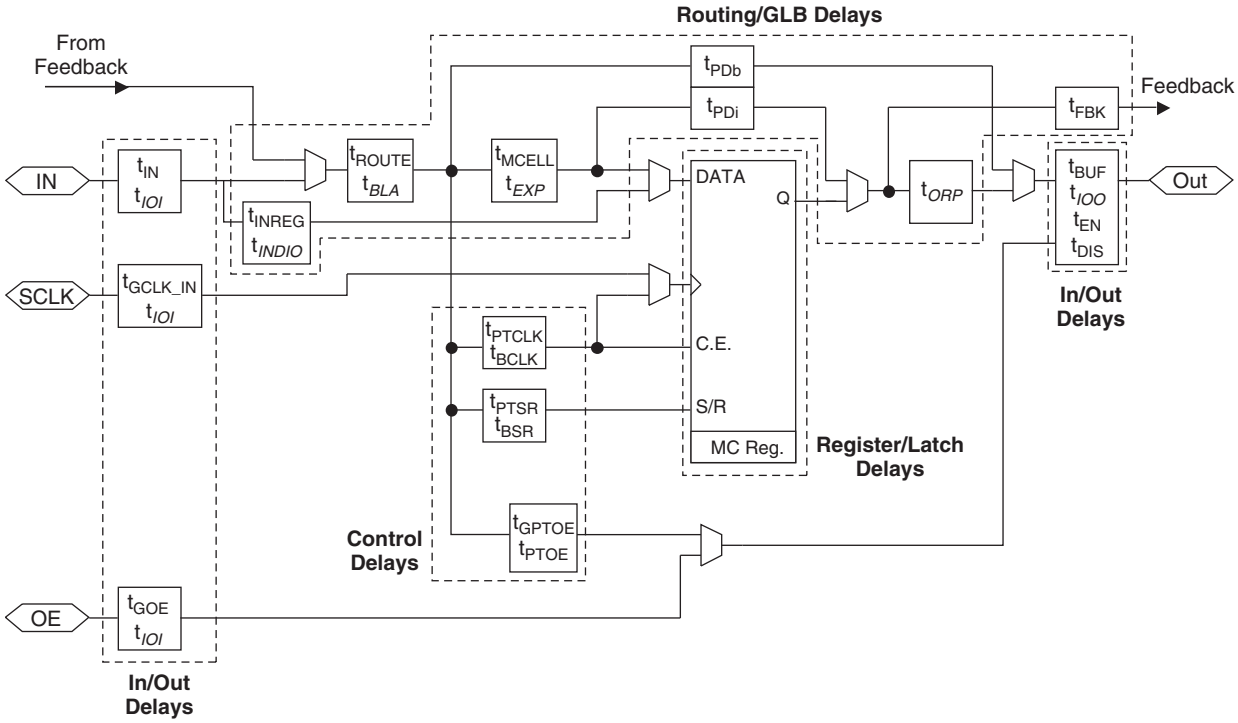
1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t_{GOE}	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t_{BUF}	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t_{EN}	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t_{DIS}	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t_{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
Register/Latch Delays								
t_{S}	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t_{H}	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t_{HT}	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t_{CES}	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t_{HL}	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{GPTOE}	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t_{PTOE}	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4000V/B/C Timing Adders[1] (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.00	—	1.00	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

ispMACH 4000Z Timing Adders (Cont.)[1]

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.30	—	1.30	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t_{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

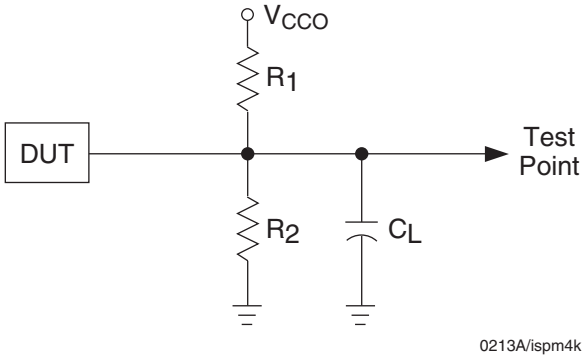


Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4000V/B/C/Z Power Supply and NC Connections[1]

Signal	44-pin TQFP[2]	48-pin TQFP[2]	56-ball csBGA[3]	100-pin TQFP[2]	128-pin TQFP[2]
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	**4032Z**: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D^7	G4	G^2
44	0	D8	D^6	G2	G^1
45	0	NC[2]	-	I[2]	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D^5	H12	H^6
49	0	D5	D^4	H10	H^5
50	0	D4	D^3	H8	H^4
51	0	D2	D^2	H6	H^3
52	0	D1	D^1	H4	H^2
53	0	D0	D^0	H2	H^1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E^0	I2	I^1
59	1	E1	E^1	I4	I^2
60	1	E2	E^2	I6	I^3
61	1	E4	E^3	I8	I^4
62	1	E5	E^4	I10	I^5
63	1	E6	E^5	I12	I^6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E^6	J2	J^1
67	1	E9	E^7	J4	J^2
68	1	E10	E^8	J6	J^3
69	1	E12	E^9	J8	J^4
70	1	E13	E^10	J10	J^5
71	1	E14	E^11	J12	J^6
72	1	NC[2]	-	I[2]	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F^0	K12	K^6
77	1	F1	F^1	K10	K^5
78	1	F2	F^2	K8	K^4
79	1	F4	F^3	K6	K^3
80	1	F5	F^4	K4	K^2
81	1	F6	F^5	K2	K^1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F^6	L14	L^7
84	1	F9	F^7	L12	L^6
85	1	F10	F^8	L10	L^5

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
142	1	O0	O^0	GX0	GX^0	OX0	OX^0
143	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
145	1	P14	P^7	HX14	HX^7	PX14	PX^7
146	1	P12	P^6	HX12	HX^6	PX12	PX^6
147	1	P10	P^5	HX10	HX^5	PX10	PX^5
148	1	P8	P^4	HX8	HX^4	PX8	PX^4
149	1	P6	P^3	HX6	HX^3	PX6	PX^3
150	1	P4	P^2	HX4	HX^2	PX4	PX^2
151	1	P2/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE1	PX^1
152	1	P0	P^0	HX0	HX^0	PX0	PX^0
153	-	GND	-	GND	-	GND	-
154	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
155	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
156	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
157	-	VCC	-	VCC	-	VCC	-
158	0	A0	A^0	A0	A^0	A0	A^0
159	0	A2/GOE0	A^1	A2/GOE0	A^1	A2//GOE0	A^1
160	0	A4	A^2	A4	A^2	A4	A^2
161	0	A6	A^3	A6	A^3	A6	A^3
162	0	A8	A^4	A8	A^4	A8	A^4
163	0	A10	A^5	A10	A^5	A10	A^5
164	0	A12	A^6	A12	A^6	A12	A^6
165	0	A14	A^7	A14	A^7	A14	A^7
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
167	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
168	0	B0	B^0	B0	B^0	B0	B^0
169	0	B2	B^1	B2	B^1	B2	B^1
170	0	B4	B^2	B4	B^2	B4	B^2
171	0	B6	B^3	B6	B^3	B6	B^3
172	0	B8	B^4	B8	B^4	B8	B^4
173	0	B10	B^5	B10	B^5	B10	B^5
174	0	B12	B^6	B12	B^6	B12	B^6
175	0	B14	B^7	B14	B^7	B14	B^7
176	-	VCC	-	VCC	-	VCC	-

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M^1	M1	M^1	DX2	DX^1	JX2	JX^1
H14	1	M4	M^2	M2	M^2	DX4	DX^2	JX4	JX^2
H13	1	M6	M^3	M4	M^3	DX6	DX^3	JX6	JX^3
G16	1	M8	M^4	M6	M^4	DX8	DX^4	JX8	JX^4
H12	1	M10	M^5	M8	M^5	DX10	DX^5	JX10	JX^5
G15	1	M12	M^6	M9	M^6	DX12	DX^6	JX12	JX^6
H11	1	M14	M^7	M10	M^7	DX14	DX^7	JX14	JX^7
F16	1	NC	-	M12	M^8	CX0	CX^0	IX0	IX^0
G13	1	NC	-	M14	M^9	CX2	CX^1	IX4	IX^1
G14	1	NC	-	NC	-	EX14	EX^7	KX0	KX^0
F15	1	NC	-	NC	-	EX12	EX^6	KX2	KX^1
E16	1	NC	-	NC	-	NC	-	KX4	KX^2
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX^3
G12	1	NC	-	NC	-	EX10	EX^5	KX8	KX^4
E13	1	NC	-	NC	-	EX8	EX^4	KX10	KX^5
D16	1	NC	-	N0	N^0	CX4	CX^2	IX8	IX^2
E14	1	NC	-	N1	N^1	CX6	CX^3	IX12	IX^3
G11	1	N0	N^0	N2	N^2	FX0	FX^0	NX0	NX^0
D15	1	N2	N^1	N4	N^3	FX2	FX^1	NX2	NX^1
F11	1	N4	N^2	N6	N^4	FX4	FX^2	NX4	NX^2
C16	1	N6	N^3	N8	N^5	FX6	FX^3	NX6	NX^3
F12	1	N8	N^4	N9	N^6	FX8	FX^4	NX8	NX^4
D14	1	N10	N^5	N10	N^7	FX10	FX^5	NX10	NX^5
C15	1	N12	N^6	N12	N^8	FX12	FX^6	NX12	NX^6
B16	1	N14	N^7	N14	N^9	FX14	FX^7	NX14	NX^7
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX^3	KX12	KX^6
B14	1	NC	-	NC	-	EX4	EX^2	KX14	KX^7
E12	1	O14	O^7	O14	O^9	GX14	GX^7	OX14	OX^7
A14	1	O12	O^6	O12	O^8	GX12	GX^6	OX12	OX^6
C13	1	O10	O^5	O10	O^7	GX10	GX^5	OX10	OX^5
D13	1	O8	O^4	O9	O^6	GX8	GX^4	OX8	OX^4
E11	1	O6	O^3	O8	O^5	GX6	GX^3	OX6	OX^3
B13	1	O4	O^2	O6	O^4	GX4	GX^2	OX4	OX^2
F10	1	O2	O^1	O4	O^3	GX2	GX^1	OX2	OX^1

ispMACH 4000C (1.8V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92	C
	LC4128C-5T128C	128	1.8	5	TQFP	128	92	C
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92	C
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64	C
	LC4128C-5T100C	128	1.8	5	TQFP	100	64	C
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256C	LC4256C-3FT256AC	256	1.8	3	ftBGA	256	128	C
	LC4256C-5FT256AC	256	1.8	5	ftBGA	256	128	C
	LC4256C-75FT256AC	256	1.8	7.5	ftBGA	256	128	C
	LC4256C-3FT256BC	256	1.8	3	ftBGA	256	160	C
	LC4256C-5FT256BC	256	1.8	5	ftBGA	256	160	C
	LC4256C-75FT256BC	256	1.8	7.5	ftBGA	256	160	C
	LC4256C-3F256AC[1]	256	1.8	3	fpBGA	256	128	C
	LC4256C-5F256AC[1]	256	1.8	5	fpBGA	256	128	C
	LC4256C-75F256AC[1]	256	1.8	7.5	fpBGA	256	128	C
	LC4256C-3F256BC[1]	256	1.8	3	fpBGA	256	160	C
	LC4256C-5F256BC[1]	256	1.8	5	fpBGA	256	160	C
	LC4256C-75F256BC[1]	256	1.8	7.5	fpBGA	256	160	C
	LC4256C-3T176C	256	1.8	3	TQFP	176	128	C
	LC4256C-5T176C	256	1.8	5	TQFP	176	128	C
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256C-3T100C	256	1.8	3	TQFP	100	64	C
	LC4256C-5T100C	256	1.8	5	TQFP	100	64	C
	LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C
LC4384C	LC4384C-35FT256C	384	1.8	3.5	ftBGA	256	192	C
	LC4384C-5FT256C	384	1.8	5	ftBGA	256	192	C
	LC4384C-75FT256C	384	1.8	7.5	ftBGA	256	192	C
	LC4384C-35F256C[1]	384	1.8	3.5	fpBGA	256	192	C
	LC4384C-5F256C[1]	384	1.8	5	fpBGA	256	192	C
	LC4384C-75F256C[1]	384	1.8	7.5	fpBGA	256	192	C
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128	C
	LC4384C-5T176C	384	1.8	5	TQFP	176	128	C
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128	C
LC4512C	LC4512C-35FT256C	512	1.8	3.5	ftBGA	256	208	C
	LC4512C-5FT256C	512	1.8	5	ftBGA	256	208	C
	LC4512C-75FT256C	512	1.8	7.5	ftBGA	256	208	C
	LC4512C-35F256C[1]	512	1.8	3.5	fpBGA	256	208	C
	LC4512C-5F256C[1]	512	1.8	5	fpBGA	256	208	C
	LC4512C-75F256C[1]	512	1.8	7.5	fpBGA	256	208	C
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
	LC4512C-5T176C	512	1.8	5	TQFP	176	128	C
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI[1]	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI[1]	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI[1]	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI[1]	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI[1]	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI[1]	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC[1]	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC[1]	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC[1]	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC[1]	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC[1]	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC[1]	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C[1]	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C[1]	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C[1]	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

ispMACH 4000B (2.5V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128B	LC4128B-5TN128I	128	2.5	5	Lead-Free TQFP	128	92	I
	LC4128B-75TN128I	128	2.5	7.5	Lead-Free TQFP	128	92	I
	LC4128B-10TN128I	128	2.5	10	Lead-Free TQFP	128	92	I
	LC4128B-5TN100I	128	2.5	5	Lead-Free TQFP	100	64	I
	LC4128B-75TN100I	128	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4128B-10TN100I	128	2.5	10	Lead-Free TQFP	100	64	I
LC4256B	LC4256B-5FTN256AI	256	2.5	5	Lead-Free ftBGA	256	128	I
	LC4256B-75FTN256AI	256	2.5	7.5	Lead-Free ftBGA	256	128	I
	LC4256B-10FTN256AI	256	2.5	10	Lead-Free ftBGA	256	128	I
	LC4256B-5FTN256BI	256	2.5	5	Lead-Free ftBGA	256	160	I
	LC4256B-75FTN256BI	256	2.5	7.5	Lead-Free ftBGA	256	160	I
	LC4256B-10FTN256BI	256	2.5	10	Lead-Free ftBGA	256	160	I
	LC4256B-5FN256AI[1]	256	2.5	5	Lead-Free fpBGA	256	128	I
	LC4256B-75FN256AI[1]	256	2.5	7.5	Lead-Free fpBGA	256	128	I
	LC4256B-10FN256AI[1]	256	2.5	10	Lead-Free fpBGA	256	128	I
	LC4256B-5FN256BI[1]	256	2.5	5	Lead-Free fpBGA	256	160	I
	LC4256B-75FN256BI[1]	256	2.5	7.5	Lead-Free fpBGA	256	160	I
	LC4256B-10FN256BI[1]	256	2.5	10	Lead-Free fpBGA	256	160	I
	LC4256B-5TN176I	256	2.5	5	Lead-Free TQFP	176	128	I
	LC4256B-75TN176I	256	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4256B-10TN176I	256	2.5	10	Lead-Free TQFP	176	128	I
	LC4256B-5TN100I	256	2.5	5	Lead-Free TQFP	100	64	I
	LC4256B-75TN100I	256	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4256B-10TN100I	256	2.5	10	Lead-Free TQFP	100	64	I
LC4384B	LC4384B-5FTN256I	384	2.5	5	Lead-Free ftBGA	256	192	I
	LC4384B-75FTN256I	384	2.5	7.5	Lead-Free ftBGA	256	192	I
	LC4384B-10FTN256I	384	2.5	10	Lead-Free ftBGA	256	192	I
	LC4384B-5FN256I[1]	384	2.5	5	Lead-Free fpBGA	256	192	I
	LC4384B-75FN256I[1]	384	2.5	7.5	Lead-Free fpBGA	256	192	I
	LC4384B-10FN256I[1]	384	2.5	10	Lead-Free fpBGA	256	192	I
	LC4384B-5TN176I	384	2.5	5	Lead-Free TQFP	176	128	I
	LC4384B-75TN176I	384	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4384B-10TN176I	384	2.5	10	Lead-Free TQFP	176	128	I
LC4512B	LC4512B-5FTN256I	512	2.5	5	Lead-Free ftBGA	256	208	I
	LC4512B-75FTN256I	512	2.5	7.5	Lead-Free ftBGA	256	208	I
	LC4512B-10FTN256I	512	2.5	10	Lead-Free ftBGA	256	208	I
	LC4512B-5FN256I[1]	512	2.5	5	Lead-Free fpBGA	256	208	I
	LC4512B-75FN256I[1]	512	2.5	7.5	Lead-Free fpBGA	256	208	I
	LC4512B-10FN256I[1]	512	2.5	10	Lead-Free fpBGA	256	208	I
	LC4512B-5TN176I	512	2.5	5	Lead-Free TQFP	176	128	I
	LC4512B-75TN176I	512	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4512B-10TN176I	512	2.5	10	Lead-Free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-3FTN256AC	256	3.3	3	Lead-free ftBGA	256	128	C
	LC4256V-5FTN256AC	256	3.3	5	Lead-free ftBGA	256	128	C
	LC4256V-75FTN256AC	256	3.3	7.5	Lead-free ftBGA	256	128	C
	LC4256V-3FTN256BC	256	3.3	3	Lead-free ftBGA	256	160	C
	LC4256V-5FTN256BC	256	3.3	5	Lead-free ftBGA	256	160	C
	LC4256V-75FTN256BC	256	3.3	7.5	Lead-free ftBGA	256	160	C
	LC4256V-3FN256AC[1]	256	3.3	3	Lead-free fpBGA	256	128	C
	LC4256V-5FN256AC[1]	256	3.3	5	Lead-free fpBGA	256	128	C
	LC4256V-75FN256AC[1]	256	3.3	7.5	Lead-free fpBGA	256	128	C
	LC4256V-3FN256BC[1]	256	3.3	3	Lead-free fpBGA	256	160	C
	LC4256V-5FN256BC[1]	256	3.3	5	Lead-free fpBGA	256	160	C
	LC4256V-75FN256BC[1]	256	3.3	7.5	Lead-free fpBGA	256	160	C
	LC4256V-3TN176C	256	3.3	3	Lead-free TQFP	176	128	C
	LC4256V-5TN176C	256	3.3	5	Lead-free TQFP	176	128	C
	LC4256V-75TN176C	256	3.3	7.5	Lead-free TQFP	176	128	C
	LC4256V-3TN144C	256	3.3	3	Lead-free TQFP	144	96	C
	LC4256V-5TN144C	256	3.3	5	Lead-free TQFP	144	96	C
	LC4256V-75TN144C	256	3.3	7.5	Lead-free TQFP	144	96	C
	LC4256V-3TN100C	256	3.3	3	Lead-free TQFP	100	64	C
	LC4256V-5TN100C	256	3.3	5	Lead-free TQFP	100	64	C
	LC4256V-75TN100C	256	3.3	7.5	Lead-free TQFP	100	64	C
LC4384V	LC4384V-35FTN256C	384	3.3	3.5	Lead-free ftBGA	256	192	C
	LC4384V-5FTN256C	384	3.3	5	Lead-free ftBGA	256	192	C
	LC4384V-75FTN256C	384	3.3	7.5	Lead-free ftBGA	256	192	C
	LC4384V-35FN256C[1]	384	3.3	3.5	Lead-free fpBGA	256	192	C
	LC4384V-5FN256C[1]	384	3.3	5	Lead-free fpBGA	256	192	C
	LC4384V-75FN256C[1]	384	3.3	7.5	Lead-free fpBGA	256	192	C
	LC4384V-35TN176C	384	3.3	3.5	Lead-free TQFP	176	128	C
	LC4384V-5TN176C	384	3.3	5	Lead-free TQFP	176	128	C
	LC4384V-75TN176C	384	3.3	7.5	Lead-free TQFP	176	128	C
LC4512V	LC4512V-35FTN256C	512	3.3	3.5	Lead-free ftBGA	256	208	C
	LC4512V-5FTN256C	512	3.3	5	Lead-free ftBGA	256	208	C
	LC4512V-75FTN256C	512	3.3	7.5	Lead-free ftBGA	256	208	C
	LC4512V-35FN256C[1]	512	3.3	3.5	Lead-free fpBGA	256	208	C
	LC4512V-5FN256C[1]	512	3.3	5	Lead-free fpBGA	256	208	C
	LC4512V-75FN256C[1]	512	3.3	7.5	Lead-free fpBGA	256	208	C
	LC4512V-35TN176C	512	3.3	3.5	Lead-free TQFP	176	128	C
	LC4512V-5TN176C	512	3.3	5	Lead-free TQFP	176	128	C
	LC4512V-75TN176C	512	3.3	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I