# Lattice Semiconductor Corporation - LC4384B-5T176C Datasheet

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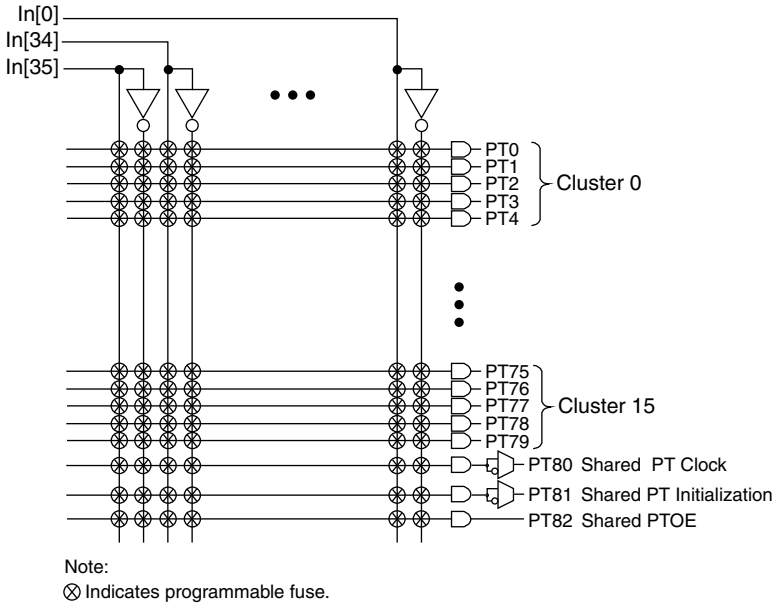
## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5 ns |
| Voltage Supply - Internal | 2.3V ~ 2.7V |
| Number of Logic Elements/Blocks | 24 |
| Number of Macrocells | 384 |
| Number of Gates | - |
| Number of I/O | 128 |
| Operating Temperature | 0°C ~ 90°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-TQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384b-5t176c |

***Figure 3. AND Array***




## Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

***Figure 4. Macrocell Slice***

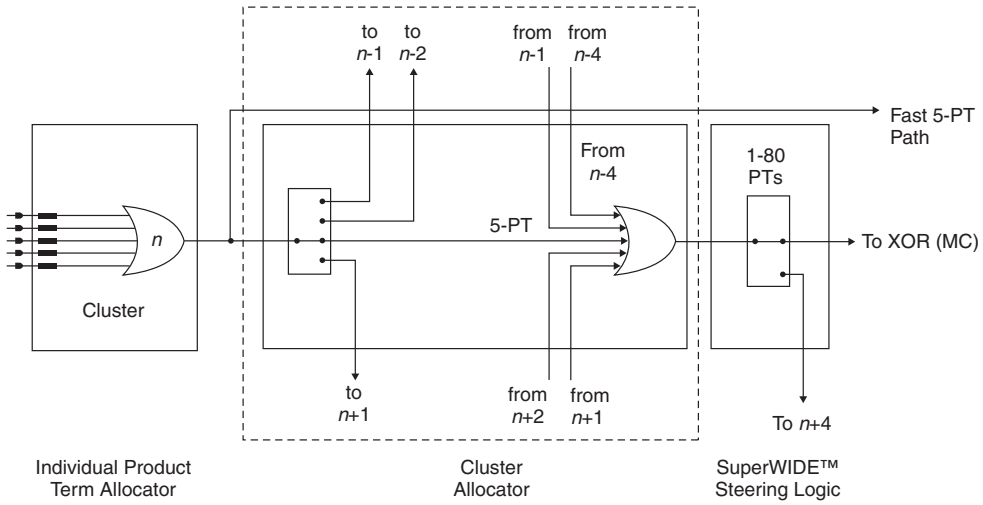


*Table 10. ORP Combinations for I/O Blocks with 12 I/Os*

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M1, M2, M3, M4, M5, M6, M7, M8 |
| I/O 2 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 3 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 4 | M5, M6, M7, M8, M9, M10, M11, M12 |
| I/O 5 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 6 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 7 | M9, M10, M11, M12, M13, M14, M15, M0 |
| I/O 8 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 9 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 10 | M13, M14, M15, M0, M1, M2, M3, M4 |
| I/O 11 | M14, M15, M0, M1, M2, M3, M4, M5 |

### ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster $t_{CO}$.

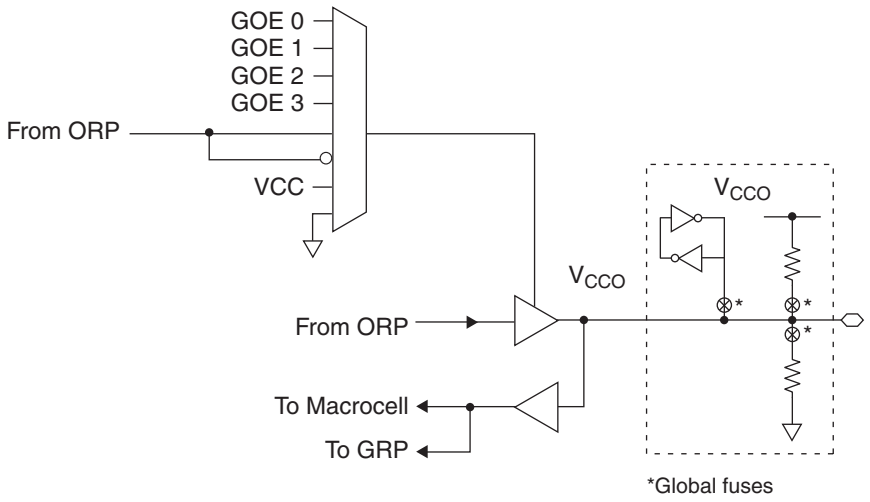
### Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

## I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

*Figure 8. I/O Cell*




Each output supports a variety of output standards dependent on the $V_{CCO}$ supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the $V_{CCO}$ supplied to its I/O bank. The I/O standards supported are:

# I/O Recommended Operating Conditions

| Standard | $V_{CCO}$ (V)[1] | |
|---|---|---|
| | Min. | Max. |
| LVTTL | 3.0 | 3.6 |
| LVCMOS 3.3 | 3.0 | 3.6 |
| Extended LVCMOS 3.3[2] | 2.7 | 3.6 |
| LVCMOS 2.5 | 2.3 | 2.7 |
| LVCMOS 1.8 | 1.65 | 1.95 |
| PCI 3.3 | 3.0 | 3.6 |

1. Typical values for $V_{CCO}$ are the average of the min. and max. values.
2. ispMACH 4000Z only.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4] | Input Leakage Current (ispMACH 4000Z) | $0 \le V_{IN} < V_{CCO}$ | — | 0.5 | 1 | µA |
| $I_{IH}$[1] | Input High Leakage Current (ispMACH 4000Z) | $V_{CCO} < V_{IN} \le 5.5V$ | — | — | 10 | µA |
| $I_{IL}$, $I_{IH}$[1] | Input Leakage Current (ispMACH 4000V/B/C) | $0 \le V_{IN} \le 3.6V$, $T_j = 105°C$ | — | — | 10 | µA |
| | | $0 \le V_{IN} \le 3.6V$, $T_j = 130°C$ | — | — | 15 | µA |
| $I_{IH}$[1,2] | Input High Leakage Current (ispMACH 4000V/B/C) | $3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$<br>$3.0V \le V_{CCO} \le 3.6V$ | — | — | 20 | µA |
| | | $3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$<br>$3.0V \le V_{CCO} \le 3.6V$ | — | — | 50 | µA |
| $I_{PU}$ | I/O Weak Pull-up Resistor Current (ispMACH 4000Z) | $0 \le V_{IN} \le 0.7V_{CCO}$ | -30 | — | -150 | µA |
| | I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C) | $0 \le V_{IN} \le 0.7V_{CCO}$ | -30 | — | -200 | µA |
| $I_{PD}$ | I/O Weak Pull-down Resistor Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MIN) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0V \le V_{IN} \le V_{BHT}$ | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $V_{BHT} \le V_{IN} \le V_{CCO}$ | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | — | $V_{CCO}$ * 0.35 | — | $V_{CCO}$ * 0.65 | V |
| $C_1$ | I/O Capacitance[3] | $V_{CCO} = 3.3V, 2.5V, 1.8V$ | — | 8 | — | pf |
| | | $V_{CC} = 1.8V$, $V_{IO} = 0$ to $V_{IH}$ (MAX) | — | | — | |
| $C_2$ | Clock Capacitance[3] | $V_{CCO} = 3.3V, 2.5V, 1.8V$ | — | 6 | — | pf |
| | | $V_{CC} = 1.8V$, $V_{IO} = 0$ to $V_{IH}$ (MAX) | — | | — | |
| $C_3$ | Global Input Capacitance[3] | $V_{CCO} = 3.3V, 2.5V, 1.8V$ | — | 6 | — | pf |
| | | $V_{CC} = 1.8V$, $V_{IO} = 0$ to $V_{IH}$ (MAX) | — | | — | |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. $T_A = 25°C$, f = 1.0MHz
4. $I_{IH}$ excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

# ispMACH 4000Z External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 3.5 | — | 3.7 | — | 4.2 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 4.4 | — | 4.7 | — | 5.7 | ns |
| $t_S$ | GLB register setup time before clock | 2.2 | — | 2.5 | — | 2.7 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 2.4 | — | 2.7 | — | 2.9 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.0 | — | 1.1 | — | 1.3 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.0 | — | 2.1 | — | 2.6 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.0 | — | 1.0 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.0 | — | 3.2 | — | 3.5 | ns |
| $t_R$ | External reset pin to output delay | — | 5.0 | — | 6.0 | — | 7.3 | ns |
| $t_{RW}$ | External reset pulse duration | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 7.0 | — | 8.0 | — | 8.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 6.5 | — | 7.0 | — | 8.0 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 4.5 | — | 4.5 | — | 4.8 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 267 | — | 250 | — | 220 | MHz |
| $f_{MAX}$ (Ext.) | clock frequency with external feedback, $[1 / (t_S + t_{CO})]$ | — | 192 | — | 175 | — | 161 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

# ispMACH 4000Z External Switching Characteristics (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -45 | | -5 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 4.5 | — | 5.0 | — | 7.5 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 5.8 | — | 6.0 | — | 8.0 | ns |
| $t_S$ | GLB register setup time before clock | 2.9 | — | 3.0 | — | 4.5 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 3.1 | — | 3.2 | — | 4.7 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.3 | — | 1.3 | — | 1.4 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.6 | — | 2.6 | — | 2.7 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.8 | — | 4.2 | — | 4.5 | ns |
| $t_R$ | External reset pin to output delay | — | 7.5 | — | 7.5 | — | 9.0 | ns |
| $t_{RW}$ | External reset pulse duration | 2.0 | — | 2.0 | — | 4.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 8.2 | — | 8.5 | — | 9.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 10.0 | — | 10.0 | — | 10.5 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 5.5 | — | 6.0 | — | 7.0 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.8 | — | 2.0 | — | 2.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.8 | — | 2.0 | — | 2.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.8 | — | 2.0 | — | 2.8 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 200 | — | 200 | — | 168 | MHz |
| $f_{MAX}$ (Ext.) | clock frequency with external feedback, [1 / ($t_S$ + $t_{CO}$)] | — | 150 | — | 139 | — | 111 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

# ispMACH 4000V/B/C Internal Timing Parameters

**Over Recommended Operating Conditions**

| Parameter | Description | -2.5 | | -2.7 | | -3 | | -3.5 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **In/Out Delays** | | | | | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 0.60 | — | 0.60 | — | 0.70 | — | 0.70 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 2.04 | — | 2.54 | — | 3.04 | — | 3.54 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 0.78 | — | 1.28 | — | 1.28 | — | 1.28 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 0.85 | — | 0.85 | — | 0.85 | — | 0.85 | ns |
| $t_{EN}$ | Output Enable Time | — | 0.96 | — | 0.96 | — | 0.96 | — | 0.96 | ns |
| $t_{DIS}$ | Output Disable Time | — | 0.96 | — | 0.96 | — | 0.96 | — | 0.96 | ns |
| **Routing/GLB Delays** | | | | | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 0.61 | — | 0.81 | — | 1.01 | — | 1.01 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 0.45 | — | 0.55 | — | 0.55 | — | 0.65 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 0.11 | — | 0.31 | — | 0.31 | — | 0.31 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| $t_{PDb}$ | 5-PT Bypass Propagation Delay | — | 0.44 | — | 0.44 | — | 0.44 | — | 0.94 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.64 | — | 0.64 | — | 0.64 | — | 0.94 | ns |
| **Register/Latch Delays** | | | | | | | | | | |
| $t_S$ | D-Register Setup Time (Global Clock) | 0.92 | — | 1.12 | — | 1.02 | — | 0.92 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 1.42 | — | 1.32 | — | 1.32 | — | 1.32 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.12 | — | 1.32 | — | 1.22 | — | 1.12 | — | ns |
| $t_{ST\_PT}$ | T-Register Setup Time (Product Term Clock) | 1.42 | — | 1.32 | — | 1.32 | — | 1.32 | — | ns |
| $t_H$ | D-Register Hold Time | 0.88 | — | 0.68 | — | 0.98 | — | 1.08 | — | ns |
| $t_{HT}$ | T-Register Hold Time | 0.88 | — | 0.68 | — | 0.98 | — | 1.08 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 0.82 | — | 1.37 | — | 1.27 | — | 1.27 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 0.88 | — | 0.63 | — | 0.73 | — | 0.73 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 0.88 | — | 0.63 | — | 0.73 | — | 0.73 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.52 | — | 0.52 | — | 0.52 | — | 0.52 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 2.25 | — | 2.25 | — | 2.25 | — | 2.25 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 1.88 | — | 1.88 | — | 1.88 | — | 1.88 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 0.92 | — | 1.12 | — | 1.02 | — | 0.92 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 1.42 | — | 1.32 | — | 1.32 | — | 1.32 | — | ns |
| $t_{HL}$ | Latch Hold Time | 1.17 | — | 1.17 | — | 1.17 | — | 1.17 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.33 | — | 0.33 | — | 0.33 | — | 0.33 | ns |

# ispMACH 4000Z Internal Timing Parameters

**Over Recommended Operating Conditions**

| Parameter | Description | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 0.75 | — | 0.80 | — | 0.75 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 2.25 | — | 2.25 | — | 2.30 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 1.60 | — | 1.60 | — | 1.95 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 0.75 | — | 0.90 | — | 0.90 | ns |
| $t_{EN}$ | Output Enable Time | — | 2.25 | — | 2.25 | — | 2.50 | ns |
| $t_{DIS}$ | Output Disable Time | — | 1.35 | — | 1.35 | — | 2.50 | ns |
| **Routing/GLB Delays** | | | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 1.60 | — | 1.60 | — | 2.15 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 0.65 | — | 0.75 | — | 0.85 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 0.91 | — | 1.00 | — | 1.00 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.05 | — | 0.00 | — | 0.00 | ns |
| $t_{PDb}$ | 5-PT Bypass Propagation Delay | — | 0.40 | — | 0.40 | — | 0.40 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.25 | — | 0.25 | — | 0.65 | ns |
| **Register/Latch Delays** | | | | | | | | |
| $t_{S}$ | D-Register Setup Time (Global Clock) | 0.80 | — | 0.95 | — | 0.90 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 1.35 | — | 1.95 | — | 1.90 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.00 | — | 1.15 | — | 1.10 | — | ns |
| $t_{ST\_PT}$ | T-register Setup Time (Product Term Clock) | 1.55 | — | 1.75 | — | 2.10 | — | ns |
| $t_{H}$ | D-Register Hold Time | 1.40 | — | 1.55 | — | 1.80 | — | ns |
| $t_{HT}$ | T-Resister Hold Time | 1.40 | — | 1.55 | — | 1.80 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 0.94 | — | 0.90 | — | 1.50 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 1.06 | — | 1.20 | — | 1.10 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 0.88 | — | 1.00 | — | 1.00 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.65 | — | 0.70 | — | 0.65 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 1.00 | — | 2.00 | — | 2.00 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 0.80 | — | 0.95 | — | 0.90 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 1.55 | — | 1.95 | — | 1.90 | — | ns |
| $t_{HL}$ | Latch Hold Time | 1.40 | — | 1.80 | — | 1.80 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.40 | — | 0.33 | — | 0.33 | ns |
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.30 | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.28 | — | 0.28 | — | 1.27 | ns |
| $t_{SRR}$ | Asynchronous Reset or Set Recovery Delay | — | 2.00 | — | 1.67 | — | 1.80 | ns |
| **Control Delays** | | | | | | | | |
| $t_{BCLK}$ | GLB PT Clock Delay | — | 1.30 | — | 1.50 | — | 1.55 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | — | 1.50 | — | 1.70 | — | 1.55 | ns |
| $t_{BSR}$ | GLB PT Set/Reset Delay | — | 1.10 | — | 1.83 | — | 1.83 | ns |
| $t_{PTSR}$ | Macrocell PT Set/Reset Delay | — | 1.22 | — | 2.02 | — | 1.83 | ns |

# ispMACH 4000V/B/C Timing Adders[1]

| Adder Type | Base Parameter | Description | -25 | | -27 | | -3 | | -35 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Optional Delay Adders** | | | | | | | | | | | |
| $t_{INDIO}$ | $t_{INREG}$ | Input register delay | — | 0.95 | — | 1.00 | — | 1.00 | — | 1.00 | ns |
| $t_{EXP}$ | $t_{MCELL}$ | Product term expander delay | — | 0.33 | — | 0.33 | — | 0.33 | — | 0.33 | ns |
| $t_{ORP}$ | — | Output routing pool delay | — | 0.05 | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| $t_{BLA}$ | $t_{ROUTE}$ | Additional block loading adder | — | 0.03 | — | 0.05 | — | 0.05 | — | 0.05 | ns |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | | | |
| LVTTL_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVTTL standard | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS33_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 3.3 standard | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS25_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 2.5 standard | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| LVCMOS18_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using LVCMOS 1.8 standard | — | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_in | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | Using PCI compatible input | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.60 | ns |
| **$t_{IOO}$ Output Adjusters** | | | | | | | | | | | |
| LVTTL_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as TTL buffer | — | 0.20 | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS33_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 3.3V buffer | — | 0.20 | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| LVCMOS25_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 2.5V buffer | — | 0.10 | — | 0.10 | — | 0.10 | — | 0.10 | ns |
| LVCMOS18_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as 1.8V buffer | — | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| PCI_out | $t_{BUF}$, $t_{EN}$, $t_{DIS}$ | Output configured as PCI compatible buffer | — | 0.20 | — | 0.20 | — | 0.20 | — | 0.20 | ns |
| Slow Slew | $t_{BUF}$, $t_{EN}$ | Output configured for slow slew rate | — | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | ns |

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

## Signal Descriptions

| Signal Names | Description | |
|---|---|---|
| TMS | Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine. | |
| TCK | Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine. | |
| TDI | Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data. | |
| TDO | Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out. | |
| GOE0/IO, GOE1/IO | These pins are configured to be either Global Output Enable Input or as general I/O pins. | |
| GND | Ground | |
| NC | Not Connected | |
| $V_{CC}$ | The power supply pins for logic core and JTAG port. | |
| CLK0/I, CLK1/I, CLK2/I, CLK3/I | These pins are configured to be either CLK input or as an input. | |
| $V_{CCO0}$, $V_{CCO1}$ | The power supply pins for each I/O bank. | |
| yzz | Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15. | |
| | ispMACH 4032 | y: A-B |
| | ispMACH 4064 | y: A-D |
| | ispMACH 4128 | y: A-H |
| | ispMACH 4256 | y: A-P |
| | ispMACH 4384 | y: A-P, AX-HX |
| | ispMACH 4512 | y: A-P, AX-PX |

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

## ispMACH 4000V/B/C ORP Reference Table

| | 4032V/B/C | | 4064V/B/C | | | 4128V/B/C | | | 4256V/B/C | | | | 4384V/B/C | | 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Number of I/Os | 30[1] | 32 | 30[2] | 32 | 64 | 64 | 92[3] | 96 | 64 | 96[4] | 128 | 160 | 128 | 192 | 128 | 208 |
| Number of GLBs | 2 | 2 | 4 | 4 | 4 | 8 | 8 | 8 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| Number of I/Os / GLB | 16 | 16 | 8 | 8 | 16 | 8 | 12 | 12 | 4 | 8 | 8 | 10 | 8 | 8 | 8 | Mixture of 8 & 4[5] |
| Reference ORP Table | 16 I/Os / GLB | | 8 I/Os / GLB | | 16 I/Os / GLB | 8 I/Os / GLB | 12 I/Os / GLB | | 4 I/Os / GLB | 8 I/Os / GLB | 8 I/Os / GLB | 10 I/Os / GLB | 8 I/Os / GLB | | 8 I/Os / GLB | 8 I/Os / GLB 4 I/Os / GLB |

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.
2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.
3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os
4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per
5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

## ispMACH 4000Z ORP Reference Table

| | 4032Z | 4064Z | | 4128Z | | 4256Z | | |
|---|---|---|---|---|---|---|---|---|
| Number of I/Os | 32 | 32 | 64 | 64 | 96 | 64 | 96[1] | 128 |
| Number of GLBs | 2 | 4 | 4 | 8 | 8 | 16 | 16 | 16 |
| Number of I/Os / GLB | 16 | 8 | 16 | 8 | 12 | 4 | 8 | 8 |
| Reference ORP Table | 16 I/Os / GLB | 8 I/Os / GLB | 16 I/Os / GLB | 8 I/Os / GLB | 12 I/Os / GLB | 4 I/Os / GLB | 8 I/Os / GLB | 8 I/Os / GLB |

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

## ispMACH 4000V/B/C/Z Power Supply and NC Connections[1]

| Signal | 44-pin TQFP[2] | 48-pin TQFP[2] | 56-ball csBGA[3] | 100-pin TQFP[2] | 128-pin TQFP[2] |
|---|---|---|---|---|---|
| VCC | 11, 33 | 12, 36 | K2, A9 | 25, 40, 75, 90 | 32, 51, 96, 115 |
| VCCO0<br>VCCO (Bank 0) | 6 | 6 | F3 | 13, 33, 95 | 3, 17, 30, 41, 122 |
| VCCO1<br>VCCO (Bank 1) | 28 | 30 | E8 | 45, 63, 83 | 58, 67, 81, 94, 105 |
| GND | 12, 34 | 13, 37 | H3, C8 | 1, 26, 51, 76 | 1, 33, 65, 97 |
| GND (Bank 0) | 5 | 5 | D3 | 7, 18, 32, 96 | 10, 24, 40, 113, 123 |
| GND (Bank 1) | 27 | 29 | G8 | 46, 57, 68, 82 | 49, 59, 74, 88, 104 |
| NC | — | — | **4032Z**: A8, B10, E1, E3, F8, F10, J1, K3 | — | — |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

## ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4032V/B/C | | ispMACH 4064V/B/C | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 42 | 0 | A2 | A^2 | A4 | A^2 |
| 43 | 0 | A3 | A^3 | A6 | A^3 |
| 44 | 0 | A4 | A^4 | A8 | A^4 |

## ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP

| Pin Number | Bank Number | ispMACH 4032V/B/C/Z | | ispMACH 4064V/B/C | | ispMACH 4064Z | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 1 | - | TDI | - | TDI | - | TDI | - |
| 2 | 0 | A5 | A^5 | A10 | A^5 | A8 | A^5 |
| 3 | 0 | A6 | A^6 | A12 | A^6 | A10 | A^6 |
| 4 | 0 | A7 | A^7 | A14 | A^7 | A11 | A^7 |
| 5 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 6 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 7 | 0 | A8 | A^8 | B0 | B^0 | B15 | B^7 |
| 8 | 0 | A9 | A^9 | B2 | B^1 | B12 | B^6 |
| 9 | 0 | A10 | A^10 | B4 | B^2 | B10 | B^5 |
| 10 | 0 | A11 | A^11 | B6 | B^3 | B8 | B^4 |
| 11 | - | TCK | - | TCK | - | TCK | - |
| 12 | - | VCC | - | VCC | - | VCC | - |
| 13 | - | GND | - | GND | - | GND | - |
| 14 | 0 | A12 | A^12 | B8 | B^4 | B6 | B^3 |
| 15 | 0 | A13 | A^13 | B10 | B^5 | B4 | B^2 |
| 16 | 0 | A14 | A^14 | B12 | B^6 | B2 | B^1 |
| 17 | 0 | A15 | A^15 | B14 | B^7 | B0 | B^0 |
| 18 | 0 | CLK1/I | - | CLK1/I | - | CLK1/I | - |
| 19 | 1 | CLK2/I | - | CLK2/I | - | CLK2/I | - |
| 20 | 1 | B0 | B^0 | C0 | C^0 | C0 | C^0 |
| 21 | 1 | B1 | B^1 | C2 | C^1 | C1 | C^1 |
| 22 | 1 | B2 | B^2 | C4 | C^2 | C2 | C^2 |
| 23 | 1 | B3 | B^3 | C6 | C^3 | C4 | C^3 |
| 24 | 1 | B4 | B^4 | C8 | C^4 | C6 | C^4 |
| 25 | - | TMS | - | TMS | - | TMS | - |
| 26 | 1 | B5 | B^5 | C10 | C^5 | C8 | C^5 |
| 27 | 1 | B6 | B^6 | C12 | C^6 | C10 | C^6 |
| 28 | 1 | B7 | B^7 | C14 | C^7 | C11 | C^7 |
| 29 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| 30 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 31 | 1 | B8 | B^8 | D0 | D^0 | D15 | D^7 |
| 32 | 1 | B9 | B^9 | D2 | D^1 | D12 | D^6 |

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 19 | 0 | C13 | C^10 |
| 20 | 0 | C12 | C^9 |
| 21 | 0 | C10 | C^8 |
| 22 | 0 | C9 | C^7 |
| 23 | 0 | C8 | C^6 |
| 24 | 0 | GND (Bank 0) | - |
| 25 | 0 | C6 | C^5 |
| 26 | 0 | C5 | C^4 |
| 27 | 0 | C4 | C^3 |
| 28 | 0 | C2 | C^2 |
| 29 | 0 | C0 | C^0 |
| 30 | 0 | VCCO (Bank 0) | - |
| 31 | 0 | TCK | - |
| 32 | 0 | VCC | - |
| 33 | 0 | GND | - |
| 34 | 0 | D14 | D^11 |
| 35 | 0 | D13 | D^10 |
| 36 | 0 | D12 | D^9 |
| 37 | 0 | D10 | D^8 |
| 38 | 0 | D9 | D^7 |
| 39 | 0 | D8 | D^6 |
| 40 | 0 | GND (Bank 0) | - |
| 41 | 0 | VCCO (Bank 0) | - |
| 42 | 0 | D6 | D^5 |
| 43 | 0 | D5 | D^4 |
| 44 | 0 | D4 | D^3 |
| 45 | 0 | D2 | D^2 |
| 46 | 0 | D1 | D^1 |
| 47 | 0 | D0 | D^0 |
| 48 | 0 | CLK1/I | - |
| 49 | 1 | GND (Bank 1) | - |
| 50 | 1 | CLK2/I | - |
| 51 | 1 | VCC | - |
| 52 | 1 | E0 | E^0 |
| 53 | 1 | E1 | E^1 |
| 54 | 1 | E2 | E^2 |
| 55 | 1 | E4 | E^3 |
| 56 | 1 | E5 | E^4 |
| 57 | 1 | E6 | E^5 |
| 58 | 1 | VCCO (Bank 1) | - |
| 59 | 1 | GND (Bank 1) | - |
| 60 | 1 | E8 | E^6 |
| 61 | 1 | E9 | E^7 |

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 105 | 1 | VCCO (Bank 1) | - |
| 106 | 1 | H6 | H^5 |
| 107 | 1 | H5 | H^4 |
| 108 | 1 | H4 | H^3 |
| 109 | 1 | H2 | H^2 |
| 110 | 1 | H1 | H^1 |
| 111 | 1 | H0/GOE1 | H^0 |
| 112 | 1 | CLK3/I | - |
| 113 | 0 | GND (Bank 0) | - |
| 114 | 0 | CLK0/I | - |
| 115 | 0 | VCC | - |
| 116 | 0 | A0/GOE0 | A^0 |
| 117 | 0 | A1 | A^1 |
| 118 | 0 | A2 | A^2 |
| 119 | 0 | A4 | A^3 |
| 120 | 0 | A5 | A^4 |
| 121 | 0 | A6 | A^5 |
| 122 | 0 | VCCO (Bank 0) | - |
| 123 | 0 | GND (Bank 0) | - |
| 124 | 0 | A8 | A^6 |
| 125 | 0 | A9 | A^7 |
| 126 | 0 | A10 | A^8 |
| 127 | 0 | A12 | A^9 |
| 128 | 0 | A14 | A^11 |

## ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA

| Ball Number | Bank Number | ispMACH 4064Z | | ispMACH 4128Z | | ispMACH 4256Z | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| B1 | - | GND | - | GND | - | GND | - |
| B2 | - | TDI | - | TDI | - | TDI | - |
| C1 | 0 | NC | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| C3 | 0 | NC | - | B0 | B^0 | C12 | C^6 |
| C2 | 0 | A8 | A^8 | B1 | B^1 | C10 | C^5 |
| D1 | 0 | A9 | A^9 | B2 | B^2 | C8 | C^4 |
| D3 | 0 | A10 | A^10 | B4 | B^3 | C6 | C^3 |
| D2 | 0 | A11 | A^11 | B5 | B^4 | C4 | C^2 |
| E1 | 0 | NC | | B6 | B^5 | C2 | C^1 |
| E2 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |

## ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

| Pin Number | Bank Number | ispMACH 4128V | | ispMACH 4256V | |
|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 1 | - | GND | - | GND | - |
| 2 | - | TDI | - | TDI | - |
| 3 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 4 | 0 | B0 | B^0 | C12 | C^6 |
| 5 | 0 | B1 | B^1 | C10 | C^5 |
| 6 | 0 | B2 | B^2 | C8 | C^4 |
| 7 | 0 | B4 | B^3 | C6 | C^3 |
| 8 | 0 | B5 | B^4 | C4 | C^2 |
| 9 | 0 | B6 | B^5 | C2 | C^1 |
| 10 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 11 | 0 | B8 | B^6 | D14 | D^7 |
| 12 | 0 | B9 | B^7 | D12 | D^6 |
| 13 | 0 | B10 | B^8 | D10 | D^5 |
| 14 | 0 | B12 | B^9 | D8 | D^4 |
| 15 | 0 | B13 | B^10 | D6 | D^3 |
| 16 | 0 | B14 | B^11 | D4 | D^2 |
| 17 | - | NC[2] | - | I[2] | - |
| 18 | 0 | GND (Bank 0)[1] | - | NC[1] | - |
| 19 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 20 | 0 | NC[2] | - | I[2] | - |
| 21 | 0 | C14 | C^11 | E2 | E^1 |
| 22 | 0 | C13 | C^10 | E4 | E^2 |
| 23 | 0 | C12 | C^9 | E6 | E^3 |
| 24 | 0 | C10 | C^8 | E8 | E^4 |
| 25 | 0 | C9 | C^7 | E10 | E^5 |
| 26 | 0 | C8 | C^6 | E12 | E^6 |
| 27 | 0 | GND (Bank 0) | - | GND (Bank 0) | - |
| 28 | 0 | C6 | C^5 | F2 | F^1 |
| 29 | 0 | C5 | C^4 | F4 | F^2 |
| 30 | 0 | C4 | C^3 | F6 | F^3 |
| 31 | 0 | C2 | C^2 | F8 | F^4 |
| 32 | 0 | C1 | C^1 | F10 | F^5 |
| 33 | 0 | C0 | C^0 | F12 | F^6 |
| 34 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 35 | - | TCK | - | TCK | - |
| 36 | - | VCC | - | VCC | - |
| 37 | - | GND | - | GND | - |
| 38 | 0 | NC[2] | - | I[2] | - |
| 39 | 0 | D14 | D^11 | G12 | G^6 |
| 40 | 0 | D13 | D^10 | G10 | G^5 |
| 41 | 0 | D12 | D^9 | G8 | G^4 |
| 42 | 0 | D10 | D^8 | G6 | G^3 |

## ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4256V/B/C/Z | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 60 | 0 | H8 | H^4 | L8 | L^4 | P8 | P^4 |
| 61 | 0 | H6 | H^3 | L6 | L^3 | P6 | P^3 |
| 62 | 0 | H4 | H^2 | L4 | L^2 | P4 | P^2 |
| 63 | 0 | H2 | H^1 | L2 | L^1 | P2 | P^1 |
| 64 | 0 | H0 | H^0 | L0 | L^0 | P0 | P^0 |
| 65 | - | GND | - | GND | - | GND | - |
| 66 | 0 | CLK1/I | - | CLK1/I | - | CLK1/I | - |
| 67 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| 68 | 1 | CLK2/I | - | CLK2/I | - | CLK2/I | - |
| 69 | - | VCC | - | VCC | - | VCC | - |
| 70 | 1 | I0 | I^0 | M0 | M^0 | AX0 | AX^0 |
| 71 | 1 | I2 | I^1 | M2 | M^1 | AX2 | AX^1 |
| 72 | 1 | I4 | I^2 | M4 | M^2 | AX4 | AX^2 |
| 73 | 1 | I6 | I^3 | M6 | M^3 | AX6 | AX^3 |
| 74 | 1 | I8 | I^4 | M8 | M^4 | AX8 | AX^4 |
| 75 | 1 | I10 | I^5 | M10 | M^5 | AX10 | AX^5 |
| 76 | 1 | I12 | I^6 | M12 | M^6 | AX12 | AX^6 |
| 77 | 1 | I14 | I^7 | M14 | M^7 | AX14 | AX^7 |
| 78 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 79 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| 80 | 1 | J0 | J^0 | N0 | N^0 | BX0 | BX^0 |
| 81 | 1 | J2 | J^1 | N2 | N^1 | BX2 | BX^1 |
| 82 | 1 | J4 | J^2 | N4 | N^2 | BX4 | BX^2 |
| 83 | 1 | J6 | J^3 | N6 | N^3 | BX6 | BX^3 |
| 84 | 1 | J8 | J^4 | N8 | N^4 | BX8 | BX^4 |
| 85 | 1 | J10 | J^5 | N10 | N^5 | BX10 | BX^5 |
| 86 | 1 | J12 | J^6 | N12 | N^6 | BX12 | BX^6 |
| 87 | 1 | J14 | J^7 | N14 | N^7 | BX14 | BX^7 |
| 88 | - | VCC | - | VCC | - | VCC | - |
| 89 | - | NC | - | NC | - | NC | - |
| 90 | - | GND | - | GND | - | GND | - |
| 91 | - | TMS | - | TMS | - | TMS | - |
| 92 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 93 | 1 | K14 | K^7 | O14 | O^7 | CX14 | CX^7 |
| 94 | 1 | K12 | K^6 | O12 | O^6 | CX12 | CX^6 |
| 95 | 1 | K10 | K^5 | O10 | O^5 | CX10 | CX^5 |
| 96 | 1 | K8 | K^4 | O8 | O^4 | CX8 | CX^4 |
| 97 | 1 | K6 | K^3 | O6 | O^3 | CX6 | CX^3 |
| 98 | 1 | K4 | K^2 | O4 | O^2 | CX4 | CX^2 |
| 99 | 1 | K2 | K^1 | O2 | O^1 | CX2 | CX^1 |
| 100 | 1 | K0 | K^0 | O0 | O^0 | CX0 | CX^0 |

**ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | tPD | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4064ZC | LC4064ZC-5M132I | 64 | 1.8 | 5 | csBGA | 132 | 64 | I |
| | LC4064ZC-75M132I | 64 | 1.8 | 7.5 | csBGA | 132 | 64 | I |
| | LC4064ZC-5T100I | 64 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4064ZC-75T100I | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4064ZC-5M56I | 64 | 1.8 | 5 | csBGA | 56 | 34 | I |
| | LC4064ZC-75M56I | 64 | 1.8 | 7.5 | csBGA | 56 | 34 | I |
| | LC4064ZC-5T48I | 64 | 1.8 | 5 | TQFP | 48 | 32 | I |
| | LC4064ZC-75T48I | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | I |
| LC4128ZC | LC4128ZC-75M132I | 128 | 1.8 | 7.5 | csBGA | 132 | 96 | I |
| | LC4128ZC-75T100I | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| LC4256ZC | LC4256ZC-75T176I | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4256ZC-75M132I | 256 | 1.8 | 7.5 | csBGA | 132 | 96 | I |
| | LC4256ZC-75T100I | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | I |

**ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZC | LC4032ZC-75T48E | 32 | 1.8 | 7.5 | TQFP | 48 | 32 | E |
| LC4064ZC | LC4064ZC-75T100E | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | E |
| | LC4064ZC-75T48E | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | E |
| LC4128ZC | LC4128ZC-75T100E | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | E |
| LC4256ZC | LC4256ZC-75T176E | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | E |
| | LC4256ZC-75T100E | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | E |

**ispMACH 4000C (1.8V) Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032C | LC4032C-25T48C | 32 | 1.8 | 2.5 | TQFP | 48 | 32 | C |
| | LC4032C-5T48C | 32 | 1.8 | 5 | TQFP | 48 | 32 | C |
| | LC4032C-75T48C | 32 | 1.8 | 7.5 | TQFP | 48 | 32 | C |
| | LC4032C-25T44C | 32 | 1.8 | 2.5 | TQFP | 44 | 30 | C |
| | LC4032C-5T44C | 32 | 1.8 | 5 | TQFP | 44 | 30 | C |
| | LC4032C-75T44C | 32 | 1.8 | 7.5 | TQFP | 44 | 30 | C |
| LC4064C | LC4064C-25T100C | 64 | 1.8 | 2.5 | TQFP | 100 | 64 | C |
| | LC4064C-5T100C | 64 | 1.8 | 5 | TQFP | 100 | 64 | C |
| | LC4064C-75T100C | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | C |
| | LC4064C-25T48C | 64 | 1.8 | 2.5 | TQFP | 48 | 32 | C |
| | LC4064C-5T48C | 64 | 1.8 | 5 | TQFP | 48 | 32 | C |
| | LC4064C-75T48C | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | C |
| | LC4064C-25T44C | 64 | 1.8 | 2.5 | TQFP | 44 | 30 | C |
| | LC4064C-5T44C | 64 | 1.8 | 5 | TQFP | 44 | 30 | C |
| | LC4064C-75T44C | 64 | 1.8 | 7.5 | TQFP | 44 | 30 | C |

**ispMACH 4000C (1.8V) Industrial Devices**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032C | LC4032C-5T48I | 32 | 1.8 | 5 | TQFP | 48 | 32 | I |
| | LC4032C-75T48I | 32 | 1.8 | 7.5 | TQFP | 48 | 32 | I |
| | LC4032C-10T48I | 32 | 1.8 | 10 | TQFP | 48 | 32 | I |
| | LC4032C-5T44I | 32 | 1.8 | 5 | TQFP | 44 | 30 | I |
| | LC4032C-75T44I | 32 | 1.8 | 7.5 | TQFP | 44 | 30 | I |
| | LC4032C-10T44I | 32 | 1.8 | 10 | TQFP | 44 | 30 | I |
| LC4064C | LC4064C-5T100I | 64 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4064C-75T100I | 64 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4064C-10T100I | 64 | 1.8 | 10 | TQFP | 100 | 64 | I |
| | LC4064C-5T48I | 64 | 1.8 | 5 | TQFP | 48 | 32 | I |
| | LC4064C-75T48I | 64 | 1.8 | 7.5 | TQFP | 48 | 32 | I |
| | LC4064C-10T48I | 64 | 1.8 | 10 | TQFP | 48 | 32 | I |
| | LC4064C-5T44I | 64 | 1.8 | 5 | TQFP | 44 | 30 | I |
| | LC4064C-75T44I | 64 | 1.8 | 7.5 | TQFP | 44 | 30 | I |
| | LC4064C-10T44I | 64 | 1.8 | 10 | TQFP | 44 | 30 | I |
| LC4128C | LC4128C-5T128I | 128 | 1.8 | 5 | TQFP | 128 | 92 | I |
| | LC4128C-75T128I | 128 | 1.8 | 7.5 | TQFP | 128 | 92 | I |
| | LC4128C-10T128I | 128 | 1.8 | 10 | TQFP | 128 | 92 | I |
| | LC4128C-5T100I | 128 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4128C-75T100I | 128 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4128C-10T100I | 128 | 1.8 | 10 | TQFP | 100 | 64 | I |
| LC4256C | LC4256C-5FT256AI | 256 | 1.8 | 5 | ftBGA | 256 | 128 | I |
| | LC4256C-75FT256AI | 256 | 1.8 | 7.5 | ftBGA | 256 | 128 | I |
| | LC4256C-10FT256AI | 256 | 1.8 | 10 | ftBGA | 256 | 128 | I |
| | LC4256C-5FT256BI | 256 | 1.8 | 5 | ftBGA | 256 | 160 | I |
| | LC4256C-75FT256BI | 256 | 1.8 | 7.5 | ftBGA | 256 | 160 | I |
| | LC4256C-10FT256BI | 256 | 1.8 | 10 | ftBGA | 256 | 160 | I |
| | LC4256C-5F256AI[1] | 256 | 1.8 | 5 | fpBGA | 256 | 128 | I |
| | LC4256C-75F256AI[1] | 256 | 1.8 | 7.5 | fpBGA | 256 | 128 | I |
| | LC4256C-10F256AI[1] | 256 | 1.8 | 10 | fpBGA | 256 | 128 | I |
| | LC4256C-5F256BI[1] | 256 | 1.8 | 5 | fpBGA | 256 | 160 | I |
| | LC4256C-75F256BI[1] | 256 | 1.8 | 7.5 | fpBGA | 256 | 160 | I |
| | LC4256C-10F256BI[1] | 256 | 1.8 | 10 | fpBGA | 256 | 160 | I |
| | LC4256C-5T176I | 256 | 1.8 | 5 | TQFP | 176 | 128 | I |
| | LC4256C-75T176I | 256 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4256C-10T176I | 256 | 1.8 | 10 | TQFP | 176 | 128 | I |
| | LC4256C-5T100I | 256 | 1.8 | 5 | TQFP | 100 | 64 | I |
| | LC4256C-75T100I | 256 | 1.8 | 7.5 | TQFP | 100 | 64 | I |
| | LC4256C-10T100I | 256 | 1.8 | 10 | TQFP | 100 | 64 | I |

**ispMACH 4000C (1.8V) Industrial Devices (Cont.)**

| Family | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4384C | LC4384C-5FT256I | 384 | 1.8 | 5 | ftBGA | 256 | 192 | I |
| | LC4384C-75FT256I | 384 | 1.8 | 7.5 | ftBGA | 256 | 192 | I |
| | LC4384C-10FT256I | 384 | 1.8 | 10 | ftBGA | 256 | 192 | I |
| | LC4384C-5F256I[1] | 384 | 1.8 | 5 | fpBGA | 256 | 192 | I |
| | LC4384C-75F256I[1] | 384 | 1.8 | 7.5 | fpBGA | 256 | 192 | I |
| | LC4384C-10F256I[1] | 384 | 1.8 | 10 | fpBGA | 256 | 192 | I |
| | LC4384C-5T176I | 384 | 1.8 | 5 | TQFP | 176 | 128 | I |
| | LC4384C-75T176I | 384 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4384C-10T176I | 384 | 1.8 | 10 | TQFP | 176 | 128 | I |
| LC4512C | LC4512C-5FT256I | 512 | 1.8 | 5 | ftBGA | 256 | 208 | I |
| | LC4512C-75FT256I | 512 | 1.8 | 7.5 | ftBGA | 256 | 208 | I |
| | LC4512C-10FT256I | 512 | 1.8 | 10 | ftBGA | 256 | 208 | I |
| | LC4512C-5F256I[1] | 512 | 1.8 | 5 | fpBGA | 256 | 208 | I |
| | LC4512C-75F256I[1] | 512 | 1.8 | 7.5 | fpBGA | 256 | 208 | I |
| | LC4512C-10F256I[1] | 512 | 1.8 | 10 | fpBGA | 256 | 208 | I |
| | LC4512C-5T176I | 512 | 1.8 | 5 | TQFP | 176 | 128 | I |
| | LC4512C-75T176I | 512 | 1.8 | 7.5 | TQFP | 176 | 128 | I |
| | LC4512C-10T176I | 512 | 1.8 | 10 | TQFP | 176 | 128 | I |

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**ispMACH 4000B (2.5V) Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032B | LC4032B-25T48C | 32 | 2.5 | 2.5 | TQFP | 48 | 32 | C |
| | LC4032B-5T48C | 32 | 2.5 | 5 | TQFP | 48 | 32 | C |
| | LC4032B-75T48C | 32 | 2.5 | 7.5 | TQFP | 48 | 32 | C |
| | LC4032B-25T44C | 32 | 2.5 | 2.5 | TQFP | 44 | 30 | C |
| | LC4032B-5T44C | 32 | 2.5 | 5 | TQFP | 44 | 30 | C |
| | LC4032B-75T44C | 32 | 2.5 | 7.5 | TQFP | 44 | 30 | C |
| LC4064B | LC4064B-25T100C | 64 | 2.5 | 2.5 | TQFP | 100 | 64 | C |
| | LC4064B-5T100C | 64 | 2.5 | 5 | TQFP | 100 | 64 | C |
| | LC4064B-75T100C | 64 | 2.5 | 7.5 | TQFP | 100 | 64 | C |
| | LC4064B-25T48C | 64 | 2.5 | 2.5 | TQFP | 48 | 32 | C |
| | LC4064B-5T48C | 64 | 2.5 | 5 | TQFP | 48 | 32 | C |
| | LC4064B-75T48C | 64 | 2.5 | 7.5 | TQFP | 48 | 32 | C |
| | LC4064B-25T44C | 64 | 2.5 | 2.5 | TQFP | 44 | 30 | C |
| | LC4064B-5T44C | 64 | 2.5 | 5 | TQFP | 44 | 30 | C |
| | LC4064B-75T44C | 64 | 2.5 | 7.5 | TQFP | 44 | 30 | C |
| LC4128B | LC4128B-27T128C | 128 | 2.5 | 2.7 | TQFP | 128 | 92 | C |
| | LC4128B-5T128C | 128 | 2.5 | 5 | TQFP | 128 | 92 | C |
| | LC4128B-75T128C | 128 | 2.5 | 7.5 | TQFP | 128 | 92 | C |
| | LC4128B-27T100C | 128 | 2.5 | 2.7 | TQFP | 100 | 64 | C |
| | LC4128B-5T100C | 128 | 2.5 | 5 | TQFP | 100 | 64 | C |
| | LC4128B-75T100C | 128 | 2.5 | 7.5 | TQFP | 100 | 64 | C |

## Lead-Free Packaging

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZC | LC4032ZC-35MN56C | 32 | 1.8 | 3.5 | Lead-free csBGA | 56 | 32 | C |
| | LC4032ZC-5MN56C | 32 | 1.8 | 5 | Lead-free csBGA | 56 | 32 | C |
| | LC4032ZC-75MN56C | 32 | 1.8 | 7.5 | Lead-free csBGA | 56 | 32 | C |
| | LC4032ZC-35TN48C | 32 | 1.8 | 3.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032ZC-5TN48C | 32 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032ZC-75TN48C | 32 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| LC4064ZC | LC4064ZC-37MN132C | 64 | 1.8 | 3.7 | Lead-free csBGA | 132 | 64 | C |
| | LC4064ZC-5MN132C | 64 | 1.8 | 5 | Lead-free csBGA | 132 | 64 | C |
| | LC4064ZC-75MN132C | 64 | 1.8 | 7.5 | Lead-free csBGA | 132 | 64 | C |
| | LC4064ZC-37TN100C | 64 | 1.8 | 3.7 | Lead-free TQFP | 100 | 64 | C |
| | LC4064ZC-5TN100C | 64 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064ZC-75TN100C | 64 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064ZC-37MN56C | 64 | 1.8 | 3.7 | Lead-free csBGA | 56 | 32 | C |
| | LC4064ZC-5MN56C | 64 | 1.8 | 5 | Lead-free csBGA | 56 | 32 | C |
| | LC4064ZC-75MN56C | 64 | 1.8 | 7.5 | Lead-free csBGA | 56 | 32 | C |
| | LC4064ZC-37TN48C | 64 | 1.8 | 3.7 | Lead-free TQFP | 48 | 32 | C |
| | LC4064ZC-5TN48C | 64 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064ZC-75TN48C | 64 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| LC4128ZC | LC4128ZC-42MN132C | 128 | 1.8 | 4.2 | Lead-free csBGA | 132 | 96 | C |
| | LC4128ZC-75MN132C | 128 | 1.8 | 7.5 | Lead-free csBGA | 132 | 96 | C |
| | LC4128ZC-42TN100C | 128 | 1.8 | 4.2 | Lead-free TQFP | 100 | 64 | C |
| | LC4128ZC-75TN100C | 128 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| LC4256ZC | LC4256ZC-45TN176C | 256 | 1.8 | 4.5 | Lead-free TQFP | 176 | 128 | C |
| | LC4256ZC-75TN176C | 256 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | C |
| | LC4256ZC-45MN132C | 256 | 1.8 | 4.5 | Lead-free csBGA | 132 | 96 | C |
| | LC4256ZC-75MN132C | 256 | 1.8 | 7.5 | Lead-free csBGA | 132 | 96 | C |
| | LC4256ZC-45TN100C | 256 | 1.8 | 4.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4256ZC-75TN100C | 256 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZC | LC4032ZC-5MN56I | 32 | 1.8 | 5 | Lead-free csBGA | 56 | 32 | I |
| | LC4032ZC-75MN56I | 32 | 1.8 | 7.5 | Lead-free csBGA | 56 | 32 | I |
| | LC4032ZC-5TN48I | 32 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | I |
| | LC4032ZC-75TN48I | 32 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | I |

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4064ZC | LC4064ZC-5MN132I | 64 | 1.8 | 5 | Lead-free csBGA | 132 | 64 | I |
| | LC4064ZC-75MN132I | 64 | 1.8 | 7.5 | Lead-free csBGA | 132 | 64 | I |
| | LC4064ZC-5TN100I | 64 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | I |
| | LC4064ZC-75TN100I | 64 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | I |
| | LC4064ZC-5MN56I | 64 | 1.8 | 5 | Lead-free csBGA | 56 | 32 | I |
| | LC4064ZC-75MN56I | 64 | 1.8 | 7.5 | Lead-free csBGA | 56 | 32 | I |
| | LC4064ZC-5TN48I | 64 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | I |
| | LC4064ZC-75TN48I | 64 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | I |
| LC4128ZC | LC4128ZC-75MN132I | 128 | 1.8 | 7.5 | Lead-free csBGA | 132 | 96 | I |
| | LC4128ZC-75TN100I | 128 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | I |
| LC4256ZC | LC4256ZC-75TN176I | 256 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | I |
| | LC4256ZC-75MN132I | 256 | 1.8 | 7.5 | Lead-free csBGA | 132 | 96 | I |
| | LC4256ZC-75TN100I | 256 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | I |

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZC | LC4032ZC-75TN48E | 32 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | E |
| LC4064ZC | LC4064ZC-75TN100E | 64 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | E |
| | LC4064ZC-75TN48E | 64 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | E |
| LC4128ZC | LC4128ZC-75TN100E | 128 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | E |
| LC4256ZC | LC4256ZC-75TN176E | 256 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | E |
| | LC4256ZC-75TN100E | 256 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | E |

**ispMACH 4000C (1.8V) Lead-Free Commercial Devices**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032C | LC4032C-25TN48C | 32 | 1.8 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032C-5TN48C | 32 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032C-75TN48C | 32 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4032C-25TN44C | 32 | 1.8 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4032C-5TN44C | 32 | 1.8 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4032C-75TN44C | 32 | 1.8 | 7.5 | Lead-free TQFP | 44 | 30 | C |