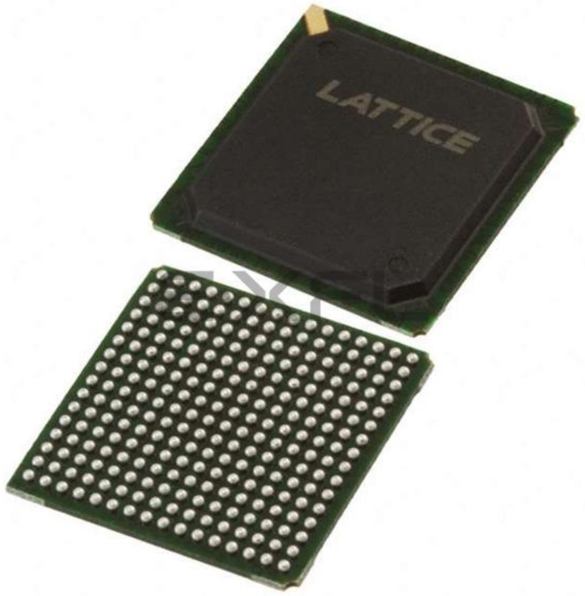
Lattice Semiconductor Corporation - LC4384B-75F256C Datasheet



Welcome to E-XFL.COM

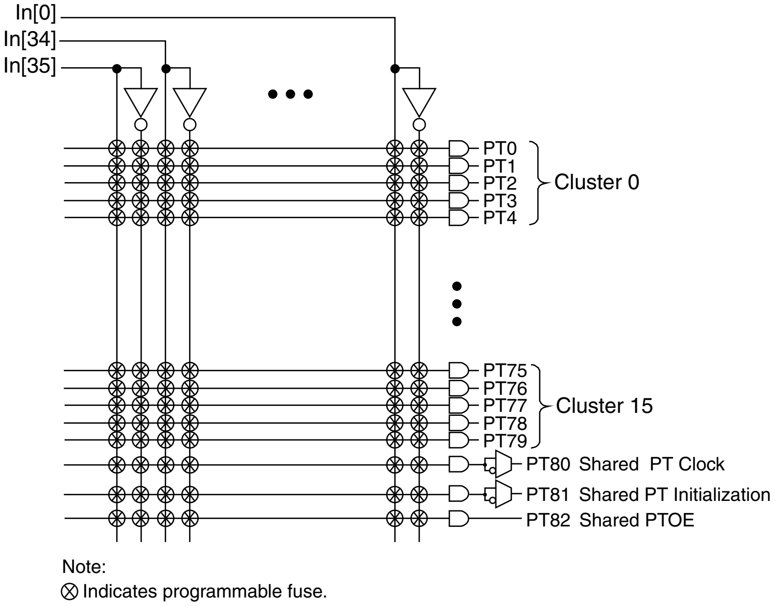
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	192
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384b-75f256c

Figure 3. AND Array



Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice

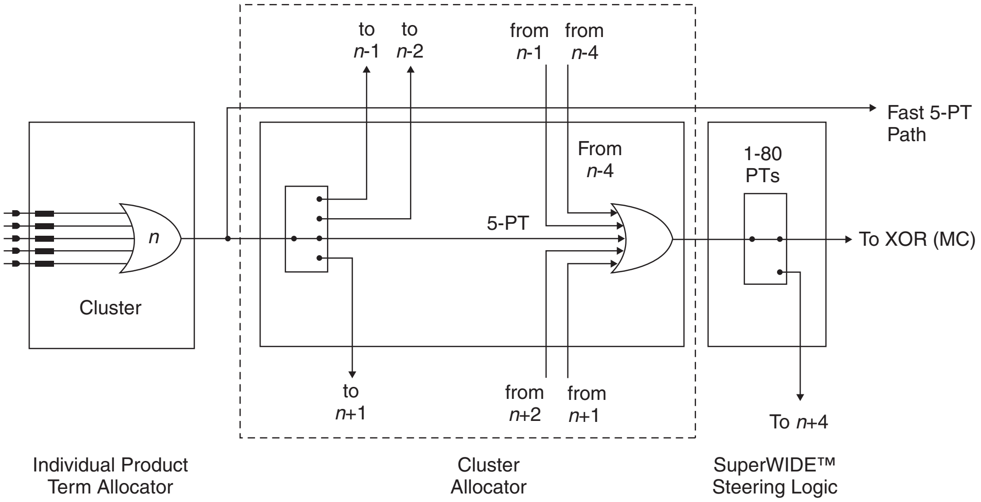


Table 5. Product Term Expansion Capability

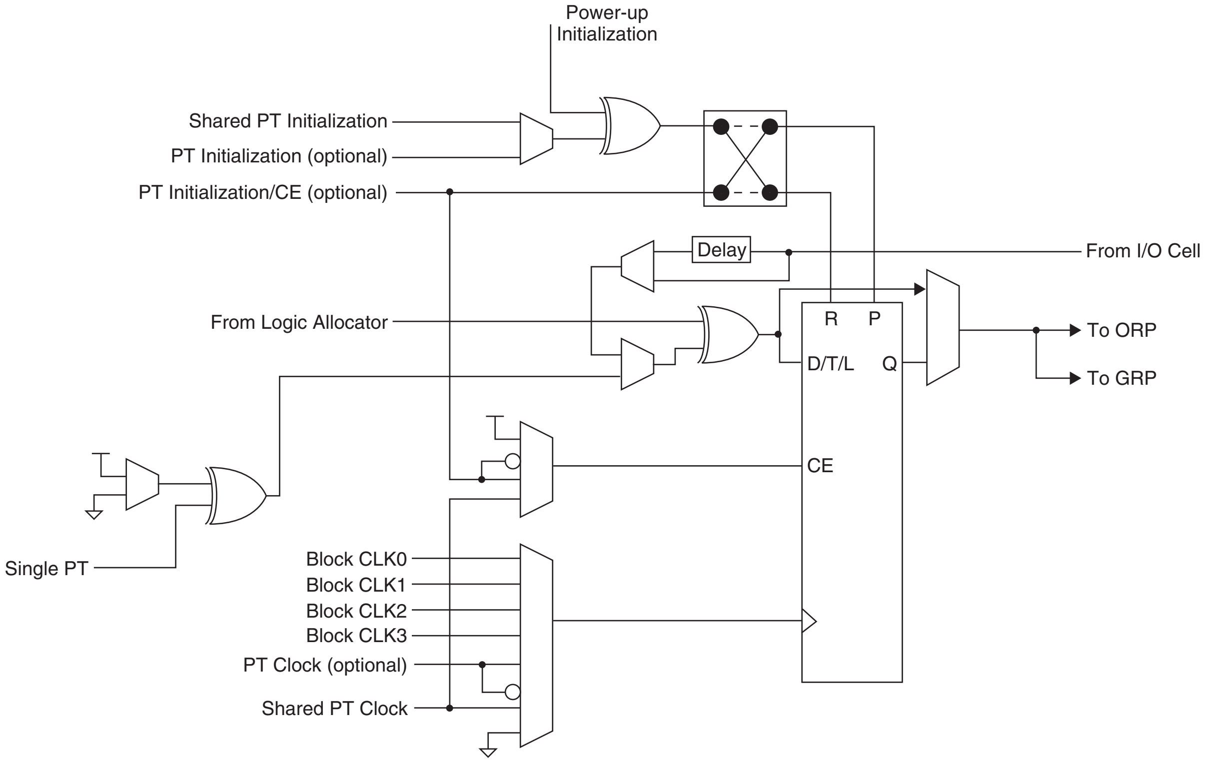
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6[1, 2]	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T_j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

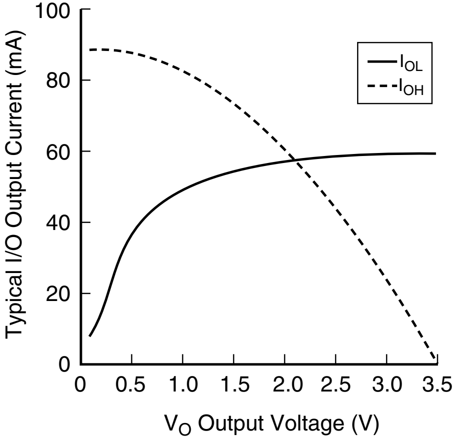
Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

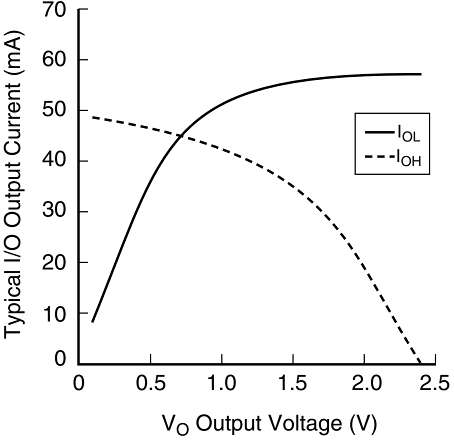
Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

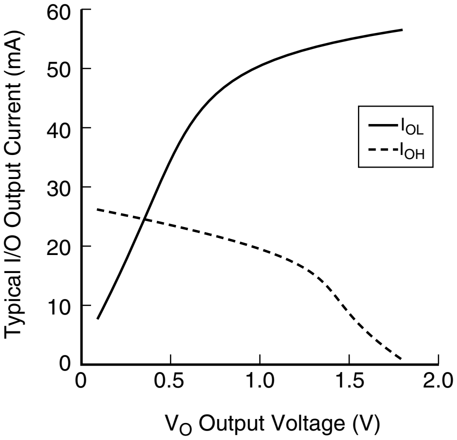
1. Insensitive to sequence of V_{CC} or $V_{CCO.}$ However, assumes monotonic rise/fall rates for V_{CC} and $V_{CCO,}$ provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.



3.3V V_{CCO}



2.5V V_{CCO}

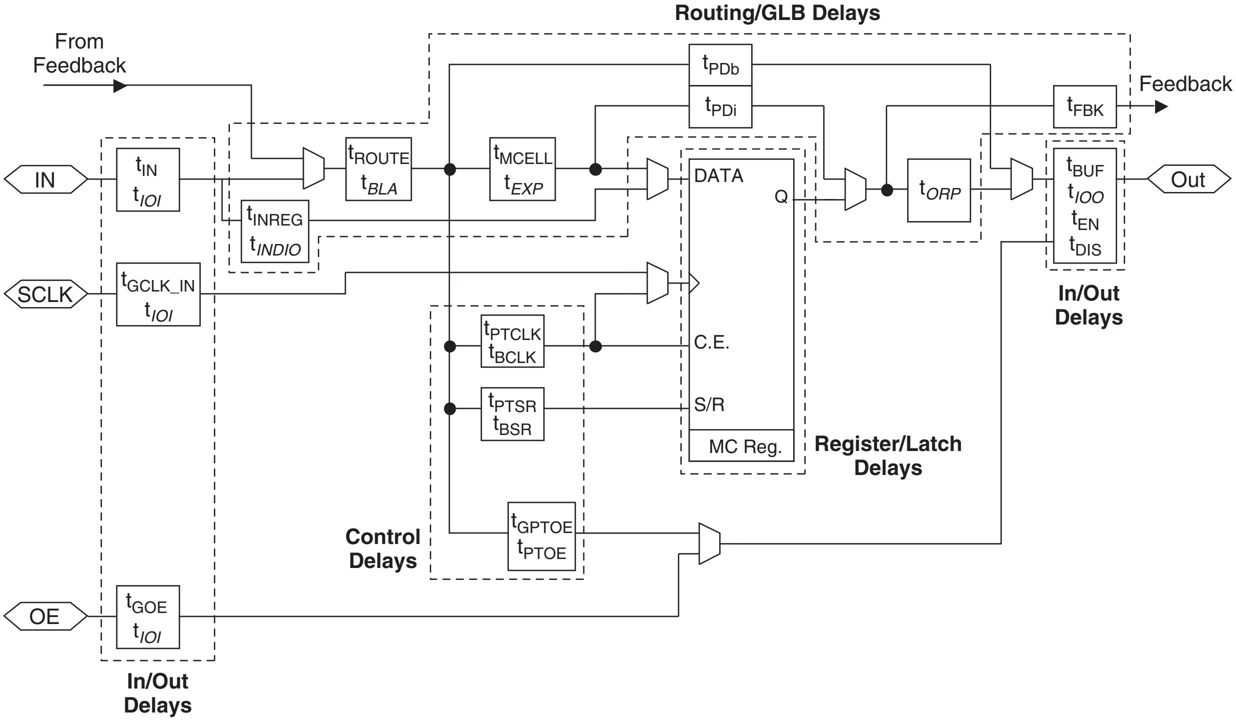


1.8V V_{CCO}

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{H}	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000V/B/C Timing Adders[1]

Adder Type	Base Parameter	Description	-25		-27		-3		-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders											
t_{INDIO}	t_{INREG}	Input register delay	—	0.95	—	1.00	—	1.00	—	1.00	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	—	0.33	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	—	0.05	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.03	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters											
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters											
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A^2	A4	A^2
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5	A8	A^5
3	0	A6	A^6	A12	A^6	A10	A^6
4	0	A7	A^7	A14	A^7	A11	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0	B15	B^7
8	0	A9	A^9	B2	B^1	B12	B^6
9	0	A10	A^10	B4	B^2	B10	B^5
10	0	A11	A^11	B6	B^3	B8	B^4
11	-	TCK	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-	VCC	-
13	-	GND	-	GND	-	GND	-
14	0	A12	A^12	B8	B^4	B6	B^3
15	0	A13	A^13	B10	B^5	B4	B^2
16	0	A14	A^14	B12	B^6	B2	B^1
17	0	A15	A^15	B14	B^7	B0	B^0
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
20	1	B0	B^0	C0	C^0	C0	C^0
21	1	B1	B^1	C2	C^1	C1	C^1
22	1	B2	B^2	C4	C^2	C2	C^2
23	1	B3	B^3	C6	C^3	C4	C^3
24	1	B4	B^4	C8	C^4	C6	C^4
25	-	TMS	-	TMS	-	TMS	-
26	1	B5	B^5	C10	C^5	C8	C^5
27	1	B6	B^6	C12	C^6	C10	C^6
28	1	B7	B^7	C14	C^7	C11	C^7
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B^8	D0	D^0	D15	D^7
32	1	B9	B^9	D2	D^1	D12	D^6

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3	P12	P^3
85	1	D2	D^2	H4	H^2	P10	P^2
86	1	D1	D^1	H2	H^1	P6	P^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	P^0
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^0
92	0	A1	A^1	A2	A^1	A6	A^1
93	0	A2	A^2	A4	A^2	A10	A^2
94	0	A3	A^3	A6	A^3	A12	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4	B2	B^0
98	0	A5	A^5	A10	A^5	B6	B^1
99	0	A6	A^6	A12	A^6	B10	B^2
100	0	A7	A^7	A14	A^7	B12	B^3

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

		ispMACH 4128V/B/C	
Pin Number	**Bank Number**	**GLB/MC/Pad**	**ORP**
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	**ORP**
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

		ispMACH 4128V		ispMACH 4256V	
Pin Number	**Bank Number**	**GLB/MC/Pad**	**ORP**	**GLB/MC/Pad**	**ORP**
43	0	D9	D^7	G4	G^2
44	0	D8	D^6	G2	G^1
45	0	NC[2]	-	I[2]	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D^5	H12	H^6
49	0	D5	D^4	H10	H^5
50	0	D4	D^3	H8	H^4
51	0	D2	D^2	H6	H^3
52	0	D1	D^1	H4	H^2
53	0	D0	D^0	H2	H^1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E^0	I2	I^1
59	1	E1	E^1	I4	I^2
60	1	E2	E^2	I6	I^3
61	1	E4	E^3	I8	I^4
62	1	E5	E^4	I10	I^5
63	1	E6	E^5	I12	I^6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E^6	J2	J^1
67	1	E9	E^7	J4	J^2
68	1	E10	E^8	J6	J^3
69	1	E12	E^9	J8	J^4
70	1	E13	E^10	J10	J^5
71	1	E14	E^11	J12	J^6
72	1	NC[2]	-	I[2]	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F^0	K12	K^6
77	1	F1	F^1	K10	K^5
78	1	F2	F^2	K8	K^4
79	1	F4	F^3	K6	K^3
80	1	F5	F^4	K4	K^2
81	1	F6	F^5	K2	K^1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F^6	L14	L^7
84	1	F9	F^7	L12	L^6
85	1	F10	F^8	L10	L^5

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC[2]	-	I[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L^1
T5	0	NC	-	NC	-	I2	I^1	L8	L^2
R6	0	NC	-	NC	-	I0	I^0	L12	L^3
T6	0	NC	-	H14	H^9	G12	G^6	M8	M^2
N7	0	NC	-	H12	H^8	G14	G^7	M12	M^3
P7	0	H14	H^7	H10	H^7	L14	L^7	P14	P^7
R7	0	H12	H^6	H9	H^6	L12	L^6	P12	P^6
L8	0	H10	H^5	H8	H^5	L10	L^5	P10	P^5
T7	0	H8	H^4	H6	H^4	L8	L^4	P8	P^4
M8	0	H6	H^3	H4	H^3	L6	L^3	P6	P^3
N8	0	H4	H^2	H2	H^2	L4	L^2	P4	P^2
R8	0	H2	H^1	H1	H^1	L2	L^1	P2	P^1
P8	0	H0	H^0	H0	H^0	L0	L^0	P0	P^0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I^0	I0	I^0	M0	M^0	AX0	AX^0
R9	1	I2	I^1	I1	I^1	M2	M^1	AX2	AX^1
T9	1	I4	I^2	I2	I^2	M4	M^2	AX4	AX^2
T10	1	I6	I^3	I4	I^3	M6	M^3	AX6	AX^3
R10	1	I8	I^4	I6	I^4	M8	M^4	AX8	AX^4
M9	1	I10	I^5	I8	I^5	M10	M^5	AX10	AX^5
P10	1	I12	I^6	I9	I^6	M12	M^6	AX12	AX^6
L9	1	I14	I^7	I10	I^7	M14	M^7	AX14	AX^7
N10	1	NC	-	I12	I^8	BX14	BX^7	DX0	DX^0
T11	1	NC	-	I14	I^9	BX12	BX^6	DX4	DX^1
R11	1	NC	-	NC	-	P0	P^0	EX0	EX^0
T12	1	NC	-	NC	-	P2	P^1	EX4	EX^1
N12	1	NC	-	NC	-	NC	-	EX8	EX^2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX^3
T13	1	NC	-	J0	J^0	BX10	BX^5	DX8	DX^2
P12	1	NC	-	J1	J^1	BX8	BX^4	DX12	DX^3
M10	1	J0	J^0	J2	J^2	N0	N^0	BX0	BX^0
R13	1	J2	J^1	J4	J^3	N2	N^1	BX2	BX^1
L10	1	J4	J^2	J6	J^4	N4	N^2	BX4	BX^2
T14	1	J6	J^3	J8	J^5	N6	N^3	BX6	BX^3
M11	1	J8	J^4	J9	J^6	N8	N^4	BX8	BX^4

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
C12	1	O0	O^0	O2	O^2	GX0	GX^0	OX0	OX^0
E10	1	NC	-	O1	O^1	CX8	CX^4	MX0	MX^0
A13	1	NC	-	O0	O^0	CX10	CX^5	MX4	MX^1
D12	1	NC	-	NC	-	NC	-	LX0	LX^0
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B12	1	NC	-	NC	-	NC	-	LX4	LX^1
A12	1	NC	-	NC	-	EX2	EX^1	LX8	LX^2
B11	1	NC	-	NC	-	EX0	EX^0	LX12	LX^3
A11	1	NC	-	P14	P^9	CX12	CX^6	MX8	MX^2
D10	1	NC	-	P12	P^8	CX14	CX^7	MX12	MX^3
C10	1	P14	P^7	P10	P^7	HX14	HX^7	PX14	PX^7
B10	1	P12	P^6	P9	P6	HX12	HX^6	PX12	PX^6
A10	1	P10	P^5	P8	P^5	HX10	HX^5	PX10	PX^5
A9	1	P8	P^4	P6	P^4	HX8	HX^4	PX8	PX^4
F9	1	P6	P^3	P4	P^3	HX6	HX^3	PX6	PX^3
B9	1	P4	P^2	P2	P^2	HX4	HX^2	PX4	PX^2
E9	1	P2/GOE1	P^1	P1/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE1	PX^1
C9	1	P0	P^0	P0	P^0	HX0	HX^0	PX0	PX^0
-	-	GND	-	GND		GND	-	GND	-
D9	1	CLK3/I	-	CLK3/I	-	CLK3/I	-	CLK3/I	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
B8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-	CLK0/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
D8	0	A0	A^0	A0	A^0	A0	A^0	A0	A^0
C8	0	A2/GOE0	A^1	A1/GOE0	A^1	A2/GOE0	A^1	A2/GOE0	A^1
A8	0	A4	A^2	A2	A^2	A4	A^2	A4	A^2
A7	0	A6	A^3	A4	A^3	A6	A^3	A6	A^3
B7	0	A8	A^4	A6	A^4	A8	A^4	A8	A^4
E8	0	A10	A^5	A8	A^5	A10	A^5	A10	A^5
D7	0	A12	A^6	A9	A^6	A12	A^6	A12	A^6
F8	0	A14	A^7	A10	A^7	A14	A^7	A14	A^7
C7	0	NC	-	A12	A^8	F14	F^7	D0	D^0
A6	0	NC	-	A14	A^9	F12	F^6	D4	D^1
B6	0	NC	-	NC	-	D14	D^7	E0	E^0
A5	0	NC	-	NC	-	D12	D^6	E4	E^1
B5	0	NC	-	NC	-	NC	-	E8	E^2
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
D5	0	NC	-	NC	-	NC	-	E12	E^3
A4	0	NC	-	B0	B^0	F10	F^5	D8	D^2

ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I[1]	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I[1]	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I[1]	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I[1]	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I[1]	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I[1]	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC[1]	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC[1]	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC[1]	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC[1]	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC[1]	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC[1]	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C[1]	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C[1]	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C[1]	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C[1]	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C[1]	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C[1]	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-5FT256I	384	2.5	5	ftBGA	256	192	I
	LC4384B-75FT256I	384	2.5	7.5	ftBGA	256	192	I
	LC4384B-10FT256I	384	2.5	10	ftBGA	256	192	I
	LC4384B-5F256I[1]	384	2.5	5	fpBGA	256	192	I
	LC4384B-75F256I[1]	384	2.5	7.5	fpBGA	256	192	I
	LC4384B-10F256I[1]	384	2.5	10	fpBGA	256	192	I
	LC4384B-5T176I	384	2.5	5	TQFP	176	128	I
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128	I
	LC4384B-10T176I	384	2.5	10	TQFP	176	128	I
LC4512B	LC4512B-5FT256I	512	2.5	5	ftBGA	256	208	I
	LC4512B-75FT256I	512	2.5	7.5	ftBGA	256	208	I
	LC4512B-10FT256I	512	2.5	10	ftBGA	256	208	I
	LC4512B-5F256I[1]	512	2.5	5	fpBGA	256	208	I
	LC4512B-75F256I[1]	512	2.5	7.5	fpBGA	256	208	I
	LC4512B-10F256I[1]	512	2.5	10	fpBGA	256	208	I
	LC4512B-5T176I	512	2.5	5	TQFP	176	128	I
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
	LC4512B-10T176I	512	2.5	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32	C
	LC4032V-5T48C	32	3.3	5	TQFP	48	32	C
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32	C
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30	C
	LC4032V-5T44C	32	3.3	5	TQFP	44	30	C
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30	C
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64	C
	LC4064V-5T100C	64	3.3	5	TQFP	100	64	C
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64	C
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32	C
	LC4064V-5T48C	64	3.3	5	TQFP	48	32	C
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32	C
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30	C
	LC4064V-5T44C	64	3.3	5	TQFP	44	30	C
	LC4064V-75T44C	64	3.3	7.5	TQFP	44	30	C

ispMACH 4000V (3.3V) Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75T48E	32	3.3	7.5	TQFP	48	32	E
	LC4032V-75T44E	32	3.3	7.5	TQFP	44	30	E
LC4064V	LC4064V-75T100E	64	3.3	7.5	TQFP	100	64	E
	LC4064V-75T48E	64	3.3	7.5	TQFP	48	32	E
	LC4064V-75T44E	64	3.3	7.5	TQFP	44	30	E
LC4128V	LC4128V-75T144E	128	3.3	7.5	TQFP	144	96	E
	LC4128V-75T128E	128	3.3	7.5	TQFP	128	92	E
	LC4128V-75T100E	128	3.3	7.5	TQFP	100	64	E
LC4256V	LC4256V-75T176E	256	3.3	7.5	TQFP	176	128	E
	LC4256V-75T144E	256	3.3	7.5	TQFP	144	96	E
	LC4256V-75T100E	256	3.3	7.5	TQFP	100	64	E

ispMACH 4000B (2.5V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128B	LC4128B-5TN128I	128	2.5	5	Lead-Free TQFP	128	92	I
	LC4128B-75TN128I	128	2.5	7.5	Lead-Free TQFP	128	92	I
	LC4128B-10TN128I	128	2.5	10	Lead-Free TQFP	128	92	I
	LC4128B-5TN100I	128	2.5	5	Lead-Free TQFP	100	64	I
	LC4128B-75TN100I	128	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4128B-10TN100I	128	2.5	10	Lead-Free TQFP	100	64	I
LC4256B	LC4256B-5FTN256AI	256	2.5	5	Lead-Free ftBGA	256	128	I
	LC4256B-75FTN256AI	256	2.5	7.5	Lead-Free ftBGA	256	128	I
	LC4256B-10FTN256AI	256	2.5	10	Lead-Free ftBGA	256	128	I
	LC4256B-5FTN256BI	256	2.5	5	Lead-Free ftBGA	256	160	I
	LC4256B-75FTN256BI	256	2.5	7.5	Lead-Free ftBGA	256	160	I
	LC4256B-10FTN256BI	256	2.5	10	Lead-Free ftBGA	256	160	I
	LC4256B-5FN256AI[1]	256	2.5	5	Lead-Free fpBGA	256	128	I
	LC4256B-75FN256AI[1]	256	2.5	7.5	Lead-Free fpBGA	256	128	I
	LC4256B-10FN256AI[1]	256	2.5	10	Lead-Free fpBGA	256	128	I
	LC4256B-5FN256BI[1]	256	2.5	5	Lead-Free fpBGA	256	160	I
	LC4256B-75FN256BI[1]	256	2.5	7.5	Lead-Free fpBGA	256	160	I
	LC4256B-10FN256BI[1]	256	2.5	10	Lead-Free fpBGA	256	160	I
	LC4256B-5TN176I	256	2.5	5	Lead-Free TQFP	176	128	I
	LC4256B-75TN176I	256	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4256B-10TN176I	256	2.5	10	Lead-Free TQFP	176	128	I
	LC4256B-5TN100I	256	2.5	5	Lead-Free TQFP	100	64	I
	LC4256B-75TN100I	256	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4256B-10TN100I	256	2.5	10	Lead-Free TQFP	100	64	I
LC4384B	LC4384B-5FTN256I	384	2.5	5	Lead-Free ftBGA	256	192	I
	LC4384B-75FTN256I	384	2.5	7.5	Lead-Free ftBGA	256	192	I
	LC4384B-10FTN256I	384	2.5	10	Lead-Free ftBGA	256	192	I
	LC4384B-5FN256I[1]	384	2.5	5	Lead-Free fpBGA	256	192	I
	LC4384B-75FN256I[1]	384	2.5	7.5	Lead-Free fpBGA	256	192	I
	LC4384B-10FN256I[1]	384	2.5	10	Lead-Free fpBGA	256	192	I
	LC4384B-5TN176I	384	2.5	5	Lead-Free TQFP	176	128	I
	LC4384B-75TN176I	384	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4384B-10TN176I	384	2.5	10	Lead-Free TQFP	176	128	I
LC4512B	LC4512B-5FTN256I	512	2.5	5	Lead-Free ftBGA	256	208	I
	LC4512B-75FTN256I	512	2.5	7.5	Lead-Free ftBGA	256	208	I
	LC4512B-10FTN256I	512	2.5	10	Lead-Free ftBGA	256	208	I
	LC4512B-5FN256I[1]	512	2.5	5	Lead-Free fpBGA	256	208	I
	LC4512B-75FN256I[1]	512	2.5	7.5	Lead-Free fpBGA	256	208	I
	LC4512B-10FN256I[1]	512	2.5	10	Lead-Free fpBGA	256	208	I
	LC4512B-5TN176I	512	2.5	5	Lead-Free TQFP	176	128	I
	LC4512B-75TN176I	512	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4512B-10TN176I	512	2.5	10	Lead-Free TQFP	176	128	I

[1] Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.