Lattice Semiconductor Corporation - LC4384C-35FT256C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	3.5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	192
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384c-35ft256c

Table 5. Product Term Expansion Capability

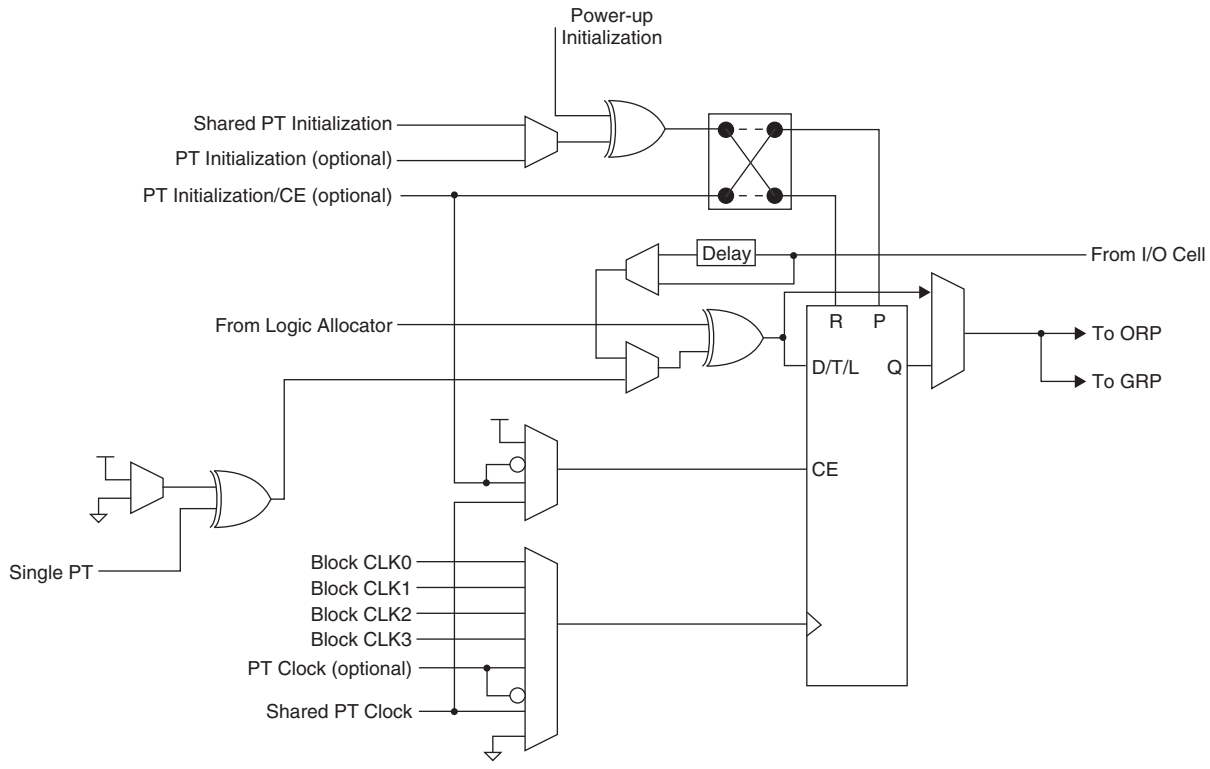
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

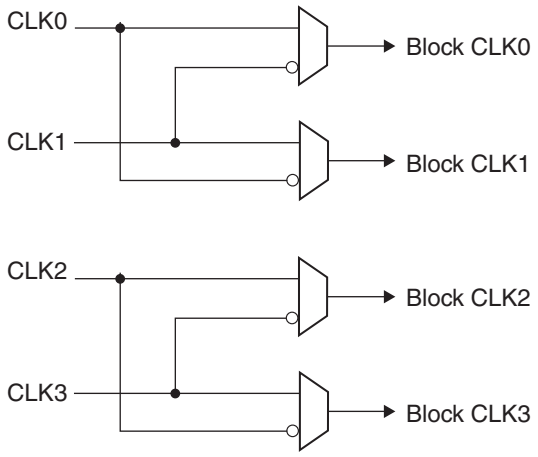
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



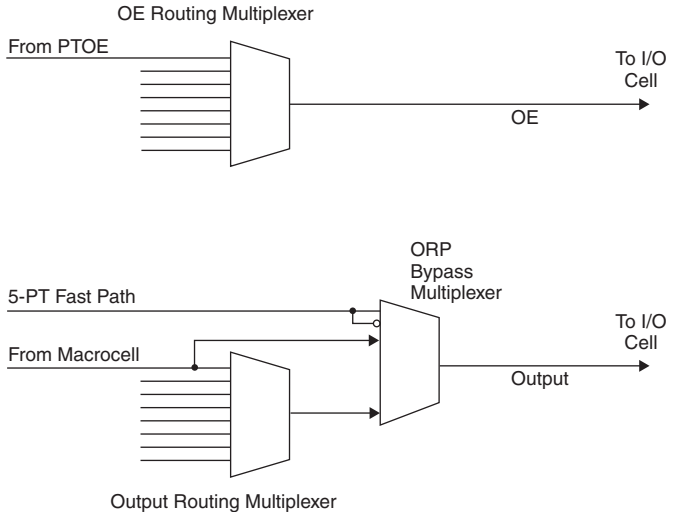
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}[4]	Standby Power Supply Current	Vcc = 3.3V	—	13	—	mA
		Vcc = 2.5V	—	13	—	mA
		Vcc = 1.8V	—	3	—	mA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. T_A = 25°C

Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22	—	µA
ispMACH 4064ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37	—	µA
ispMACH 4128ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t_S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t_{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t_R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t_{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t_{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$	—	250	—	222	—	212	—	212	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

ispMACH 4000V/B/C External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t_R	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t_{CW}	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t_{WIR}	Input register clock width, high or low	2.2	—	2.8	—	4.0		ns
f_{MAX}[4]	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
t_S	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
t_R	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
t_{RW}	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
t_{CW}	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
t_{WIR}	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
f_{MAX} (Ext.)	clock frequency with external feedback, $[1 / (t_S + t_{CO})]$	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{GPTOE}	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t_{PTOE}	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4000V/B/C Timing Adders[1] (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.00	—	1.00	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C^1	E2	E^1	I6	I^1
43	1	C2	C^2	E4	E^2	I10	I^2
44	1	C3	C^3	E6	E^3	I12	I^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4	J2	J^0
48	1	C5	C^5	E10	E^5	J6	J^1
49	1	C6	C^6	E12	E^6	J10	J^2
50	1	C7	C^7	E14	E^7	J12	J^3
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0	K12	K^3
54	1	C9	C^9	F2	F^1	K10	K^2
55	1	C10	C^10	F4	F^2	K6	K^1
56	1	C11	C^11	F6	F^3	K2	K^0
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4	L12	L^3
59	1	C13	C^13	F10	F^5	L10	L^2
60	1	C14	C^14	F12	F^6	L6	L^1
61	1	C15	C^15	F13	F^7	L4	L^0
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7	M4	M^0
65	1	D14	D^14	G12	G^6	M6	M^1
66	1	D13	D^13	G10	G^5	M10	M^2
67	1	D12	D^12	G8	G^4	M12	M^3
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3	N2	N^0
70	1	D10	D^10	G5	G^2	N6	N^1
71	1	D9	D^9	G4	G^1	N10	N^2
72	1	D8	D^8	G2	G^0	N12	N^3
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D^7	H13	H^7	O12	O^3
79	1	D6	D^6	H12	H^6	O10	O^2
80	1	D5	D^5	H10	H^5	O6	O^1
81	1	D4	D^4	H8	H^4	O2	O^0
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C^7	C14	C^9	C14	C^7	C14	C^7
F5	0	C12	C^6	C12	C^8	C12	C^6	C12	C^6
D3	0	C10	C^5	C10	C^7	C10	C^5	C10	C^5
C1	0	C8	C^4	C9	C^6	C8	C^4	C8	C^4
C2	0	C6	C^3	C8	C^5	C6	C^3	C6	C^3
E3	0	C4	C^2	C6	C^4	C4	C^2	C4	C^2
D2	0	C2	C^1	C4	C^3	C2	C^1	C2	C^1
F6	0	C0	C^0	C2	C^2	C0	C^0	C0	C^0
D1	0	NC	-	C1	C^1	F6	F^3	H0	H^0
E2	0	NC	-	C0	C^0	F4	F^2	H4	H^1
E4	0	NC	-	NC	-	D6	D^3	F4	F^2
G5	0	NC	-	NC	-	D4	D^2	F6	F^3
E1	0	NC	-	NC	-	NC	-	F8	F^4
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F^5
F1	0	NC	-	NC	-	D2	D^1	F12	F^6
G1	0	NC	-	NC	-	D0	D^0	F14	F^7
G6	0	NC	-	D14	D^9	F2	F^1	H8	H^2
G4	0	NC	-	D12	D^8	F0	F^0	H12	H^3
H6	0	D14	D^7	D10	D^7	E14	E^7	G14	G^7
G3	0	D12	D^6	D9	D^6	E12	E^6	G12	G^6
H5	0	D10	D^5	D8	D^5	E10	E^5	G10	G^5
G2	0	D8	D^4	D6	D^4	E8	E^4	G8	G^4
H1	0	D6	D^3	D4	D^3	E6	E^3	G6	G^3
H2	0	D4	D^2	D2	D^2	E4	E^2	G4	G^2
H3	0	D2	D^1	D1	D^1	E2	E^1	G2	G^1
H4	0	D0	D^0	D0	D^0	E0	E^0	G0	G^0
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E^0	E0	E^0	H0	H^0	J0	J^0
J3	0	E2	E^1	E1	E^1	H2	H^1	J2	J^1
J2	0	E4	E^2	E2	E^2	H4	H^2	J4	J^2
J1	0	E6	E^3	E4	E^3	H6	H^3	J6	J^3
K1	0	E8	E^4	E6	E^4	H8	H^4	J8	J^4
J5	0	E10	E^5	E8	E^5	H10	H^5	J10	J^5
K2	0	E12	E^6	E9	E^6	H12	H^6	J12	J^6

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E^7	E10	E^7	H14	H^7	J14	J^7
K3	0	NC	-	E12	E^8	G0	G^0	I0	I^0
K4	0	NC	-	E14	E^9	G2	G^1	I4	I^1
L1	0	NC	-	NC	-	I14	I^7	K0	K^0
L2	0	NC	-	NC	-	I12	I^6	K2	K^1
M1	0	NC	-	NC	-	NC	-	K4	K^2
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K^3
N1	0	NC	-	NC	-	I10	I^5	K8	K^4
M3	0	NC	-	NC	-	I8	I^4	K10	K^5
M4	0	NC	-	F0	F^0	G4	G^2	I8	I^2
N2	0	NC	-	F1	F^1	G6	G^3	I12	I^3
K5	0	F0	F^0	F2	F^2	J0	J^0	N0	N^0
P1	0	F2	F^1	F4	F^3	J2	J^1	N2	N^1
K6	0	F4	F^2	F6	F^4	J4	J^2	N4	N^2
N3	0	F6	F^3	F8	F^5	J6	J^3	N6	N^3
L5	0	F8	F^4	F9	F^6	J8	J^4	N8	N^4
P2	0	F10	F^5	F10	F^7	J10	J^5	N10	N^5
L6	0	F12	F^6	F12	F^8	J12	J^6	N12	N^6
R1	0	F14	F^7	F14	F^9	J14	J^7	N14	N^7
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G^9	I6	I^3	K12	K^6
M5	0	NC	-	G12	G^8	I4	I^2	K14	K^7
N4	0	G14	G^7	G10	G^7	K14	K^7	O14	O^7
T3	0	G12	G^6	G9	G^6	K12	K^6	O12	O^6
R3	0	G10	G^5	G8	G^5	K10	K^5	O10	O^5
M6	0	G8	G^4	G6	G^4	K8	K^4	O8	O^4
P4	0	G6	G^3	G4	G^3	K6	K^3	O6	O^3
L7	0	G4	G^2	G2	G^2	K4	K^2	O4	O^2
N5	0	G2	G^1	G1	G^1	K2	K^1	O2	O^1
M7	0	G0	G^0	G0	G^0	K0	K^0	O0	O^0
P5	0	NC	-	NC	-	G8	G^4	M0	M^0
R4	0	NC	-	NC	-	G10	G^5	M4	M^1
T4	0	NC	-	NC	-	NC	-	L0	L^0
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B^1	F8	F^4	D12	D^3
A3	0	B0	B^0	B2	B^2	B0	B^0	B0	B^0
F7	0	B2	B^1	B4	B^3	B2	B^1	B2	B^1
B4	0	B4	B^2	B6	B^4	B4	B^2	B4	B^2
C5	0	B6	B^3	B8	B^5	B6	B^3	B6	B^3
A2	0	B8	B^4	B9	B^6	B8	B^4	B8	B^4
E6	0	B10	B^5	B10	B^7	B10	B^5	B10	B^5
B3	0	B12	B^6	B12	B^8	B12	B^6	B12	B^6
C4	0	B14	B^7	B14	B^9	B14	B^7	B14	B^7
D4	0	NC	-	NC	-	D10	D^5	F0	F^0
E5	0	NC	-	NC	-	D8	D^4	F2	F^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

ispMACH 4000C (1.8V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92	C
	LC4128C-5T128C	128	1.8	5	TQFP	128	92	C
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92	C
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64	C
	LC4128C-5T100C	128	1.8	5	TQFP	100	64	C
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256C	LC4256C-3FT256AC	256	1.8	3	ftBGA	256	128	C
	LC4256C-5FT256AC	256	1.8	5	ftBGA	256	128	C
	LC4256C-75FT256AC	256	1.8	7.5	ftBGA	256	128	C
	LC4256C-3FT256BC	256	1.8	3	ftBGA	256	160	C
	LC4256C-5FT256BC	256	1.8	5	ftBGA	256	160	C
	LC4256C-75FT256BC	256	1.8	7.5	ftBGA	256	160	C
	LC4256C-3F256AC[1]	256	1.8	3	fpBGA	256	128	C
	LC4256C-5F256AC[1]	256	1.8	5	fpBGA	256	128	C
	LC4256C-75F256AC[1]	256	1.8	7.5	fpBGA	256	128	C
	LC4256C-3F256BC[1]	256	1.8	3	fpBGA	256	160	C
	LC4256C-5F256BC[1]	256	1.8	5	fpBGA	256	160	C
	LC4256C-75F256BC[1]	256	1.8	7.5	fpBGA	256	160	C
	LC4256C-3T176C	256	1.8	3	TQFP	176	128	C
	LC4256C-5T176C	256	1.8	5	TQFP	176	128	C
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256C-3T100C	256	1.8	3	TQFP	100	64	C
	LC4256C-5T100C	256	1.8	5	TQFP	100	64	C
	LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C
LC4384C	LC4384C-35FT256C	384	1.8	3.5	ftBGA	256	192	C
	LC4384C-5FT256C	384	1.8	5	ftBGA	256	192	C
	LC4384C-75FT256C	384	1.8	7.5	ftBGA	256	192	C
	LC4384C-35F256C[1]	384	1.8	3.5	fpBGA	256	192	C
	LC4384C-5F256C[1]	384	1.8	5	fpBGA	256	192	C
	LC4384C-75F256C[1]	384	1.8	7.5	fpBGA	256	192	C
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128	C
	LC4384C-5T176C	384	1.8	5	TQFP	176	128	C
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128	C
LC4512C	LC4512C-35FT256C	512	1.8	3.5	ftBGA	256	208	C
	LC4512C-5FT256C	512	1.8	5	ftBGA	256	208	C
	LC4512C-75FT256C	512	1.8	7.5	ftBGA	256	208	C
	LC4512C-35F256C[1]	512	1.8	3.5	fpBGA	256	208	C
	LC4512C-5F256C[1]	512	1.8	5	fpBGA	256	208	C
	LC4512C-75F256C[1]	512	1.8	7.5	fpBGA	256	208	C
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
	LC4512C-5T176C	512	1.8	5	TQFP	176	128	C
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC[1]	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC[1]	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC[1]	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC[1]	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC[1]	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC[1]	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C[1]	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C[1]	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C[1]	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI[1]	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI[1]	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI[1]	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI[1]	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI[1]	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI[1]	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I[1]	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I[1]	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I[1]	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I[1]	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I[1]	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I[1]	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.