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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	128
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384c-5tn176c

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator

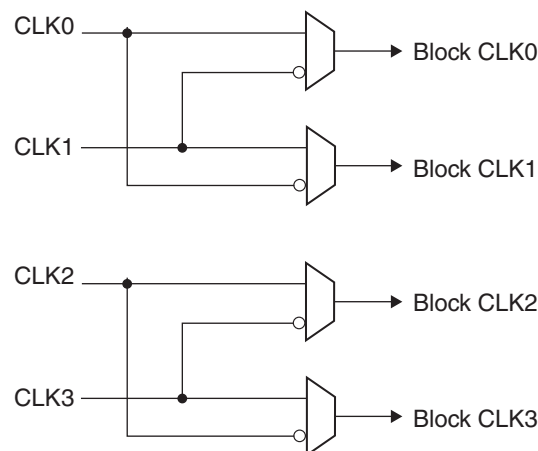


Table 10. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO} .

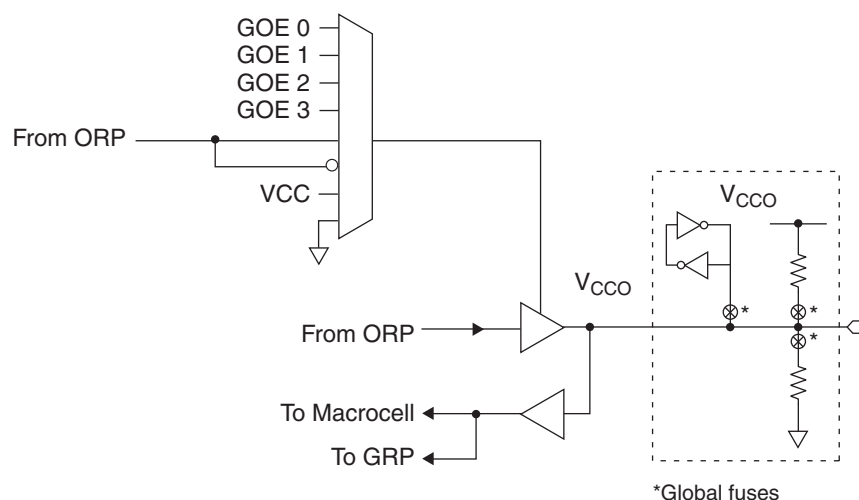
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	341	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	361	—	μA
		V _{CC} = 1.9V, T _A = 85°C	—	372	—	μA
		V _{CC} = 1.9V, T _A = 125°C	—	468	—	μA
ICC ^{4, 5}	Standby Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	13	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	32	55	μA
		V _{CC} = 1.9V, T _A = 85°C	—	43	90	μA
		V _{CC} = 1.9V, T _A = 125°C	—	135	—	μA

1. T_A = 25°C, frequency = 1.0 MHz.

2. Device configured with 16-bit counters.

3. I_{CC} varies with specific device configuration and operating frequency.

4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.

5. Includes V_{CCO} current without output loading.

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**Over Recommended Operating Conditions**

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Timing Adders ¹

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block load-ing adder	—	0.04	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

ispMACH 4000Z Timing Adders (Cont.)¹

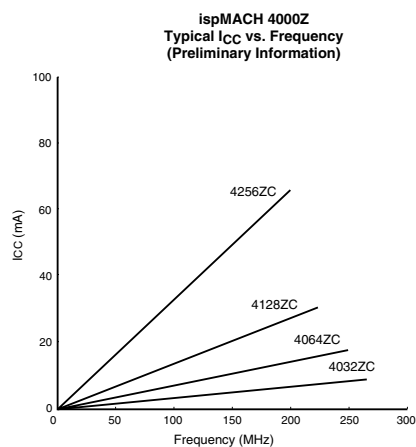
Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.30	—	1.30	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block load- ing adder	—	0.05	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

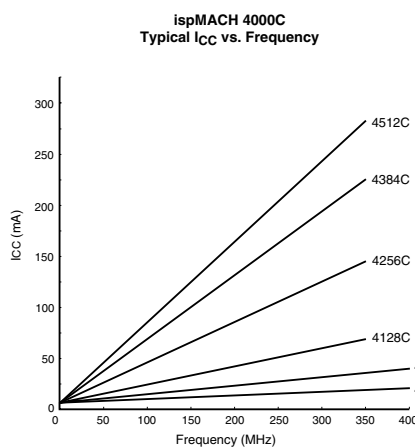
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

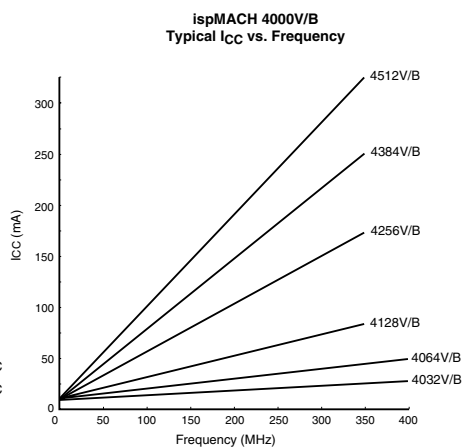
Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



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Power Estimation Coefficients¹

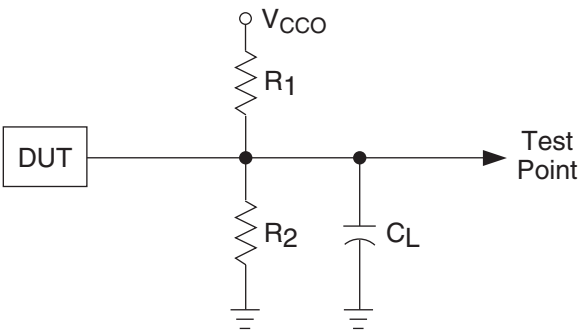
Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTTL and LVCMOS Standards



0213A/ispm4k

Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L^1	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106 Ω	106 Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $V_{CCO}/2$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $V_{CCO}/2$	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106 Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106 Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106 Ω	5pF	$V_{OH} - 0.3$	3.0V
LVCMOS I/O (L -> Z)	106 Ω	∞	5pF	$V_{OL} + 0.3$	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹

Signal	44-pin TQFP ²	48-pin TQFP ²	56-ball csBGA ³	100-pin TQFP ²	128-pin TQFP ²
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	4032Z: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:
44-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A ⁵	A10	A ⁵
3	0	A6	A ⁶	A12	A ⁶
4	0	A7	A ⁷	A14	A ⁷
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A ⁸	B0	B ⁰
8	0	A9	A ⁹	B2	B ¹
9	0	A10	A ¹⁰	B4	B ²
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A ¹²	B8	B ⁴
14	0	A13	A ¹³	B10	B ⁵
15	0	A14	A ¹⁴	B12	B ⁶
16	0	A15	A ¹⁵	B14	B ⁷
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B ⁰	C0	C ⁰
19	1	B1	B ¹	C2	C ¹
20	1	B2	B ²	C4	C ²
21	1	B3	B ³	C6	C ³
22	1	B4	B ⁴	C8	C ⁴
23	-	TMS	-	TMS	-
24	1	B5	B ⁵	C10	C ⁵
25	1	B6	B ⁶	C12	C ⁶
26	1	B7	B ⁷	C14	C ⁷
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B ⁸	D0	D ⁰
30	1	B9	B ⁹	D2	D ¹
31	1	B10	B ¹⁰	D4	D ²
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B ¹²	D8	D ⁴
36	1	B13	B ¹³	D10	D ⁵
37	1	B14	B ¹⁴	D12	D ⁶
38	1	B15/GOE1	B ¹⁵	D14/GOE1	D ⁷
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰
41	0	A1	A ¹	A2	A ¹

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B [^] 10	D4	D [^] 2	D10	D [^] 5
34	1	B11	B [^] 11	D6	D [^] 3	D8	D [^] 4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B [^] 12	D8	D [^] 4	D6	D [^] 3
39	1	B13	B [^] 13	D10	D [^] 5	D4	D [^] 2
40	1	B14	B [^] 14	D12	D [^] 6	D2	D [^] 1
41	1	B15/GOE1	B [^] 15	D14/GOE1	D [^] 7	D0/GOE1	D [^] 0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0
45	0	A1	A [^] 1	A2	A [^] 1	A1	A [^] 1
46	0	A2	A [^] 2	A4	A [^] 2	A2	A [^] 2
47	0	A3	A [^] 3	A6	A [^] 3	A4	A [^] 3
48	0	A4	A [^] 4	A8	A [^] 4	A6	A [^] 4

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A [^] 5	A8	A [^] 5
C1	0	A6	A [^] 6	A10	A [^] 6
D1	0	A7	A [^] 7	A11	A [^] 7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC ¹	-	I ¹	-
E1	0	NC ¹	-	I ¹	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A [^] 8	B15	B [^] 7
G3	0	A9	A [^] 9	B12	B [^] 6
G1	0	A10	A [^] 10	B10	B [^] 5
H1	0	A11	A [^] 11	B8	B [^] 4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC ¹	-	I ¹	-
K4	0	A12	A [^] 12	B6	B [^] 3
H4	0	A13	A [^] 13	B4	B [^] 2
H5	0	A14	A [^] 14	B2	B [^] 1

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C ¹⁰
20	0	C12	C ⁹
21	0	C10	C ⁸
22	0	C9	C ⁷
23	0	C8	C ⁶
24	0	GND (Bank 0)	-
25	0	C6	C ⁵
26	0	C5	C ⁴
27	0	C4	C ³
28	0	C2	C ²
29	0	C0	C ⁰
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D ¹¹
35	0	D13	D ¹⁰
36	0	D12	D ⁹
37	0	D10	D ⁸
38	0	D9	D ⁷
39	0	D8	D ⁶
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D ⁵
43	0	D5	D ⁴
44	0	D4	D ³
45	0	D2	D ²
46	0	D1	D ¹
47	0	D0	D ⁰
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E ⁰
53	1	E1	E ¹
54	1	E2	E ²
55	1	E4	E ³
56	1	E5	E ⁴
57	1	E6	E ⁵
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E ⁶
61	1	E9	E ⁷

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
105	1	VCCO (Bank 1)	-
106	1	H6	H ⁵
107	1	H5	H ⁴
108	1	H4	H ³
109	1	H2	H ²
110	1	H1	H ¹
111	1	H0/GOE1	H ⁰
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A ⁰
117	0	A1	A ¹
118	0	A2	A ²
119	0	A4	A ³
120	0	A5	A ⁴
121	0	A6	A ⁵
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A ⁶
125	0	A9	A ⁷
126	0	A10	A ⁸
127	0	A12	A ⁹
128	0	A14	A ¹¹

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	GND	-	GND	-	GND	-
B2	-	TDI	-	TDI	-	TDI	-
C1	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
C3	0	NC	-	B0	B ⁰	C12	C ⁶
C2	0	A8	A ⁸	B1	B ¹	C10	C ⁵
D1	0	A9	A ⁹	B2	B ²	C8	C ⁴
D3	0	A10	A ¹⁰	B4	B ³	C6	C ³
D2	0	A11	A ¹¹	B5	B ⁴	C4	C ²
E1	0	NC	-	B6	B ⁵	C2	C ¹
E2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D [^] 7	G4	G [^] 2
44	0	D8	D [^] 6	G2	G [^] 1
45	0	NC ²	-	I ²	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D [^] 5	H12	H [^] 6
49	0	D5	D [^] 4	H10	H [^] 5
50	0	D4	D [^] 3	H8	H [^] 4
51	0	D2	D [^] 2	H6	H [^] 3
52	0	D1	D [^] 1	H4	H [^] 2
53	0	D0	D [^] 0	H2	H [^] 1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E [^] 0	I2	I [^] 1
59	1	E1	E [^] 1	I4	I [^] 2
60	1	E2	E [^] 2	I6	I [^] 3
61	1	E4	E [^] 3	I8	I [^] 4
62	1	E5	E [^] 4	I10	I [^] 5
63	1	E6	E [^] 5	I12	I [^] 6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E [^] 6	J2	J [^] 1
67	1	E9	E [^] 7	J4	J [^] 2
68	1	E10	E [^] 8	J6	J [^] 3
69	1	E12	E [^] 9	J8	J [^] 4
70	1	E13	E [^] 10	J10	J [^] 5
71	1	E14	E [^] 11	J12	J [^] 6
72	1	NC ²	-	I ²	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F [^] 0	K12	K [^] 6
77	1	F1	F [^] 1	K10	K [^] 5
78	1	F2	F [^] 2	K8	K [^] 4
79	1	F4	F [^] 3	K6	K [^] 3
80	1	F5	F [^] 4	K4	K [^] 2
81	1	F6	F [^] 5	K2	K [^] 1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F [^] 6	L14	L [^] 7
84	1	F9	F [^] 7	L12	L [^] 6
85	1	F10	F [^] 8	L10	L [^] 5

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
101	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
102	1	L14	L ¹⁴	AX14	AX ¹⁴	GX14	GX ¹⁴
103	1	L12	L ¹²	AX12	AX ¹²	GX12	GX ¹²
104	1	L10	L ¹⁰	AX10	AX ¹⁰	GX10	GX ¹⁰
105	1	L8	L ⁸	AX8	AX ⁸	GX8	GX ⁸
106	1	L6	L ⁶	AX6	AX ⁶	GX6	GX ⁶
107	1	L4	L ⁴	AX4	AX ⁴	GX4	GX ⁴
108	1	L2	L ²	AX2	AX ²	GX2	GX ²
109	1	L0	L ⁰	AX0	AX ⁰	GX0	GX ⁰
110	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
111	1	M0	M ⁰	DX0	DX ⁰	JX0	JX ⁰
112	1	M2	M ²	DX2	DX ²	JX2	JX ²
113	1	M4	M ⁴	DX4	DX ⁴	JX4	JX ⁴
114	1	M6	M ⁶	DX6	DX ⁶	JX6	JX ⁶
115	1	M8	M ⁸	DX8	DX ⁸	JX8	JX ⁸
116	1	M10	M ¹⁰	DX10	DX ¹⁰	JX10	JX ¹⁰
117	1	M12	M ¹²	DX12	DX ¹²	JX12	JX ¹²
118	1	M14	M ¹⁴	DX14	DX ¹⁴	JX14	JX ¹⁴
119	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
120	1	N0	N ⁰	FX0	FX ⁰	NX0	NX ⁰
121	1	N2	N ²	FX2	FX ²	NX2	NX ²
122	1	N4	N ⁴	FX4	FX ⁴	NX4	NX ⁴
123	1	N6	N ⁶	FX6	FX ⁶	NX6	NX ⁶
124	1	N8	N ⁸	FX8	FX ⁸	NX8	NX ⁸
125	1	N10	N ¹⁰	FX10	FX ¹⁰	NX10	NX ¹⁰
126	1	N12	N ¹²	FX12	FX ¹²	NX12	NX ¹²
127	1	N14	N ¹⁴	FX14	FX ¹⁴	NX14	NX ¹⁴
128	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
129	-	TDO	-	TDO	-	TDO	-
130	-	VCC	-	VCC	-	VCC	-
131	-	NC	-	NC	-	NC	-
132	-	NC	-	NC	-	NC	-
133	-	NC	-	NC	-	NC	-
134	-	GND	-	GND	-	GND	-
135	1	O14	O ¹⁴	GX14	GX ¹⁴	OX14	OX ¹⁴
136	1	O12	O ¹²	GX12	GX ¹²	OX12	OX ¹²
137	1	O10	O ¹⁰	GX10	GX ¹⁰	OX10	OX ¹⁰
138	1	O8	O ⁸	GX8	GX ⁸	OX8	OX ⁸
139	1	O6	O ⁶	GX6	GX ⁶	OX6	OX ⁶
140	1	O4	O ⁴	GX4	GX ⁴	OX4	OX ⁴
141	1	O2	O ²	GX2	GX ²	OX2	OX ²

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B ¹	F8	F ⁴	D12	D ³
A3	0	B0	B ⁰	B2	B ²	B0	B ⁰	B0	B ⁰
F7	0	B2	B ¹	B4	B ³	B2	B ¹	B2	B ¹
B4	0	B4	B ²	B6	B ⁴	B4	B ²	B4	B ²
C5	0	B6	B ³	B8	B ⁵	B6	B ³	B6	B ³
A2	0	B8	B ⁴	B9	B ⁶	B8	B ⁴	B8	B ⁴
E6	0	B10	B ⁵	B10	B ⁷	B10	B ⁵	B10	B ⁵
B3	0	B12	B ⁶	B12	B ⁸	B12	B ⁶	B12	B ⁶
C4	0	B14	B ⁷	B14	B ⁹	B14	B ⁷	B14	B ⁷
D4	0	NC	-	NC	-	D10	D ⁵	F0	F ⁰
E5	0	NC	-	NC	-	D8	D ⁴	F2	F ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC ¹	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC ¹	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC ¹	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC ¹	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC ¹	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC ¹	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C ¹	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C ¹	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C ¹	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C ¹	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C ¹	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C ¹	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-5FT256I	384	2.5	5	ftBGA	256	192	I
	LC4384B-75FT256I	384	2.5	7.5	ftBGA	256	192	I
	LC4384B-10FT256I	384	2.5	10	ftBGA	256	192	I
	LC4384B-5F256I ¹	384	2.5	5	fpBGA	256	192	I
	LC4384B-75F256I ¹	384	2.5	7.5	fpBGA	256	192	I
	LC4384B-10F256I ¹	384	2.5	10	fpBGA	256	192	I
	LC4384B-5T176I	384	2.5	5	TQFP	176	128	I
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128	I
	LC4384B-10T176I	384	2.5	10	TQFP	176	128	I
LC4512B	LC4512B-5FT256I	512	2.5	5	ftBGA	256	208	I
	LC4512B-75FT256I	512	2.5	7.5	ftBGA	256	208	I
	LC4512B-10FT256I	512	2.5	10	ftBGA	256	208	I
	LC4512B-5F256I ¹	512	2.5	5	fpBGA	256	208	I
	LC4512B-75F256I ¹	512	2.5	7.5	fpBGA	256	208	I
	LC4512B-10F256I ¹	512	2.5	10	fpBGA	256	208	I
	LC4512B-5T176I	512	2.5	5	TQFP	176	128	I
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
	LC4512B-10T176I	512	2.5	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32	C
	LC4032V-5T48C	32	3.3	5	TQFP	48	32	C
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32	C
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30	C
	LC4032V-5T44C	32	3.3	5	TQFP	44	30	C
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30	C
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64	C
	LC4064V-5T100C	64	3.3	5	TQFP	100	64	C
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64	C
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32	C
	LC4064V-5T48C	64	3.3	5	TQFP	48	32	C
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32	C
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30	C
	LC4064V-5T44C	64	3.3	5	TQFP	44	30	C
	LC4064V-75T44C	64	3.3	7.5	TQFP	44	30	C

Lead-Free Packaging**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices**

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 μ A to -200 μ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.