Lattice Semiconductor Corporation - LC4384V-10FTN256I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	384
Number of Gates	-
Number of I/O	192
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4384v-10ftn256i

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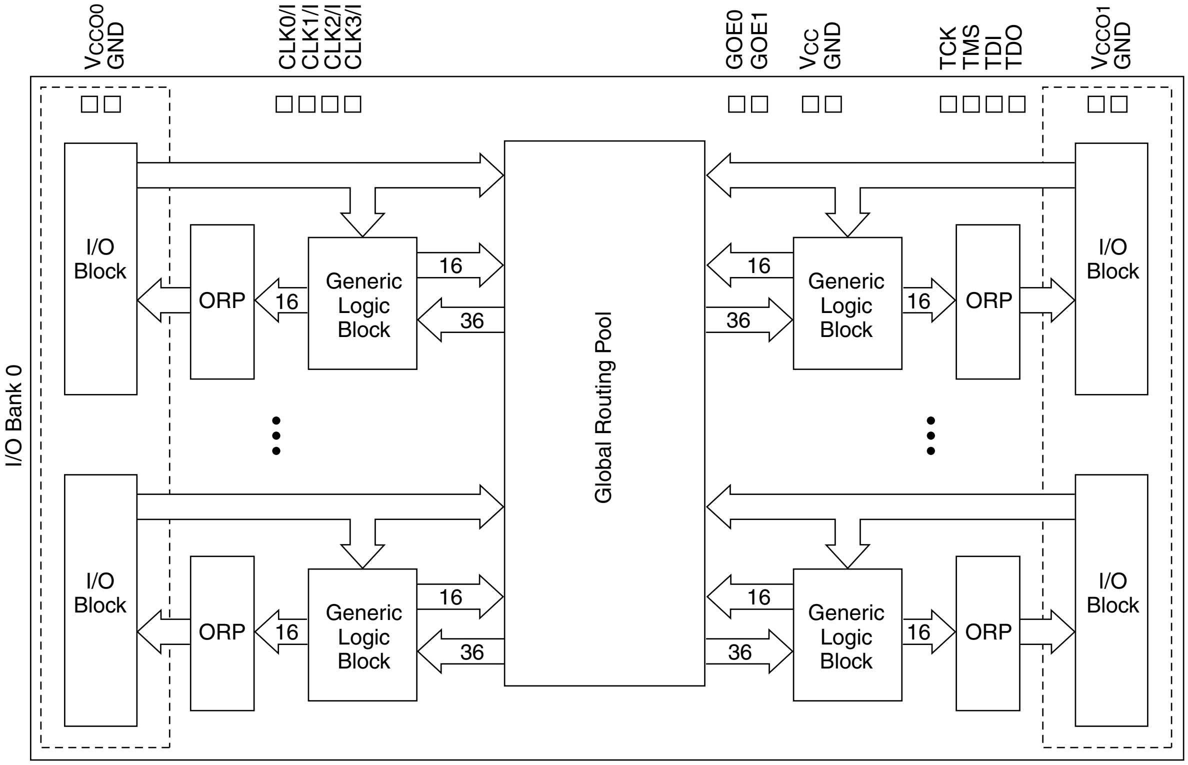
Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

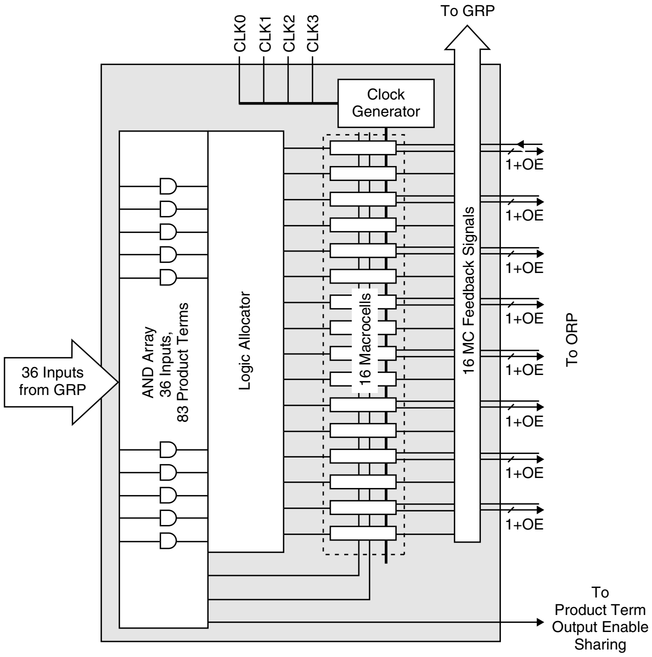
ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block



AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6[1, 2]	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T_j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or $V_{CCO.}$ However, assumes monotonic rise/fall rates for V_{CC} and $V_{CCO,}$ provided ($V_{IN} - V_{CCO}$) $\leq$ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3[2]	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.
2. ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input Leakage Current (ispMACH 4000Z)	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1]	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{IL}, I_{IH}[1]	Input Leakage Current (ispMACH 4000V/B/C)	$0 \le V_{IN} \le 3.6V$, $T_j = 105°C$	—	—	10	µA
		$0 \le V_{IN} \le 3.6V$, $T_j = 130°C$	—	—	15	µA
I_{IH}[1,2]	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	20	µA
		$3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	50	µA
I_{PU}	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-150	µA
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-200	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MIN)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. $T_A = 25°C$, f = 1.0MHz
4. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t_S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t_{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t_R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t_{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t_{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t_{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/(t_S + t_{CO})]$	—	250	—	222	—	212	—	212	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.3.2

2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t_S	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t_R	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t_{RW}	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t_{CW}	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f_{MAX} (Ext.)	clock frequency with external feedback, [1 / (t_S + t_{CO})]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{H}	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{GPTOE}	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t_{PTOE}	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A^2	A4	A^2
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5	A8	A^5
3	0	A6	A^6	A12	A^6	A10	A^6
4	0	A7	A^7	A14	A^7	A11	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0	B15	B^7
8	0	A9	A^9	B2	B^1	B12	B^6
9	0	A10	A^10	B4	B^2	B10	B^5
10	0	A11	A^11	B6	B^3	B8	B^4
11	-	TCK	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-	VCC	-
13	-	GND	-	GND	-	GND	-
14	0	A12	A^12	B8	B^4	B6	B^3
15	0	A13	A^13	B10	B^5	B4	B^2
16	0	A14	A^14	B12	B^6	B2	B^1
17	0	A15	A^15	B14	B^7	B0	B^0
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
20	1	B0	B^0	C0	C^0	C0	C^0
21	1	B1	B^1	C2	C^1	C1	C^1
22	1	B2	B^2	C4	C^2	C2	C^2
23	1	B3	B^3	C6	C^3	C4	C^3
24	1	B4	B^4	C8	C^4	C6	C^4
25	-	TMS	-	TMS	-	TMS	-
26	1	B5	B^5	C10	C^5	C8	C^5
27	1	B6	B^6	C12	C^6	C10	C^6
28	1	B7	B^7	C14	C^7	C11	C^7
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B^8	D0	D^0	D15	D^7
32	1	B9	B^9	D2	D^1	D12	D^6

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)

		ispMACH 4032Z		ispMACH 4064Z	
Ball Number	**Bank Number**	**GLB/MC/Pad**	**ORP**	**GLB/MC/Pad**	**ORP**
K5	0	A15	A^15	B0	B^0
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B^0	C0	C^0
K7	1	B1	B^1	C1	C^1
K8	1	B2	B^2	C2	C^2
K9	1	B3	B^3	C4	C^3
K10	1	B4	B^4	C6	C^4
J10	-	TMS	-	TMS	-
H8	1	B5	B^5	C8	C^5
H10	1	B6	B^6	C10	C^6
G10	1	B7	B^7	C11	C^7
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC[1]	-	I[1]	-
F10	1	NC[1]	-	I[1]	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B^8	D15	D^7
D8	1	B9	B^9	D12	D^6
D10	1	B10	B^10	D10	D^5
C10	1	B11	B^11	D8	D^4
B10	1	NC[1]	-	I[1]	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC[1]	-	I[1]	-
A7	1	B12	B^12	D6	D^3
C7	1	B13	B^13	D4	D^2
C6	1	B14	B^14	D2	D^1
A6	1	B15/GOE1	B^15	D0/GOE1	D^0
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A^0	A0/GOE0	A^0
A4	0	A1	A^1	A1	A^1
A3	0	A2	A^2	A2	A^2
A2	0	A3	A^3	A4	A^3
A1	0	A4	A^4	A6	A^4

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC[2]	-	I[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D^2	E4	E^2	G4	G^2
20	0	D2	D^1	E2	E^1	G2	G^1
21	0	D0	D^0	E0	E^0	G0	G^0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E^0	H0	H^0	J0	J^0
24	0	E2	E^1	H2	H^1	J2	J^1
25	0	E4	E^2	H4	H^2	J4	J^2
26	0	E6	E^3	H6	H^3	J6	J^3
27	0	E8	E^4	H8	H^4	J8	J^4
28	0	E10	E^5	H10	H^5	J10	J^5
29	0	E12	E^6	H12	H^6	J12	J^6
30	0	E14	E^7	H14	H^7	J14	J^7
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F^0	J0	J^0	N0	N^0
33	0	F2	F^1	J2	J^1	N2	N^1
34	0	F4	F^2	J4	J^2	N4	N^2
35	0	F6	F^3	J6	J^3	N6	N^3
36	0	F8	F^4	J8	J^4	N8	N^4
37	0	F10	F^5	J10	J^5	N10	N^5
38	0	F12	F^6	J12	J^6	N12	N^6
39	0	F14	F^7	J14	J^7	N14	N^7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G^7	K14	K^7	O14	O^7
48	0	G12	G^6	K12	K^6	O12	O^6
49	0	G10	G^5	K10	K^5	O10	O^5
50	0	G8	G^4	K8	K^4	O8	O^4
51	0	G6	G^3	K6	K^3	O6	O^3
52	0	G4	G^2	K4	K^2	O4	O^2
53	0	G2	G^1	K2	K^1	O2	O^1
54	0	G0	G^0	K0	K^0	O0	O^0
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H^7	L14	L^7	P14	P^7
58	0	H12	H^6	L12	L^6	P12	P^6
59	0	H10	H^5	L10	L^5	P10	P^5

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C^7	C14	C^9	C14	C^7	C14	C^7
F5	0	C12	C^6	C12	C^8	C12	C^6	C12	C^6
D3	0	C10	C^5	C10	C^7	C10	C^5	C10	C^5
C1	0	C8	C^4	C9	C^6	C8	C^4	C8	C^4
C2	0	C6	C^3	C8	C^5	C6	C^3	C6	C^3
E3	0	C4	C^2	C6	C^4	C4	C^2	C4	C^2
D2	0	C2	C^1	C4	C^3	C2	C^1	C2	C^1
F6	0	C0	C^0	C2	C^2	C0	C^0	C0	C^0
D1	0	NC	-	C1	C^1	F6	F^3	H0	H^0
E2	0	NC	-	C0	C^0	F4	F^2	H4	H^1
E4	0	NC	-	NC	-	D6	D^3	F4	F^2
G5	0	NC	-	NC	-	D4	D^2	F6	F^3
E1	0	NC	-	NC	-	NC	-	F8	F^4
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F^5
F1	0	NC	-	NC	-	D2	D^1	F12	F^6
G1	0	NC	-	NC	-	D0	D^0	F14	F^7
G6	0	NC	-	D14	D^9	F2	F^1	H8	H^2
G4	0	NC	-	D12	D^8	F0	F^0	H12	H^3
H6	0	D14	D^7	D10	D^7	E14	E^7	G14	G^7
G3	0	D12	D^6	D9	D^6	E12	E^6	G12	G^6
H5	0	D10	D^5	D8	D^5	E10	E^5	G10	G^5
G2	0	D8	D^4	D6	D^4	E8	E^4	G8	G^4
H1	0	D6	D^3	D4	D^3	E6	E^3	G6	G^3
H2	0	D4	D^2	D2	D^2	E4	E^2	G4	G^2
H3	0	D2	D^1	D1	D^1	E2	E^1	G2	G^1
H4	0	D0	D^0	D0	D^0	E0	E^0	G0	G^0
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E^0	E0	E^0	H0	H^0	J0	J^0
J3	0	E2	E^1	E1	E^1	H2	H^1	J2	J^1
J2	0	E4	E^2	E2	E^2	H4	H^2	J4	J^2
J1	0	E6	E^3	E4	E^3	H6	H^3	J6	J^3
K1	0	E8	E^4	E6	E^4	H8	H^4	J8	J^4
J5	0	E10	E^5	E8	E^5	H10	H^5	J10	J^5
K2	0	E12	E^6	E9	E^6	H12	H^6	J12	J^6

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC[1]	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC[1]	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC[1]	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC[1]	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC[1]	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC[1]	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C[1]	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C[1]	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C[1]	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C[1]	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C[1]	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C[1]	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC[1]	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC[1]	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC[1]	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC[1]	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC[1]	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC[1]	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C[1]	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C[1]	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C[1]	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

Lead-Free Packaging

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150µA to -200µA.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.