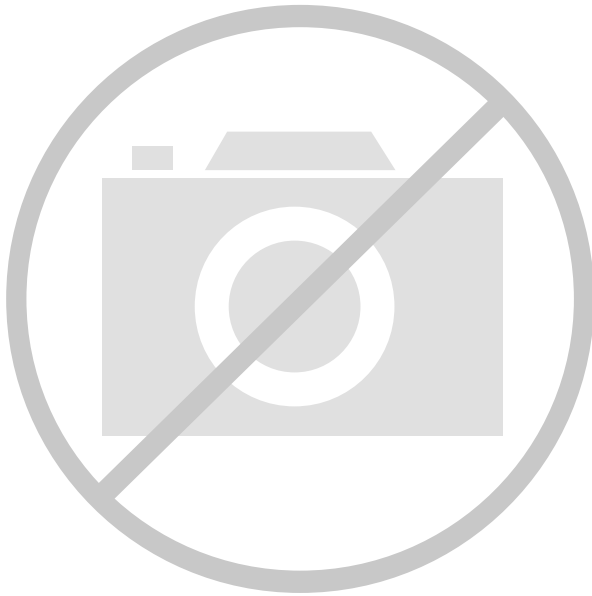




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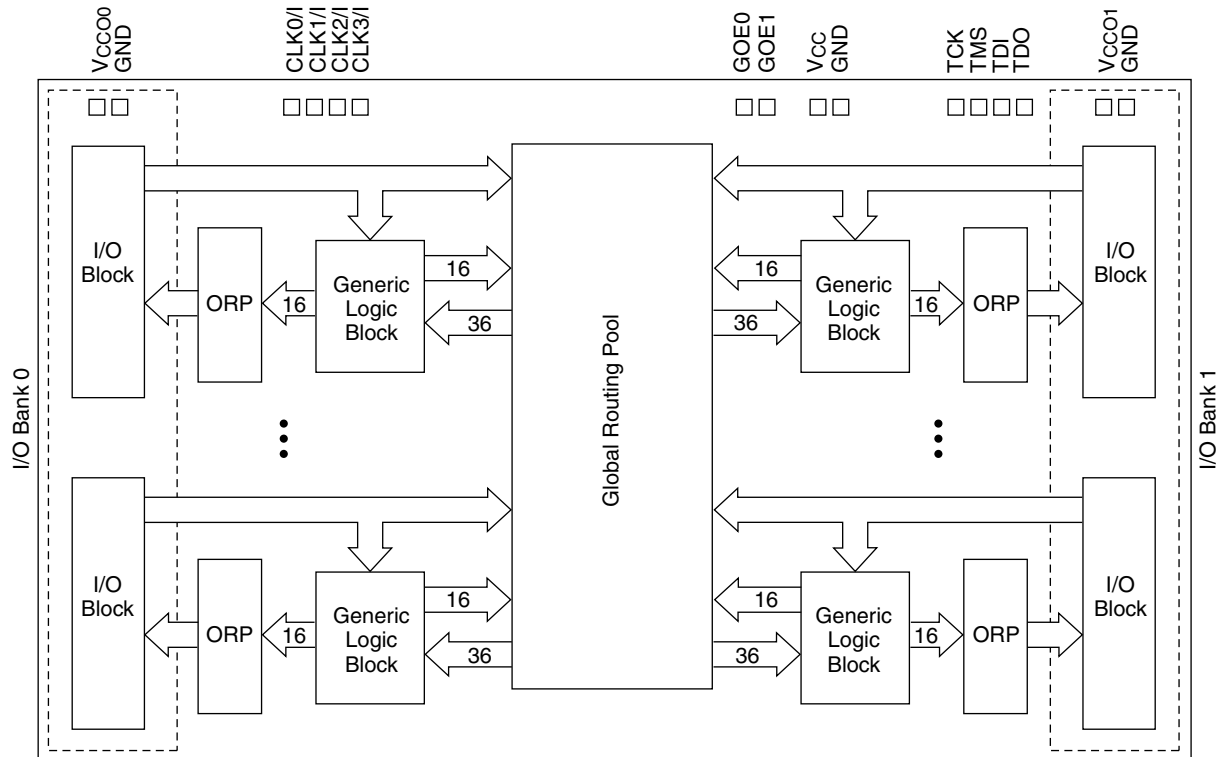
Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	-
Number of I/O	208
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4512c-75ft256c

Figure 1. Functional Block Diagram

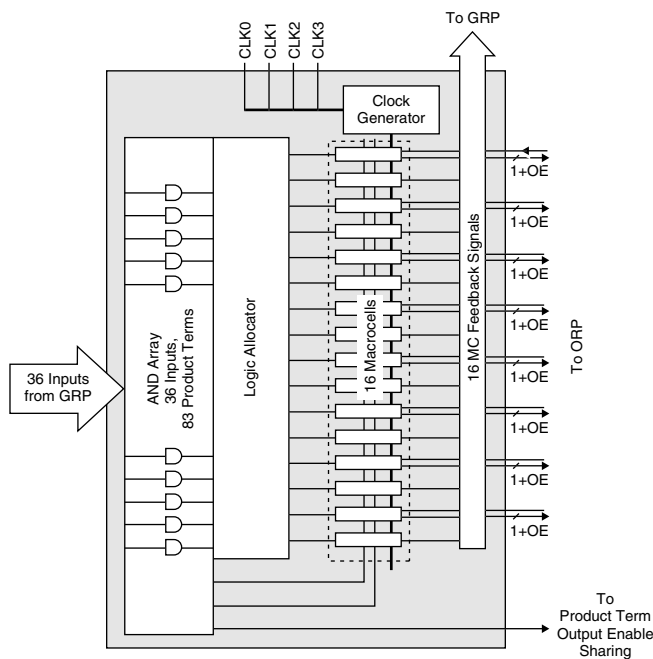
The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CC0} of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

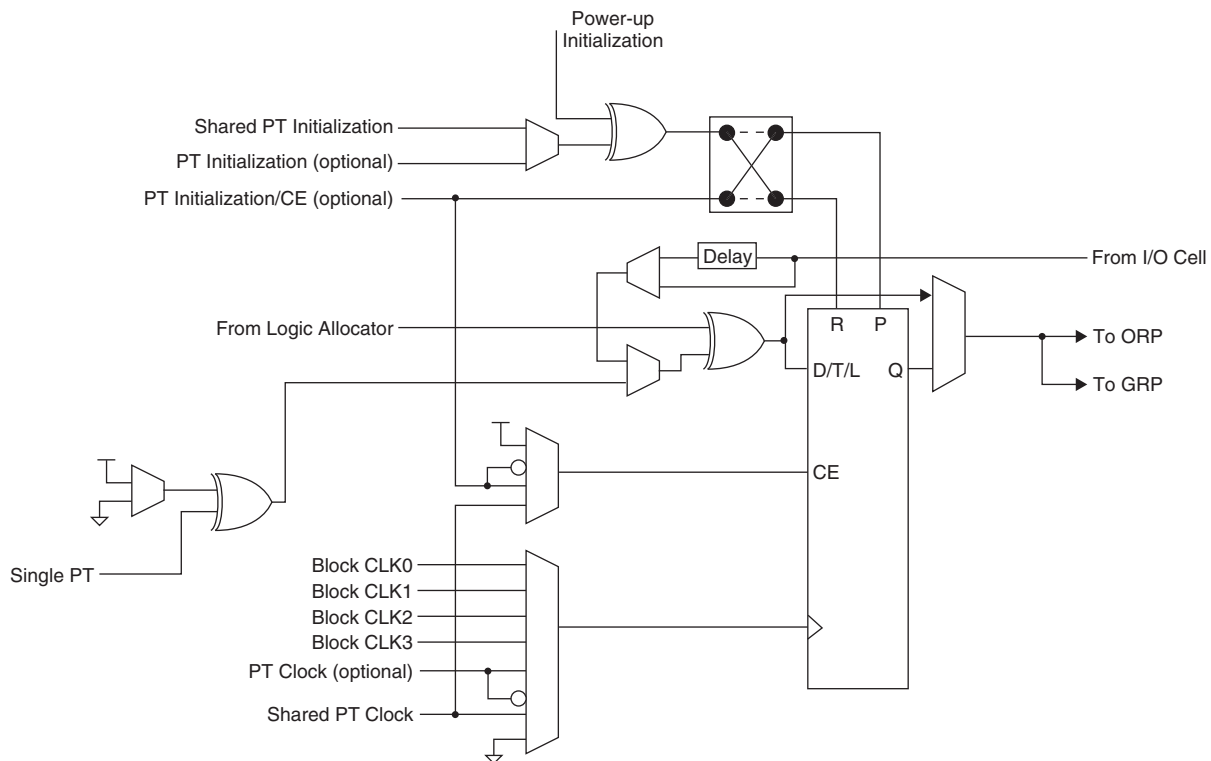
Table 5. Product Term Expansion Capability

Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP} . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell

Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

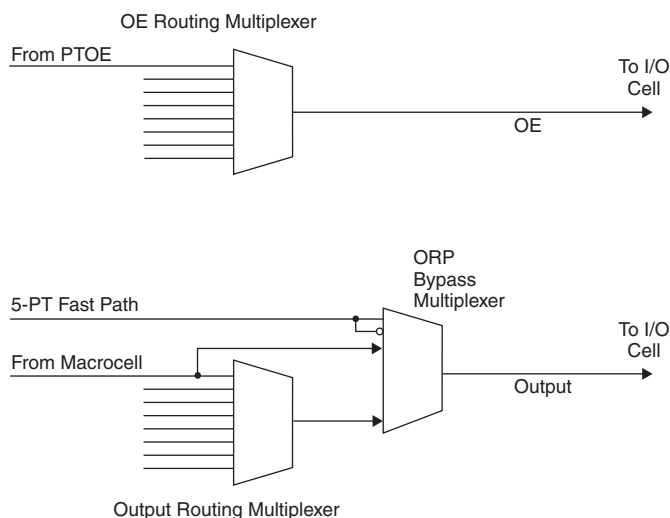
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

I/O Recommended Operating Conditions

Standard	V_{CCO} (V) ¹	
	Min.	Max.
LVTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3 ²	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

2. ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input Leakage Current (ispMACH 4000Z)	$0 \leq V_{IN} < V_{CCO}$	—	0.5	1	μA
I_{IH}^1	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \leq 5.5V$	—	—	10	μA
I_{IL}, I_{IH}^1	Input Leakage Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$	—	—	10	μA
		$0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$	—	—	15	μA
$I_{IH}^{1,2}$	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V^1$	—	—	20	μA
		$3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V^1$	—	—	50	μA
I_{PU}	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-150	μA
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-200	μA
I_{PD}	I/O Weak Pull-down Resistor Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$	30	—	150	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{BHT}$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \leq V_{IN} \leq V_{CCO}$	—	—	-150	μA
V_{BHT}	Bus Hold Trip Points	—	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
C_1	I/O Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_2	Clock Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_3	Global Input Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \leq V_{CCO} \leq 3.6V$.

3. $T_A = 25^\circ C$, $f = 1.0MHz$

4. I_{IH} excursions of up to 1.5 μA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t _S	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t _{ST}	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t _{SIR}	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t _R	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t _{RW}	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t _{CW}	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t _{WIR}	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f _{MAX} (Ext.)	clock frequency with external feedback, [1 / (t _S + t _{CO})]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

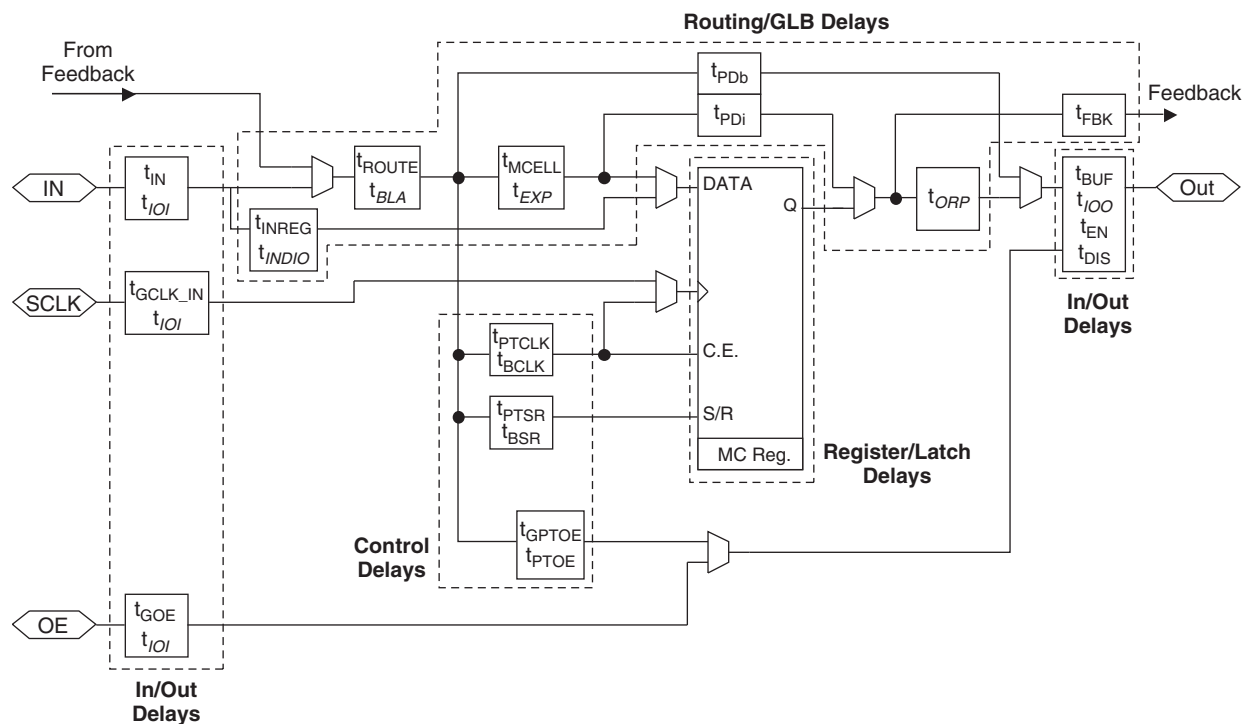
3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#).

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t _{GOE}	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t _{BUF}	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t _{EN}	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t _{DIS}	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t _{MCELL}	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t _{FBK}	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t _{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t _{ST_PT}	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t _H	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{HT}	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t _{CES}	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t _{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t _{SL}	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t _{HL}	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t _{SRI}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B [^] 10	D4	D [^] 2	D10	D [^] 5
34	1	B11	B [^] 11	D6	D [^] 3	D8	D [^] 4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B [^] 12	D8	D [^] 4	D6	D [^] 3
39	1	B13	B [^] 13	D10	D [^] 5	D4	D [^] 2
40	1	B14	B [^] 14	D12	D [^] 6	D2	D [^] 1
41	1	B15/GOE1	B [^] 15	D14/GOE1	D [^] 7	D0/GOE1	D [^] 0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0
45	0	A1	A [^] 1	A2	A [^] 1	A1	A [^] 1
46	0	A2	A [^] 2	A4	A [^] 2	A2	A [^] 2
47	0	A3	A [^] 3	A6	A [^] 3	A4	A [^] 3
48	0	A4	A [^] 4	A8	A [^] 4	A6	A [^] 4

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A [^] 5	A8	A [^] 5
C1	0	A6	A [^] 6	A10	A [^] 6
D1	0	A7	A [^] 7	A11	A [^] 7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC ¹	-	I ¹	-
E1	0	NC ¹	-	I ¹	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A [^] 8	B15	B [^] 7
G3	0	A9	A [^] 9	B12	B [^] 6
G1	0	A10	A [^] 10	B10	B [^] 5
H1	0	A11	A [^] 11	B8	B [^] 4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC ¹	-	I ¹	-
K4	0	A12	A [^] 12	B6	B [^] 3
H4	0	A13	A [^] 13	B4	B [^] 2
H5	0	A14	A [^] 14	B2	B [^] 1

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
105	1	VCCO (Bank 1)	-
106	1	H6	H ⁵
107	1	H5	H ⁴
108	1	H4	H ³
109	1	H2	H ²
110	1	H1	H ¹
111	1	H0/GOE1	H ⁰
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A ⁰
117	0	A1	A ¹
118	0	A2	A ²
119	0	A4	A ³
120	0	A5	A ⁴
121	0	A6	A ⁵
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A ⁶
125	0	A9	A ⁷
126	0	A10	A ⁸
127	0	A12	A ⁹
128	0	A14	A ¹¹

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	GND	-	GND	-	GND	-
B2	-	TDI	-	TDI	-	TDI	-
C1	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
C3	0	NC	-	B0	B ⁰	C12	C ⁶
C2	0	A8	A ⁸	B1	B ¹	C10	C ⁵
D1	0	A9	A ⁹	B2	B ²	C8	C ⁴
D3	0	A10	A ¹⁰	B4	B ³	C6	C ³
D2	0	A11	A ¹¹	B5	B ⁴	C4	C ²
E1	0	NC	-	B6	B ⁵	C2	C ¹
E2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D [^] 7	G4	G [^] 2
44	0	D8	D [^] 6	G2	G [^] 1
45	0	NC ²	-	I ²	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D [^] 5	H12	H [^] 6
49	0	D5	D [^] 4	H10	H [^] 5
50	0	D4	D [^] 3	H8	H [^] 4
51	0	D2	D [^] 2	H6	H [^] 3
52	0	D1	D [^] 1	H4	H [^] 2
53	0	D0	D [^] 0	H2	H [^] 1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E [^] 0	I2	I [^] 1
59	1	E1	E [^] 1	I4	I [^] 2
60	1	E2	E [^] 2	I6	I [^] 3
61	1	E4	E [^] 3	I8	I [^] 4
62	1	E5	E [^] 4	I10	I [^] 5
63	1	E6	E [^] 5	I12	I [^] 6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E [^] 6	J2	J [^] 1
67	1	E9	E [^] 7	J4	J [^] 2
68	1	E10	E [^] 8	J6	J [^] 3
69	1	E12	E [^] 9	J8	J [^] 4
70	1	E13	E [^] 10	J10	J [^] 5
71	1	E14	E [^] 11	J12	J [^] 6
72	1	NC ²	-	I ²	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F [^] 0	K12	K [^] 6
77	1	F1	F [^] 1	K10	K [^] 5
78	1	F2	F [^] 2	K8	K [^] 4
79	1	F4	F [^] 3	K6	K [^] 3
80	1	F5	F [^] 4	K4	K [^] 2
81	1	F6	F [^] 5	K2	K [^] 1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F [^] 6	L14	L [^] 7
84	1	F9	F [^] 7	L12	L [^] 6
85	1	F10	F [^] 8	L10	L [^] 5

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F ⁹	L8	L ⁴
87	1	F13	F ¹⁰	L6	L ³
88	1	F14	F ¹¹	L4	L ²
89	1	NC ²	-	I ²	-
90	1	GND (Bank 1) ¹	-	NC ¹	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC ²	-	I ²	-
93	1	G14	G ¹¹	M2	M ¹
94	1	G13	G ¹⁰	M4	M ²
95	1	G12	G ⁹	M6	M ³
96	1	G10	G ⁸	M8	M ⁴
97	1	G9	G ⁷	M10	M ⁵
98	1	G8	G ⁶	M12	M ⁶
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G ⁵	N2	N ¹
101	1	G5	G ⁴	N4	N ²
102	1	G4	G ³	N6	N ³
103	1	G2	G ²	N8	N ⁴
104	1	G1	G ¹	N10	N ⁵
105	1	G0	G ⁰	N12	N ⁶
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC ²	-	I ²	-
111	1	H14	H ¹¹	O12	O ⁶
112	1	H13	H ¹⁰	O10	O ⁵
113	1	H12	H ⁹	O8	O ⁴
114	1	H10	H ⁸	O6	O ³
115	1	H9	H ⁷	O4	O ²
116	1	H8	H ⁶	O2	O ¹
117	1	NC ²	-	I ²	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H ⁵	P12	P ⁶
121	1	H5	H ⁴	P10	P ⁵
122	1	H4	H ³	P8	P ⁴
123	1	H2	H ²	P6	P ³
124	1	H1	H ¹	P4	P ²
125	1	H0/GOE1	H ⁰	P2/GOE1	P ¹
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E ⁷	E10	E ⁷	H14	H ⁷	J14	J ⁷
K3	0	NC	-	E12	E ⁸	G0	G ⁰	I0	I ⁰
K4	0	NC	-	E14	E ⁹	G2	G ¹	I4	I ¹
L1	0	NC	-	NC	-	I14	I ⁷	K0	K ⁰
L2	0	NC	-	NC	-	I12	I ⁶	K2	K ¹
M1	0	NC	-	NC	-	NC	-	K4	K ²
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K ³
N1	0	NC	-	NC	-	I10	I ⁵	K8	K ⁴
M3	0	NC	-	NC	-	I8	I ⁴	K10	K ⁵
M4	0	NC	-	F0	F ⁰	G4	G ²	I8	I ²
N2	0	NC	-	F1	F ¹	G6	G ³	I12	I ³
K5	0	F0	F ⁰	F2	F ²	J0	J ⁰	N0	N ⁰
P1	0	F2	F ¹	F4	F ³	J2	J ¹	N2	N ¹
K6	0	F4	F ²	F6	F ⁴	J4	J ²	N4	N ²
N3	0	F6	F ³	F8	F ⁵	J6	J ³	N6	N ³
L5	0	F8	F ⁴	F9	F ⁶	J8	J ⁴	N8	N ⁴
P2	0	F10	F ⁵	F10	F ⁷	J10	J ⁵	N10	N ⁵
L6	0	F12	F ⁶	F12	F ⁸	J12	J ⁶	N12	N ⁶
R1	0	F14	F ⁷	F14	F ⁹	J14	J ⁷	N14	N ⁷
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G ⁹	I6	I ³	K12	K ⁶
M5	0	NC	-	G12	G ⁸	I4	I ²	K14	K ⁷
N4	0	G14	G ⁷	G10	G ⁷	K14	K ⁷	O14	O ⁷
T3	0	G12	G ⁶	G9	G ⁶	K12	K ⁶	O12	O ⁶
R3	0	G10	G ⁵	G8	G ⁵	K10	K ⁵	O10	O ⁵
M6	0	G8	G ⁴	G6	G ⁴	K8	K ⁴	O8	O ⁴
P4	0	G6	G ³	G4	G ³	K6	K ³	O6	O ³
L7	0	G4	G ²	G2	G ²	K4	K ²	O4	O ²
N5	0	G2	G ¹	G1	G ¹	K2	K ¹	O2	O ¹
M7	0	G0	G ⁰	G0	G ⁰	K0	K ⁰	O0	O ⁰
P5	0	NC	-	NC	-	G8	G ⁴	M0	M ⁰
R4	0	NC	-	NC	-	G10	G ⁵	M4	M ¹
T4	0	NC	-	NC	-	NC	-	L0	L ⁰
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M [^] 1	M1	M [^] 1	DX2	DX [^] 1	JX2	JX [^] 1
H14	1	M4	M [^] 2	M2	M [^] 2	DX4	DX [^] 2	JX4	JX [^] 2
H13	1	M6	M [^] 3	M4	M [^] 3	DX6	DX [^] 3	JX6	JX [^] 3
G16	1	M8	M [^] 4	M6	M [^] 4	DX8	DX [^] 4	JX8	JX [^] 4
H12	1	M10	M [^] 5	M8	M [^] 5	DX10	DX [^] 5	JX10	JX [^] 5
G15	1	M12	M [^] 6	M9	M [^] 6	DX12	DX [^] 6	JX12	JX [^] 6
H11	1	M14	M [^] 7	M10	M [^] 7	DX14	DX [^] 7	JX14	JX [^] 7
F16	1	NC	-	M12	M [^] 8	CX0	CX [^] 0	IX0	IX [^] 0
G13	1	NC	-	M14	M [^] 9	CX2	CX [^] 1	IX4	IX [^] 1
G14	1	NC	-	NC	-	EX14	EX [^] 7	KX0	KX [^] 0
F15	1	NC	-	NC	-	EX12	EX [^] 6	KX2	KX [^] 1
E16	1	NC	-	NC	-	NC	-	KX4	KX [^] 2
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX [^] 3
G12	1	NC	-	NC	-	EX10	EX [^] 5	KX8	KX [^] 4
E13	1	NC	-	NC	-	EX8	EX [^] 4	KX10	KX [^] 5
D16	1	NC	-	N0	N [^] 0	CX4	CX [^] 2	IX8	IX [^] 2
E14	1	NC	-	N1	N [^] 1	CX6	CX [^] 3	IX12	IX [^] 3
G11	1	N0	N [^] 0	N2	N [^] 2	FX0	FX [^] 0	NX0	NX [^] 0
D15	1	N2	N [^] 1	N4	N [^] 3	FX2	FX [^] 1	NX2	NX [^] 1
F11	1	N4	N [^] 2	N6	N [^] 4	FX4	FX [^] 2	NX4	NX [^] 2
C16	1	N6	N [^] 3	N8	N [^] 5	FX6	FX [^] 3	NX6	NX [^] 3
F12	1	N8	N [^] 4	N9	N [^] 6	FX8	FX [^] 4	NX8	NX [^] 4
D14	1	N10	N [^] 5	N10	N [^] 7	FX10	FX [^] 5	NX10	NX [^] 5
C15	1	N12	N [^] 6	N12	N [^] 8	FX12	FX [^] 6	NX12	NX [^] 6
B16	1	N14	N [^] 7	N14	N [^] 9	FX14	FX [^] 7	NX14	NX [^] 7
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX [^] 3	KX12	KX [^] 6
B14	1	NC	-	NC	-	EX4	EX [^] 2	KX14	KX [^] 7
E12	1	O14	O [^] 7	O14	O [^] 9	GX14	GX [^] 7	OX14	OX [^] 7
A14	1	O12	O [^] 6	O12	O [^] 8	GX12	GX [^] 6	OX12	OX [^] 6
C13	1	O10	O [^] 5	O10	O [^] 7	GX10	GX [^] 5	OX10	OX [^] 5
D13	1	O8	O [^] 4	O9	O [^] 6	GX8	GX [^] 4	OX8	OX [^] 4
E11	1	O6	O [^] 3	O8	O [^] 5	GX6	GX [^] 3	OX6	OX [^] 3
B13	1	O4	O [^] 2	O6	O [^] 4	GX4	GX [^] 2	OX4	OX [^] 2
F10	1	O2	O [^] 1	O4	O [^] 3	GX2	GX [^] 1	OX2	OX [^] 1

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC ¹	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC ¹	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC ¹	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC ¹	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC ¹	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC ¹	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C ¹	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C ¹	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C ¹	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C ¹	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C ¹	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C ¹	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-5FT256I	384	2.5	5	ftBGA	256	192	I
	LC4384B-75FT256I	384	2.5	7.5	ftBGA	256	192	I
	LC4384B-10FT256I	384	2.5	10	ftBGA	256	192	I
	LC4384B-5F256I ¹	384	2.5	5	fpBGA	256	192	I
	LC4384B-75F256I ¹	384	2.5	7.5	fpBGA	256	192	I
	LC4384B-10F256I ¹	384	2.5	10	fpBGA	256	192	I
	LC4384B-5T176I	384	2.5	5	TQFP	176	128	I
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128	I
	LC4384B-10T176I	384	2.5	10	TQFP	176	128	I
LC4512B	LC4512B-5FT256I	512	2.5	5	ftBGA	256	208	I
	LC4512B-75FT256I	512	2.5	7.5	ftBGA	256	208	I
	LC4512B-10FT256I	512	2.5	10	ftBGA	256	208	I
	LC4512B-5F256I ¹	512	2.5	5	fpBGA	256	208	I
	LC4512B-75F256I ¹	512	2.5	7.5	fpBGA	256	208	I
	LC4512B-10F256I ¹	512	2.5	10	fpBGA	256	208	I
	LC4512B-5T176I	512	2.5	5	TQFP	176	128	I
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
	LC4512B-10T176I	512	2.5	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32	C
	LC4032V-5T48C	32	3.3	5	TQFP	48	32	C
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32	C
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30	C
	LC4032V-5T44C	32	3.3	5	TQFP	44	30	C
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30	C
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64	C
	LC4064V-5T100C	64	3.3	5	TQFP	100	64	C
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64	C
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32	C
	LC4064V-5T48C	64	3.3	5	TQFP	48	32	C
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32	C
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30	C
	LC4064V-5T44C	64	3.3	5	TQFP	44	30	C
	LC4064V-75T44C	64	3.3	7.5	TQFP	44	30	C

ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512C	LC4512C-35FTN256C	512	1.8	3.5	Lead-free ftBGA	256	208	C
	LC4512C-5FTN256C	512	1.8	5	Lead-free ftBGA	256	208	C
	LC4512C-75FTN256C	512	1.8	7.5	Lead-free ftBGA	256	208	C
	LC4512C-35FN256C ¹	512	1.8	3.5	Lead-free fpBGA	256	208	C
	LC4512C-5FN256C ¹	512	1.8	5	Lead-free fpBGA	256	208	C
	LC4512C-75FN256C ¹	512	1.8	7.5	Lead-free fpBGA	256	208	C
	LC4512C-35TN176C	512	1.8	3.5	Lead-free TQFP	176	128	C
	LC4512C-5TN176C	512	1.8	5	Lead-free TQFP	176	128	C
	LC4512C-75TN176C	512	1.8	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000C (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032C-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I
	LC4032C-10TN48I	32	1.8	10	Lead-free TQFP	48	32	I
	LC4032C-5TN44I	32	1.8	5	Lead-free TQFP	44	30	I
	LC4032C-75TN44I	32	1.8	7.5	Lead-free TQFP	44	30	I
	LC4032C-10TN44I	32	1.8	10	Lead-free TQFP	44	30	I
LC4064C	LC4064C-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064C-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064C-10TN100I	64	1.8	10	Lead-free TQFP	100	64	I
	LC4064C-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064C-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
	LC4064C-10TN48I	64	1.8	10	Lead-free TQFP	48	32	I
	LC4064C-5TN44I	64	1.8	5	Lead-free TQFP	44	30	I
	LC4064C-75TN44I	64	1.8	5	Lead-free TQFP	44	30	I
	LC4064C-10TN44I	64	1.8	10	Lead-free TQFP	44	30	I
LC4128C	LC4128C-5TN128I	128	1.8	5	Lead-free TQFP	128	92	I
	LC4128C-75TN128I	128	1.8	7.5	Lead-free TQFP	128	92	I
	LC4128C-10TN128I	128	1.8	10	Lead-free TQFP	128	92	I
	LC4128C-5TN100I	128	1.8	5	Lead-free TQFP	100	64	I
	LC4128C-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
	LC4128C-10TN100I	128	1.8	10	Lead-free TQFP	100	64	I

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI ¹	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI ¹	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI ¹	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI ¹	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI ¹	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI ¹	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I ¹	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I ¹	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I ¹	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I ¹	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I ¹	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I ¹	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I

ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ($0 \leq V_{IN} \leq 3.6V$).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
		Improved LC4064ZC t _S to 2.5ns, t _{ST} to 2.7ns and f _{MAX} (Ext.) to 175MHz, LC4128ZC t _{CO} to 3.5ns and f _{MAX} (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs