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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

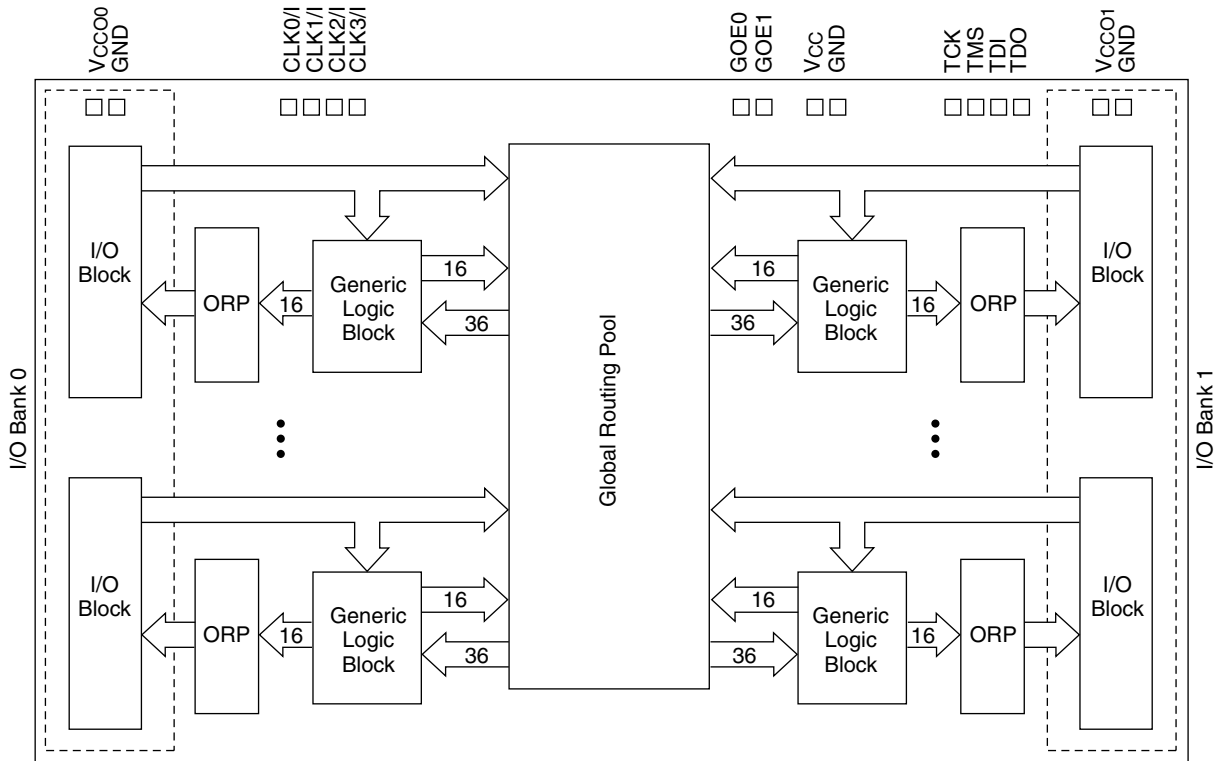
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	-
Number of I/O	208
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4512v-5ftn256i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4512v-5ftn256i</a>

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to  $V_{CC0}$  of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

## ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

### Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

**Table 5. Product Term Expansion Capability**

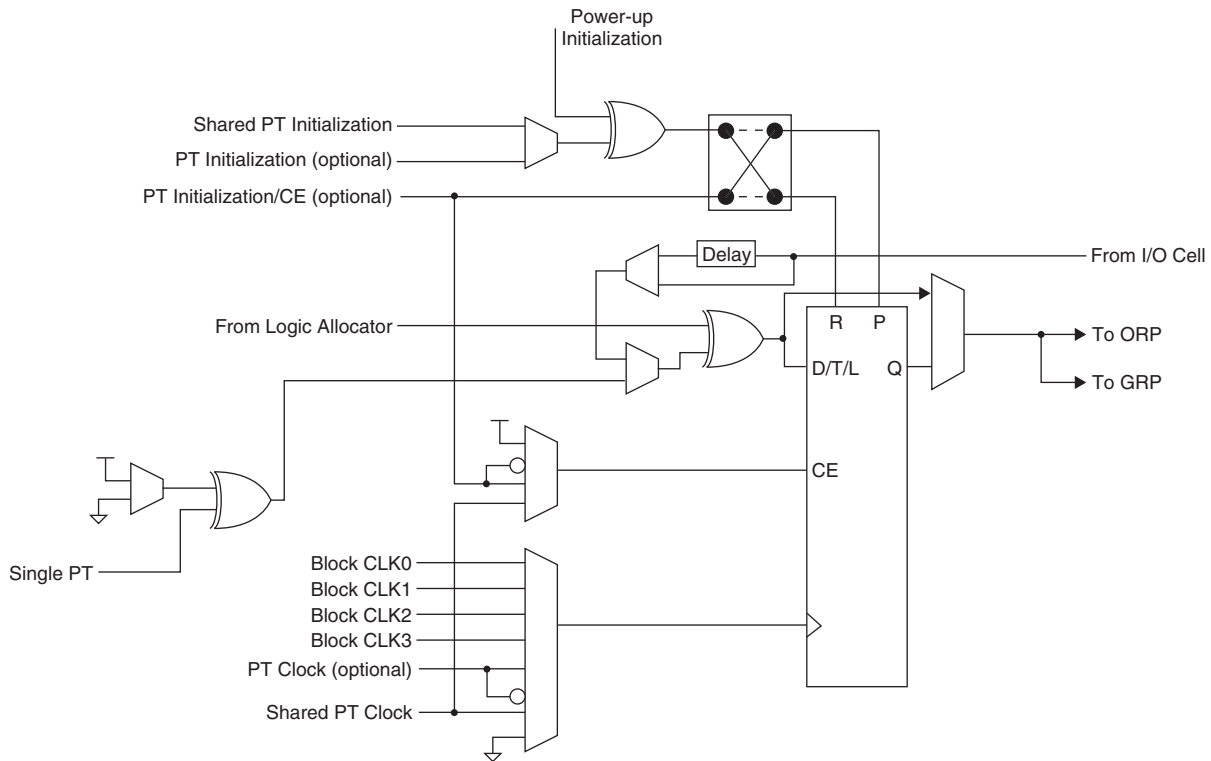
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of  $t_{EXP}$ . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

**Macrocell**

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

**Figure 5. Macrocell**



**Enhanced Clock Multiplexer**

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

## I/O Recommended Operating Conditions

Standard	$V_{CCO}$ (V) <sup>1</sup>	
	Min.	Max.
LVTTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3 <sup>2</sup>	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for  $V_{CCO}$  are the average of the min. and max. values.

2. ispMACH 4000Z only.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input Leakage Current (ispMACH 4000Z)	$0 \leq V_{IN} < V_{CCO}$	—	0.5	1	$\mu A$
$I_{IH}^1$	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \leq 5.5V$	—	—	10	$\mu A$
$I_{IL}, I_{IH}^1$	Input Leakage Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$	—	—	10	$\mu A$
		$0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$	—	—	15	$\mu A$
$I_{IH}^{1,2}$	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	20	$\mu A$
		$3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	50	$\mu A$
$I_{PU}$	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-150	$\mu A$
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-200	$\mu A$
$I_{PD}$	I/O Weak Pull-down Resistor Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$	30	—	150	$\mu A$
$I_{BHLS}$	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	$\mu A$
$I_{BHHS}$	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	$\mu A$
$I_{BHLO}$	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{BHT}$	—	—	150	$\mu A$
$I_{BHHO}$	Bus Hold High Overdrive Current	$V_{BHT} \leq V_{IN} \leq V_{CCO}$	—	—	-150	$\mu A$
$V_{BHT}$	Bus Hold Trip Points	—	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
$C_1$	I/O Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_2$	Clock Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_3$	Global Input Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where  $3.0V \leq V_{CCO} \leq 3.6V$ .

3.  $T_A = 25^\circ C, f = 1.0MHz$

4.  $I_{IH}$  excursions of up to 1.5 $\mu A$  maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

### Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I <sub>CC</sub> <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	13	—	mA
		V <sub>CC</sub> = 2.5V	—	13	—	mA
		V <sub>CC</sub> = 1.8V	—	3	—	mA

1. T<sub>A</sub> = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I<sub>CC</sub> varies with specific device configuration and operating frequency.
4. T<sub>A</sub> = 25°C

### Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4032ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	50	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	58	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	60	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	70	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	10	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	13	20	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	15	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	22	—	μA
<b>ispMACH 4064ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	80	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	89	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	92	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	109	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	11	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	15	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	18	35	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	37	—	μA
<b>ispMACH 4128ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	168	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	190	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	195	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	212	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	12	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	16	35	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	19	50	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	42	—	μA

## ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>								
t <sub>IN</sub>	Input Buffer Delay	—	0.95	—	1.50	—	2.00	ns
t <sub>GOE</sub>	Global OE Pin Delay	—	4.04	—	6.04	—	7.04	ns
t <sub>GCLK_IN</sub>	Global Clock Input Buffer Delay	—	1.83	—	2.28	—	3.28	ns
t <sub>BUF</sub>	Delay through Output Buffer	—	1.00	—	1.50	—	1.50	ns
t <sub>EN</sub>	Output Enable Time	—	0.96	—	0.96	—	0.96	ns
t <sub>DIS</sub>	Output Disable Time	—	0.96	—	0.96	—	0.96	ns
<b>Routing/GLB Delays</b>								
t <sub>ROUTE</sub>	Delay through GRP	—	1.51	—	2.26	—	3.26	ns
t <sub>MCELL</sub>	Macrocell Delay	—	1.05	—	1.45	—	1.95	ns
t <sub>INREG</sub>	Input Buffer to Macrocell Register Delay	—	0.56	—	0.96	—	1.46	ns
t <sub>FBK</sub>	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	ns
t <sub>PDb</sub>	5-PT Bypass Propagation Delay	—	1.54	—	2.24	—	3.24	ns
t <sub>PDi</sub>	Macrocell Propagation Delay	—	0.94	—	1.24	—	1.74	ns
<b>Register/Latch Delays</b>								
t <sub>S</sub>	D-Register Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t <sub>S_PT</sub>	D-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t <sub>ST</sub>	T-Register Setup Time (Global Clock)	1.52	—	1.77	—	1.77	—	ns
t <sub>ST_PT</sub>	T-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t <sub>H</sub>	D-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t <sub>HT</sub>	T-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t <sub>SIR</sub>	D-Input Register Setup Time (Global Clock)	1.52	—	1.57	—	1.57	—	ns
t <sub>SIR_PT</sub>	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t <sub>HIR</sub>	D-Input Register Hold Time (Global Clock)	0.68	—	1.18	—	1.18	—	ns
t <sub>HIR_PT</sub>	D-Input Register Hold Time (Product Term Clock)	0.68	—	1.18	—	1.18	—	ns
t <sub>COi</sub>	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.67	—	1.17	ns
t <sub>CES</sub>	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	ns
t <sub>CEH</sub>	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	ns
t <sub>SL</sub>	Latch Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t <sub>SL_PT</sub>	Latch Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t <sub>HL</sub>	Latch Hold Time	1.17	—	1.17	—	1.17	—	ns
t <sub>GOi</sub>	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t <sub>PDLi</sub>	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t <sub>SRI</sub>	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	ns
t <sub>SRR</sub>	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	ns
<b>Control Delays</b>								
t <sub>BCLK</sub>	GLB PT Clock Delay	—	1.12	—	1.12	—	0.62	ns
t <sub>PTCLK</sub>	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	ns
t <sub>BSR</sub>	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t <sub>PTSR</sub>	Macrocell PT Set/Reset Delay	—	2.51	—	3.41	—	3.41	ns

## ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>								
t <sub>IN</sub>	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t <sub>GOE</sub>	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t <sub>GCLK_IN</sub>	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t <sub>BUF</sub>	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t <sub>EN</sub>	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t <sub>DIS</sub>	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
<b>Routing/GLB Delays</b>								
t <sub>ROUTE</sub>	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t <sub>MCELL</sub>	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t <sub>INREG</sub>	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t <sub>FBK</sub>	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t <sub>PDb</sub>	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t <sub>PDi</sub>	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
<b>Register/Latch Delays</b>								
t <sub>S</sub>	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>S_PT</sub>	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t <sub>ST</sub>	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t <sub>ST_PT</sub>	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t <sub>H</sub>	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>HT</sub>	T-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>SIR</sub>	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t <sub>SIR_PT</sub>	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t <sub>HIR</sub>	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t <sub>HIR_PT</sub>	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t <sub>COi</sub>	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t <sub>CES</sub>	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t <sub>CEH</sub>	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t <sub>SL</sub>	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>SL_PT</sub>	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t <sub>HL</sub>	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t <sub>GOi</sub>	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t <sub>PDLi</sub>	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t <sub>SRI</sub>	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t <sub>SRR</sub>	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
<b>Control Delays</b>								
t <sub>BCLK</sub>	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t <sub>PTCLK</sub>	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t <sub>BSR</sub>	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t <sub>PTSR</sub>	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

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**ispMACH 4000Z Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>P<sub>TOE</sub></sub>	Macrocell PT OE Delay	—	2.50	—	2.70	—	2.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details. Timing v.2.2



ispMACH 4000V/B/C Timing Adders<sup>1</sup>

Adder Type	Base Parameter	Description	-25		-27		-3		-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>											
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	0.95	—	1.00	—	1.00	—	1.00	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.33	—	0.33	—	0.33	—	0.33	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	—	0.05	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.03	—	0.05	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>											
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>											
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

ispMACH 4000Z Timing Adders <sup>1</sup>

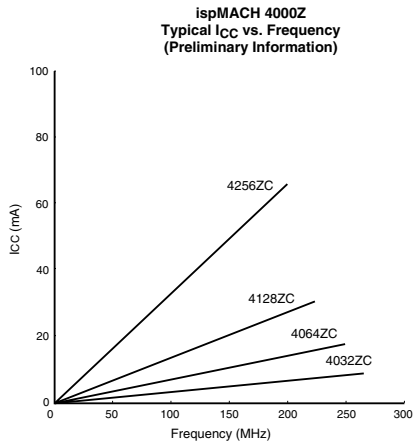
Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.00	—	1.00	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

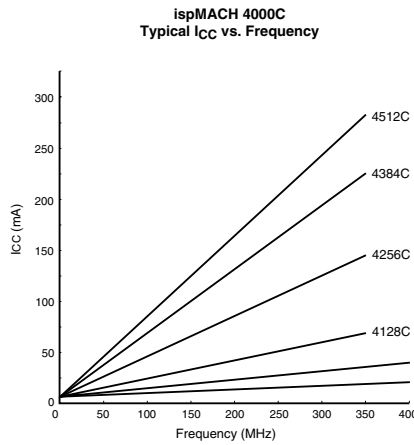
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

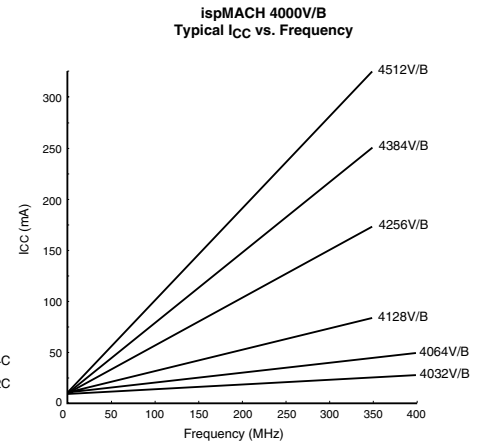
## Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

## Power Estimation Coefficients<sup>1</sup>

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

ispMACH 4000V/B/C/Z Power Supply and NC Connections<sup>1</sup> (Cont.)

Signal	132-ball csBGA <sup>7</sup>	144-pin TQFP <sup>4</sup>	176-pin TQFP <sup>4</sup>	256-ball ftBGA/fpBGA <sup>2,3,7,9</sup>
VCC	P1, A14, B7, N8	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
VCCO0 VCCO (Bank 0)	G3, P5, C1 <sup>8</sup> , M2 <sup>8</sup> , C5	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1 VCCO (Bank 1)	M10, M14 <sup>8</sup> , H12, A10, C13 <sup>8</sup>	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	B1, P2, N14, A13	1, 37, 73, 109	2, 46 <sup>5</sup> , 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank 0)	E2, K2, N4, B4	10, 18 <sup>6</sup> , 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	N11, K13, E13, B11	55, 65, 82, 90 <sup>6</sup> , 99, 118	67, 79, 101, 119, 143	
NC	<b>4064Z:</b> C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1  <b>4128Z:</b> P8, A7	<b>4128V:</b> 17, 20, 38, 45, 72, 89, 92, 110, 117, 144  <b>4256V:</b> 18, 90	1, 43, 44, 45, 89, 131, 132, 133	<b>4256V/B/C, 128 I/O:</b> A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15  <b>4256V/B/C, 160 I/O:</b> A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15  <b>4384V/B/C:</b> B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4  <b>4512V/B/C:</b> None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. V<sub>CCO</sub> balls connect to two power planes within the package, one for V<sub>CCO0</sub> and one for V<sub>CCO1</sub>.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
K5	0	A15	A <sup>15</sup>	B0	B <sup>0</sup>
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B <sup>0</sup>	C0	C <sup>0</sup>
K7	1	B1	B <sup>1</sup>	C1	C <sup>1</sup>
K8	1	B2	B <sup>2</sup>	C2	C <sup>2</sup>
K9	1	B3	B <sup>3</sup>	C4	C <sup>3</sup>
K10	1	B4	B <sup>4</sup>	C6	C <sup>4</sup>
J10	-	TMS	-	TMS	-
H8	1	B5	B <sup>5</sup>	C8	C <sup>5</sup>
H10	1	B6	B <sup>6</sup>	C10	C <sup>6</sup>
G10	1	B7	B <sup>7</sup>	C11	C <sup>7</sup>
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
F10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B <sup>8</sup>	D15	D <sup>7</sup>
D8	1	B9	B <sup>9</sup>	D12	D <sup>6</sup>
D10	1	B10	B <sup>10</sup>	D10	D <sup>5</sup>
C10	1	B11	B <sup>11</sup>	D8	D <sup>4</sup>
B10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A7	1	B12	B <sup>12</sup>	D6	D <sup>3</sup>
C7	1	B13	B <sup>13</sup>	D4	D <sup>2</sup>
C6	1	B14	B <sup>14</sup>	D2	D <sup>1</sup>
A6	1	B15/GOE1	B <sup>15</sup>	D0/GOE1	D <sup>0</sup>
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>
A4	0	A1	A <sup>1</sup>	A1	A <sup>1</sup>
A3	0	A2	A <sup>2</sup>	A2	A <sup>2</sup>
A2	0	A3	A <sup>3</sup>	A4	A <sup>3</sup>
A1	0	A4	A <sup>4</sup>	A6	A <sup>4</sup>

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

**ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F <sup>9</sup>	L8	L <sup>4</sup>
87	1	F13	F <sup>10</sup>	L6	L <sup>3</sup>
88	1	F14	F <sup>11</sup>	L4	L <sup>2</sup>
89	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
90	1	GND (Bank 1) <sup>1</sup>	-	NC <sup>1</sup>	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
93	1	G14	G <sup>11</sup>	M2	M <sup>1</sup>
94	1	G13	G <sup>10</sup>	M4	M <sup>2</sup>
95	1	G12	G <sup>9</sup>	M6	M <sup>3</sup>
96	1	G10	G <sup>8</sup>	M8	M <sup>4</sup>
97	1	G9	G <sup>7</sup>	M10	M <sup>5</sup>
98	1	G8	G <sup>6</sup>	M12	M <sup>6</sup>
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G <sup>5</sup>	N2	N <sup>1</sup>
101	1	G5	G <sup>4</sup>	N4	N <sup>2</sup>
102	1	G4	G <sup>3</sup>	N6	N <sup>3</sup>
103	1	G2	G <sup>2</sup>	N8	N <sup>4</sup>
104	1	G1	G <sup>1</sup>	N10	N <sup>5</sup>
105	1	G0	G <sup>0</sup>	N12	N <sup>6</sup>
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
111	1	H14	H <sup>11</sup>	O12	O <sup>6</sup>
112	1	H13	H <sup>10</sup>	O10	O <sup>5</sup>
113	1	H12	H <sup>9</sup>	O8	O <sup>4</sup>
114	1	H10	H <sup>8</sup>	O6	O <sup>3</sup>
115	1	H9	H <sup>7</sup>	O4	O <sup>2</sup>
116	1	H8	H <sup>6</sup>	O2	O <sup>1</sup>
117	1	NC <sup>2</sup>	-	I <sup>2</sup>	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H <sup>5</sup>	P12	P <sup>6</sup>
121	1	H5	H <sup>4</sup>	P10	P <sup>5</sup>
122	1	H4	H <sup>3</sup>	P8	P <sup>4</sup>
123	1	H2	H <sup>2</sup>	P6	P <sup>3</sup>
124	1	H1	H <sup>1</sup>	P4	P <sup>2</sup>
125	1	H0/GOE1	H <sup>0</sup>	P2/GOE1	P <sup>1</sup>
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
60	0	H8	H <sup>4</sup>	L8	L <sup>4</sup>	P8	P <sup>4</sup>
61	0	H6	H <sup>3</sup>	L6	L <sup>3</sup>	P6	P <sup>3</sup>
62	0	H4	H <sup>2</sup>	L4	L <sup>2</sup>	P4	P <sup>2</sup>
63	0	H2	H <sup>1</sup>	L2	L <sup>1</sup>	P2	P <sup>1</sup>
64	0	H0	H <sup>0</sup>	L0	L <sup>0</sup>	P0	P <sup>0</sup>
65	-	GND	-	GND	-	GND	-
66	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
67	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
68	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
69	-	VCC	-	VCC	-	VCC	-
70	1	I0	I <sup>0</sup>	M0	M <sup>0</sup>	AX0	AX <sup>0</sup>
71	1	I2	I <sup>1</sup>	M2	M <sup>1</sup>	AX2	AX <sup>1</sup>
72	1	I4	I <sup>2</sup>	M4	M <sup>2</sup>	AX4	AX <sup>2</sup>
73	1	I6	I <sup>3</sup>	M6	M <sup>3</sup>	AX6	AX <sup>3</sup>
74	1	I8	I <sup>4</sup>	M8	M <sup>4</sup>	AX8	AX <sup>4</sup>
75	1	I10	I <sup>5</sup>	M10	M <sup>5</sup>	AX10	AX <sup>5</sup>
76	1	I12	I <sup>6</sup>	M12	M <sup>6</sup>	AX12	AX <sup>6</sup>
77	1	I14	I <sup>7</sup>	M14	M <sup>7</sup>	AX14	AX <sup>7</sup>
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
79	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
80	1	J0	J <sup>0</sup>	N0	N <sup>0</sup>	BX0	BX <sup>0</sup>
81	1	J2	J <sup>1</sup>	N2	N <sup>1</sup>	BX2	BX <sup>1</sup>
82	1	J4	J <sup>2</sup>	N4	N <sup>2</sup>	BX4	BX <sup>2</sup>
83	1	J6	J <sup>3</sup>	N6	N <sup>3</sup>	BX6	BX <sup>3</sup>
84	1	J8	J <sup>4</sup>	N8	N <sup>4</sup>	BX8	BX <sup>4</sup>
85	1	J10	J <sup>5</sup>	N10	N <sup>5</sup>	BX10	BX <sup>5</sup>
86	1	J12	J <sup>6</sup>	N12	N <sup>6</sup>	BX12	BX <sup>6</sup>
87	1	J14	J <sup>7</sup>	N14	N <sup>7</sup>	BX14	BX <sup>7</sup>
88	-	VCC	-	VCC	-	VCC	-
89	-	NC	-	NC	-	NC	-
90	-	GND	-	GND	-	GND	-
91	-	TMS	-	TMS	-	TMS	-
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
93	1	K14	K <sup>7</sup>	O14	O <sup>7</sup>	CX14	CX <sup>7</sup>
94	1	K12	K <sup>6</sup>	O12	O <sup>6</sup>	CX12	CX <sup>6</sup>
95	1	K10	K <sup>5</sup>	O10	O <sup>5</sup>	CX10	CX <sup>5</sup>
96	1	K8	K <sup>4</sup>	O8	O <sup>4</sup>	CX8	CX <sup>4</sup>
97	1	K6	K <sup>3</sup>	O6	O <sup>3</sup>	CX6	CX <sup>3</sup>
98	1	K4	K <sup>2</sup>	O4	O <sup>2</sup>	CX4	CX <sup>2</sup>
99	1	K2	K <sup>1</sup>	O2	O <sup>1</sup>	CX2	CX <sup>1</sup>
100	1	K0	K <sup>0</sup>	O0	O <sup>0</sup>	CX0	CX <sup>0</sup>

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L^1
T5	0	NC	-	NC	-	I2	I^1	L8	L^2
R6	0	NC	-	NC	-	I0	I^0	L12	L^3
T6	0	NC	-	H14	H^9	G12	G^6	M8	M^2
N7	0	NC	-	H12	H^8	G14	G^7	M12	M^3
P7	0	H14	H^7	H10	H^7	L14	L^7	P14	P^7
R7	0	H12	H^6	H9	H^6	L12	L^6	P12	P^6
L8	0	H10	H^5	H8	H^5	L10	L^5	P10	P^5
T7	0	H8	H^4	H6	H^4	L8	L^4	P8	P^4
M8	0	H6	H^3	H4	H^3	L6	L^3	P6	P^3
N8	0	H4	H^2	H2	H^2	L4	L^2	P4	P^2
R8	0	H2	H^1	H1	H^1	L2	L^1	P2	P^1
P8	0	H0	H^0	H0	H^0	L0	L^0	P0	P^0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I^0	I0	I^0	M0	M^0	AX0	AX^0
R9	1	I2	I^1	I1	I^1	M2	M^1	AX2	AX^1
T9	1	I4	I^2	I2	I^2	M4	M^2	AX4	AX^2
T10	1	I6	I^3	I4	I^3	M6	M^3	AX6	AX^3
R10	1	I8	I^4	I6	I^4	M8	M^4	AX8	AX^4
M9	1	I10	I^5	I8	I^5	M10	M^5	AX10	AX^5
P10	1	I12	I^6	I9	I^6	M12	M^6	AX12	AX^6
L9	1	I14	I^7	I10	I^7	M14	M^7	AX14	AX^7
N10	1	NC	-	I12	I^8	BX14	BX^7	DX0	DX^0
T11	1	NC	-	I14	I^9	BX12	BX^6	DX4	DX^1
R11	1	NC	-	NC	-	P0	P^0	EX0	EX^0
T12	1	NC	-	NC	-	P2	P^1	EX4	EX^1
N12	1	NC	-	NC	-	NC	-	EX8	EX^2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX^3
T13	1	NC	-	J0	J^0	BX10	BX^5	DX8	DX^2
P12	1	NC	-	J1	J^1	BX8	BX^4	DX12	DX^3
M10	1	J0	J^0	J2	J^2	N0	N^0	BX0	BX^0
R13	1	J2	J^1	J4	J^3	N2	N^1	BX2	BX^1
L10	1	J4	J^2	J6	J^4	N4	N^2	BX4	BX^2
T14	1	J6	J^3	J8	J^5	N6	N^3	BX6	BX^3
M11	1	J8	J^4	J9	J^6	N8	N^4	BX8	BX^4



### Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).  
 2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

### ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

## ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC <sup>1</sup>	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC <sup>1</sup>	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC <sup>1</sup>	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC <sup>1</sup>	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC <sup>1</sup>	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC <sup>1</sup>	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C	
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C <sup>1</sup>	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C <sup>1</sup>	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C <sup>1</sup>	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

## ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI <sup>1</sup>	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI <sup>1</sup>	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I	
LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I	
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I <sup>1</sup>	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I <sup>1</sup>	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I <sup>1</sup>	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I	
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I <sup>1</sup>	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I <sup>1</sup>	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I <sup>1</sup>	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I	

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4128B	LC4128B-5TN128I	128	2.5	5	Lead-Free TQFP	128	92	I
	LC4128B-75TN128I	128	2.5	7.5	Lead-Free TQFP	128	92	I
	LC4128B-10TN128I	128	2.5	10	Lead-Free TQFP	128	92	I
	LC4128B-5TN100I	128	2.5	5	Lead-Free TQFP	100	64	I
	LC4128B-75TN100I	128	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4128B-10TN100I	128	2.5	10	Lead-Free TQFP	100	64	I
LC4256B	LC4256B-5FTN256AI	256	2.5	5	Lead-Free ftBGA	256	128	I
	LC4256B-75FTN256AI	256	2.5	7.5	Lead-Free ftBGA	256	128	I
	LC4256B-10FTN256AI	256	2.5	10	Lead-Free ftBGA	256	128	I
	LC4256B-5FTN256BI	256	2.5	5	Lead-Free ftBGA	256	160	I
	LC4256B-75FTN256BI	256	2.5	7.5	Lead-Free ftBGA	256	160	I
	LC4256B-10FTN256BI	256	2.5	10	Lead-Free ftBGA	256	160	I
	LC4256B-5FN256AI <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	128	I
	LC4256B-75FN256AI <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	128	I
	LC4256B-10FN256AI <sup>1</sup>	256	2.5	10	Lead-Free fpBGA	256	128	I
	LC4256B-5FN256BI <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	160	I
	LC4256B-75FN256BI <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	160	I
	LC4256B-10FN256BI <sup>1</sup>	256	2.5	10	Lead-Free fpBGA	256	160	I
	LC4256B-5TN176I	256	2.5	5	Lead-Free TQFP	176	128	I
	LC4256B-75TN176I	256	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4256B-10TN176I	256	2.5	10	Lead-Free TQFP	176	128	I
	LC4256B-5TN100I	256	2.5	5	Lead-Free TQFP	100	64	I
LC4256B-75TN100I	256	2.5	7.5	Lead-Free TQFP	100	64	I	
LC4256B-10TN100I	256	2.5	10	Lead-Free TQFP	100	64	I	
LC4384B	LC4384B-5FTN256I	384	2.5	5	Lead-Free ftBGA	256	192	I
	LC4384B-75FTN256I	384	2.5	7.5	Lead-Free ftBGA	256	192	I
	LC4384B-10FTN256I	384	2.5	10	Lead-Free ftBGA	256	192	I
	LC4384B-5FN256I <sup>1</sup>	384	2.5	5	Lead-Free fpBGA	256	192	I
	LC4384B-75FN256I <sup>1</sup>	384	2.5	7.5	Lead-Free fpBGA	256	192	I
	LC4384B-10FN256I <sup>1</sup>	384	2.5	10	Lead-Free fpBGA	256	192	I
	LC4384B-5TN176I	384	2.5	5	Lead-Free TQFP	176	128	I
	LC4384B-75TN176I	384	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4384B-10TN176I	384	2.5	10	Lead-Free TQFP	176	128	I
LC4512B	LC4512B-5FTN256I	512	2.5	5	Lead-Free ftBGA	256	208	I
	LC4512B-75FTN256I	512	2.5	7.5	Lead-Free ftBGA	256	208	I
	LC4512B-10FTN256I	512	2.5	10	Lead-Free ftBGA	256	208	I
	LC4512B-5FN256I <sup>1</sup>	512	2.5	5	Lead-Free fpBGA	256	208	I
	LC4512B-75FN256I <sup>1</sup>	512	2.5	7.5	Lead-Free fpBGA	256	208	I
	LC4512B-10FN256I <sup>1</sup>	512	2.5	10	Lead-Free fpBGA	256	208	I
	LC4512B-5TN176I	512	2.5	5	Lead-Free TQFP	176	128	I
	LC4512B-75TN176I	512	2.5	7.5	Lead-Free TQFP	176	128	I
LC4512B-10TN176I	512	2.5	10	Lead-Free TQFP	176	128	I	

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**Revision History (Cont.)**

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated $I_{PU}$ (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 $\mu$ A to -200 $\mu$ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage ( $I_{IH}$ ) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to "LA" automotive data sheet under the "Broad Device Offering" bullet.
		Added footnote 1 to Part Number Description to reference the "LA" automotive data sheet.
		Changed device temperature references from 'Automotive' to "Extended Temperature" for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to $t_{CW}$ , $t_{GW}$ , $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to $t_{CW}$ , $t_{GW}$ , $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000V/B/C External Switching Characteristics table.