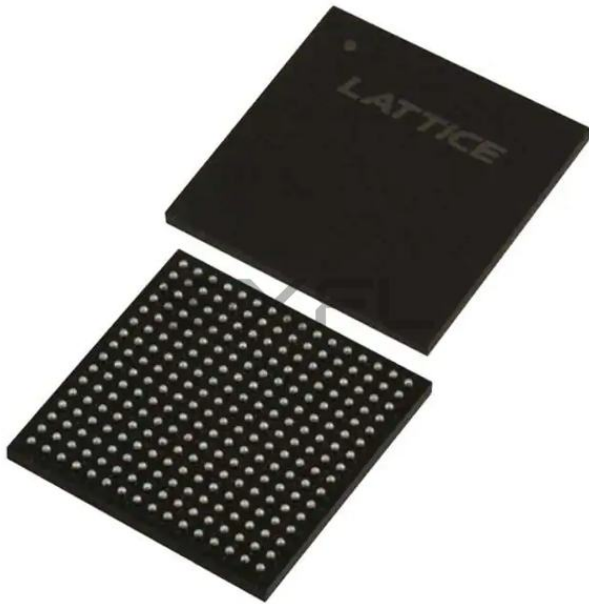




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	-
Number of I/O	208
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4512v-75ft256i

Table 2. ispMACH 4000Z Family Selection Guide

	ispMACH 4032ZC	ispMACH 4064ZC	ispMACH 4128ZC	ispMACH 4256ZC
Macrocells	32	64	128	256
I/O + Dedicated Inputs	32+4/32+4	32+4/32+12/ 64+10/64+10	64+10/96+4	64+10/96+6/ 128+4
t _{PD} (ns)	3.5	3.7	4.2	4.5
t _S (ns)	2.2	2.5	2.7	2.9
t _{CO} (ns)	3.0	3.2	3.5	3.8
f _{MAX} (MHz)	267	250	220	200
Supply Voltage (V)	1.8	1.8	1.8	1.8
Max. Standby I _{CC} (μA)	20	25	35	55
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 TQFP 132 csBGA 176 TQFP

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

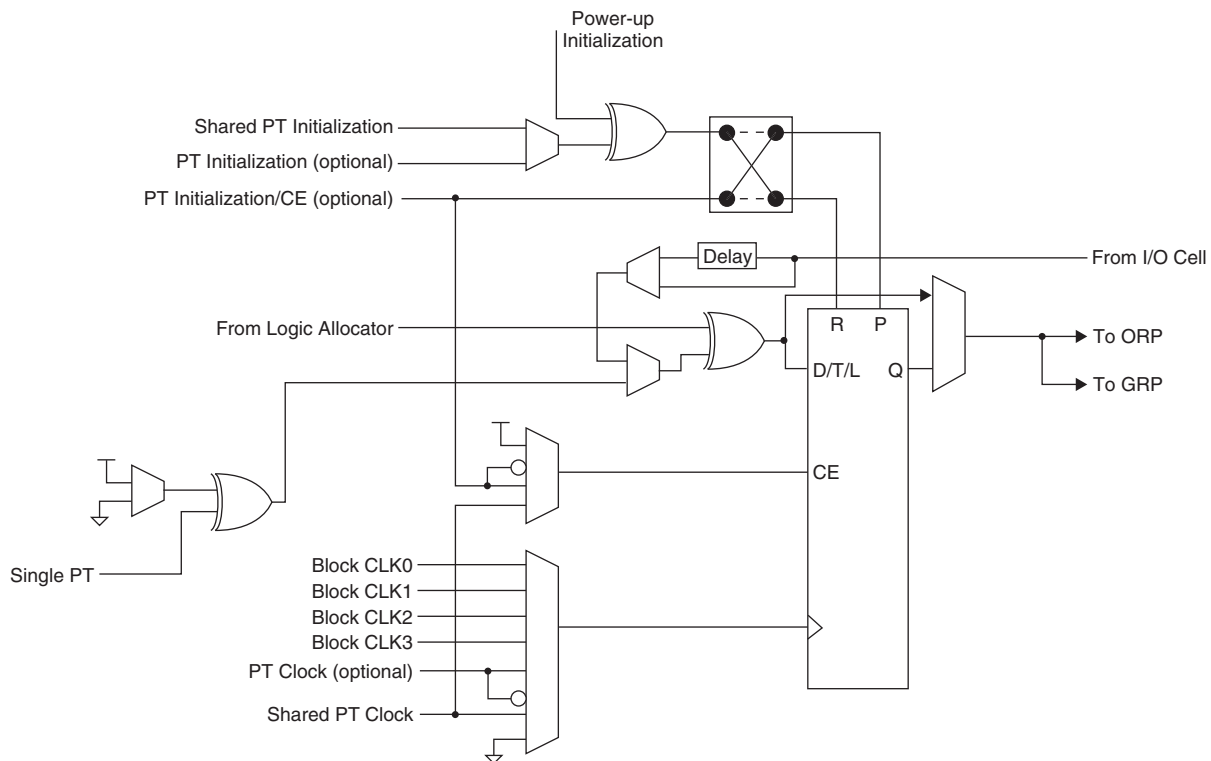
Table 5. Product Term Expansion Capability

Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP} . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell

Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

Figure 10. Global OE Generation for ispMACH 4032

Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice’s ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings^{1, 2, 3}

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied ^{4, 5}	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V _{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6 ^{1, 2}	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T _j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

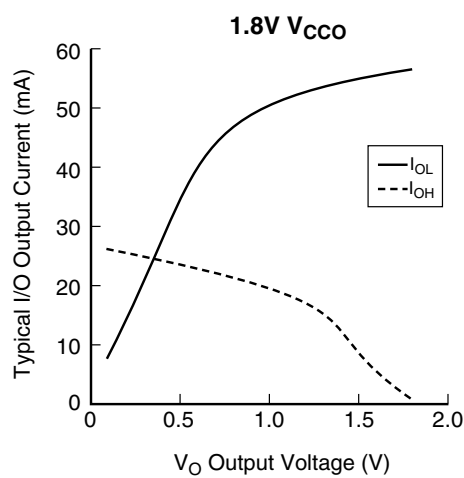
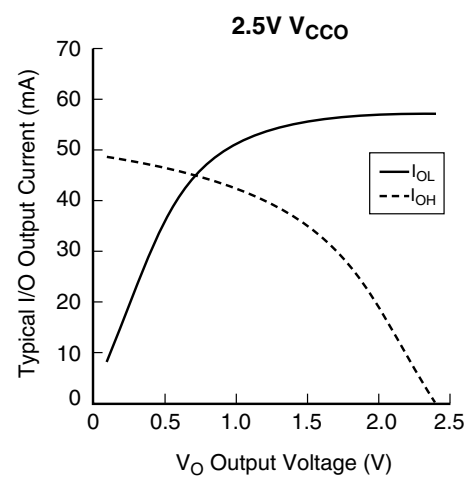
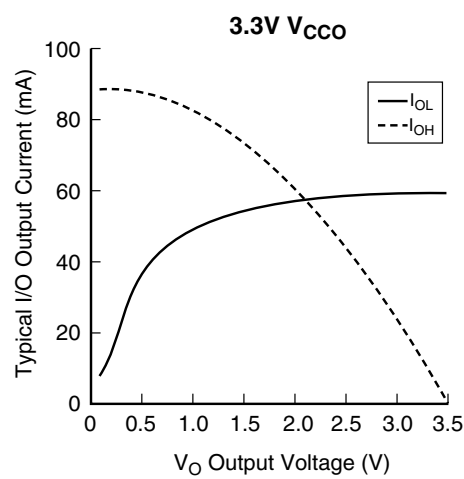
Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics^{1,2,3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, $T_j = 105^\circ C$	—	± 30	± 150	μA
		$0 \leq V_{IN} \leq 3.0V$, $T_j = 130^\circ C$	—	± 30	± 200	μA

1. Insensitive to sequence of V_{CC} or V_{CCO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
2. $0 < V_{CC} < V_{CC} (MAX)$, $0 < V_{CCO} < V_{CCO} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} . Device defaults to pull-up until fuse circuitry is active.



ispMACH 4000V/B/C External Switching Characteristics (Cont.)**Over Recommended Operating Conditions**

Parameter	Description ^{1, 2, 3}	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t_R	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t_{CW}	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t_{WIR}	Input register clock width, high or low	2.2	—	2.8	—	4.0	—	ns
f_{MAX}^4	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
$f_{MAX} (Ext.)$	Clock frequency with external feedback, $[1/(t_S + t_{CO})]$	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.3.2

2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

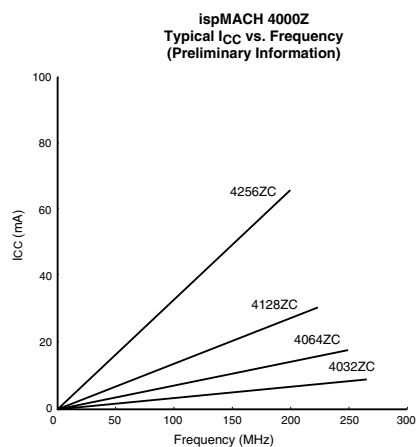
4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C Internal Timing Parameters

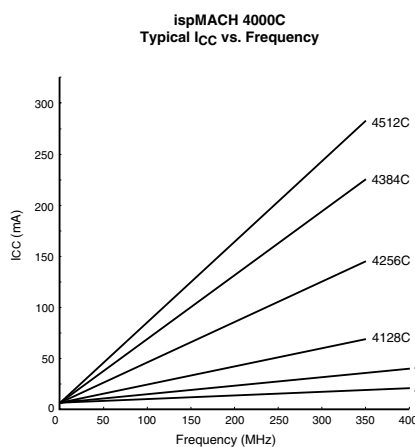
Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t _{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t _{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t _{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t _{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t _{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t _{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t _{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t _{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t _{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t _S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t _{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t _H	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t _{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t _{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t _{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t _{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t _{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

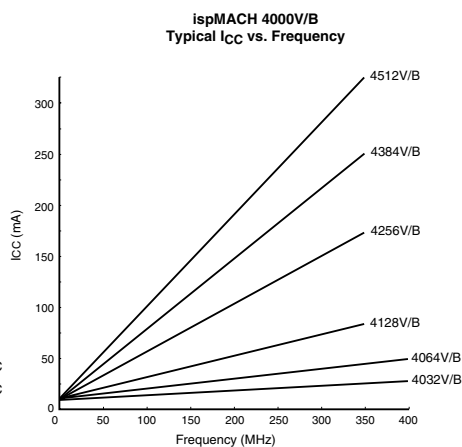
Power Consumption



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 3.3V, 2.5V, 25°C.

Power Estimation Coefficients¹

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC	0.010	0.010
ispMACH 4064ZC	0.011	0.010
ispMACH 4128ZC	0.012	0.010
ispMACH 4256ZC	0.013	0.010

1. For further information about the use of these coefficients, refer to TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#).

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:
44-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A ²	A4	A ²
43	0	A3	A ³	A6	A ³
44	0	A4	A ⁴	A8	A ⁴

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-	TDI	-
2	0	A5	A ⁵	A10	A ⁵	A8	A ⁵
3	0	A6	A ⁶	A12	A ⁶	A10	A ⁶
4	0	A7	A ⁷	A14	A ⁷	A11	A ⁷
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A ⁸	B0	B ⁰	B15	B ⁷
8	0	A9	A ⁹	B2	B ¹	B12	B ⁶
9	0	A10	A ¹⁰	B4	B ²	B10	B ⁵
10	0	A11	A ¹¹	B6	B ³	B8	B ⁴
11	-	TCK	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-	VCC	-
13	-	GND	-	GND	-	GND	-
14	0	A12	A ¹²	B8	B ⁴	B6	B ³
15	0	A13	A ¹³	B10	B ⁵	B4	B ²
16	0	A14	A ¹⁴	B12	B ⁶	B2	B ¹
17	0	A15	A ¹⁵	B14	B ⁷	B0	B ⁰
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
20	1	B0	B ⁰	C0	C ⁰	C0	C ⁰
21	1	B1	B ¹	C2	C ¹	C1	C ¹
22	1	B2	B ²	C4	C ²	C2	C ²
23	1	B3	B ³	C6	C ³	C4	C ³
24	1	B4	B ⁴	C8	C ⁴	C6	C ⁴
25	-	TMS	-	TMS	-	TMS	-
26	1	B5	B ⁵	C10	C ⁵	C8	C ⁵
27	1	B6	B ⁶	C12	C ⁶	C10	C ⁶
28	1	B7	B ⁷	C14	C ⁷	C11	C ⁷
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B ⁸	D0	D ⁰	D15	D ⁷
32	1	B9	B ⁹	D2	D ¹	D12	D ⁶

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
D13	1	D10	D [^] 10	G4	G [^] 3	N6	N [^] 3
D14	1	D9	D [^] 9	G2	G [^] 2	N8	N [^] 4
D12	1	D8	D [^] 8	G1	G [^] 1	N10	N [^] 5
C14	1	I	-	G0	G [^] 0	N12	N [^] 6
C13	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B14	-	TDO	-	TDO	-	TDO	-
A14	-	VCC	-	VCC	-	VCC	-
A13	-	GND	-	GND	-	GND	-
B13	1	NC	-	H14	H [^] 11	O12	O [^] 6
A12	1	I	-	H13	H [^] 10	O10	O [^] 5
C12	1	D7	D [^] 7	H12	H [^] 9	O8	O [^] 4
B12	1	D6	D [^] 6	H10	H [^] 8	O6	O [^] 3
A11	1	D5	D [^] 5	H9	H [^] 7	O4	O [^] 2
C11	1	D4	D [^] 4	H8	H [^] 6	O2	O [^] 1
B11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B10	1	NC	-	H6	H [^] 5	P12	P [^] 6
C10	1	NC	-	H5	H [^] 4	P10	P [^] 5
B9	1	D3	D [^] 3	H4	H [^] 3	P8	P [^] 4
A9	1	D2	D [^] 2	H2	H [^] 2	P6	P [^] 3
C9	1	D1	D [^] 1	H1	H [^] 1	P4	P [^] 2
A8	1	D0/GOE1	D [^] 0	H0/GOE1	H [^] 0	P2/GOE1	P [^] 1
B8	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
C8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
B7	-	VCC	-	VCC	-	VCC	-
A7	0	NC ¹	-	NC ¹	-	I ¹	-
C7	0	A0/GOE0	A [^] 0	A0/GOE0	A [^] 0	A2/GOE0	A [^] 1
A6	0	A1	A [^] 1	A1	A [^] 1	A4	A [^] 2
B6	0	A2	A [^] 2	A2	A [^] 2	A6	A [^] 3
C6	0	A3	A [^] 3	A4	A [^] 3	A8	A [^] 4
B5	0	NC	-	A5	A [^] 4	A10	A [^] 5
A5	0	NC	-	A6	A [^] 5	A12	A [^] 6
C5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
A4	0	NC	-	A8	A [^] 6	B2	B [^] 1
C4	0	A4	A [^] 4	A9	A [^] 7	B4	B [^] 2
A3	0	A5	A [^] 5	A10	A [^] 8	B6	B [^] 3
B3	0	A6	A [^] 6	A12	A [^] 9	B8	B [^] 4
A2	0	A7	A [^] 7	A13	A [^] 10	B10	B [^] 5
A1	0	NC	-	A14	A [^] 11	B12	B [^] 6

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F ⁹	L8	L ⁴
87	1	F13	F ¹⁰	L6	L ³
88	1	F14	F ¹¹	L4	L ²
89	1	NC ²	-	I ²	-
90	1	GND (Bank 1) ¹	-	NC ¹	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC ²	-	I ²	-
93	1	G14	G ¹¹	M2	M ¹
94	1	G13	G ¹⁰	M4	M ²
95	1	G12	G ⁹	M6	M ³
96	1	G10	G ⁸	M8	M ⁴
97	1	G9	G ⁷	M10	M ⁵
98	1	G8	G ⁶	M12	M ⁶
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G ⁵	N2	N ¹
101	1	G5	G ⁴	N4	N ²
102	1	G4	G ³	N6	N ³
103	1	G2	G ²	N8	N ⁴
104	1	G1	G ¹	N10	N ⁵
105	1	G0	G ⁰	N12	N ⁶
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC ²	-	I ²	-
111	1	H14	H ¹¹	O12	O ⁶
112	1	H13	H ¹⁰	O10	O ⁵
113	1	H12	H ⁹	O8	O ⁴
114	1	H10	H ⁸	O6	O ³
115	1	H9	H ⁷	O4	O ²
116	1	H8	H ⁶	O2	O ¹
117	1	NC ²	-	I ²	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H ⁵	P12	P ⁶
121	1	H5	H ⁴	P10	P ⁵
122	1	H4	H ³	P8	P ⁴
123	1	H2	H ²	P6	P ³
124	1	H1	H ¹	P4	P ²
125	1	H0/GOE1	H ⁰	P2/GOE1	P ¹
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M ¹	M1	M ¹	DX2	DX ¹	JX2	JX ¹
H14	1	M4	M ²	M2	M ²	DX4	DX ²	JX4	JX ²
H13	1	M6	M ³	M4	M ³	DX6	DX ³	JX6	JX ³
G16	1	M8	M ⁴	M6	M ⁴	DX8	DX ⁴	JX8	JX ⁴
H12	1	M10	M ⁵	M8	M ⁵	DX10	DX ⁵	JX10	JX ⁵
G15	1	M12	M ⁶	M9	M ⁶	DX12	DX ⁶	JX12	JX ⁶
H11	1	M14	M ⁷	M10	M ⁷	DX14	DX ⁷	JX14	JX ⁷
F16	1	NC	-	M12	M ⁸	CX0	CX ⁰	IX0	IX ⁰
G13	1	NC	-	M14	M ⁹	CX2	CX ¹	IX4	IX ¹
G14	1	NC	-	NC	-	EX14	EX ⁷	KX0	KX ⁰
F15	1	NC	-	NC	-	EX12	EX ⁶	KX2	KX ¹
E16	1	NC	-	NC	-	NC	-	KX4	KX ²
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX ³
G12	1	NC	-	NC	-	EX10	EX ⁵	KX8	KX ⁴
E13	1	NC	-	NC	-	EX8	EX ⁴	KX10	KX ⁵
D16	1	NC	-	N0	N ⁰	CX4	CX ²	IX8	IX ²
E14	1	NC	-	N1	N ¹	CX6	CX ³	IX12	IX ³
G11	1	N0	N ⁰	N2	N ²	FX0	FX ⁰	NX0	NX ⁰
D15	1	N2	N ¹	N4	N ³	FX2	FX ¹	NX2	NX ¹
F11	1	N4	N ²	N6	N ⁴	FX4	FX ²	NX4	NX ²
C16	1	N6	N ³	N8	N ⁵	FX6	FX ³	NX6	NX ³
F12	1	N8	N ⁴	N9	N ⁶	FX8	FX ⁴	NX8	NX ⁴
D14	1	N10	N ⁵	N10	N ⁷	FX10	FX ⁵	NX10	NX ⁵
C15	1	N12	N ⁶	N12	N ⁸	FX12	FX ⁶	NX12	NX ⁶
B16	1	N14	N ⁷	N14	N ⁹	FX14	FX ⁷	NX14	NX ⁷
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX ³	KX12	KX ⁶
B14	1	NC	-	NC	-	EX4	EX ²	KX14	KX ⁷
E12	1	O14	O ⁷	O14	O ⁹	GX14	GX ⁷	OX14	OX ⁷
A14	1	O12	O ⁶	O12	O ⁸	GX12	GX ⁶	OX12	OX ⁶
C13	1	O10	O ⁵	O10	O ⁷	GX10	GX ⁵	OX10	OX ⁵
D13	1	O8	O ⁴	O9	O ⁶	GX8	GX ⁴	OX8	OX ⁴
E11	1	O6	O ³	O8	O ⁵	GX6	GX ³	OX6	OX ³
B13	1	O4	O ²	O6	O ⁴	GX4	GX ²	OX4	OX ²
F10	1	O2	O ¹	O4	O ³	GX2	GX ¹	OX2	OX ¹

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B ¹	F8	F ⁴	D12	D ³
A3	0	B0	B ⁰	B2	B ²	B0	B ⁰	B0	B ⁰
F7	0	B2	B ¹	B4	B ³	B2	B ¹	B2	B ¹
B4	0	B4	B ²	B6	B ⁴	B4	B ²	B4	B ²
C5	0	B6	B ³	B8	B ⁵	B6	B ³	B6	B ³
A2	0	B8	B ⁴	B9	B ⁶	B8	B ⁴	B8	B ⁴
E6	0	B10	B ⁵	B10	B ⁷	B10	B ⁵	B10	B ⁵
B3	0	B12	B ⁶	B12	B ⁸	B12	B ⁶	B12	B ⁶
C4	0	B14	B ⁷	B14	B ⁹	B14	B ⁷	B14	B ⁷
D4	0	NC	-	NC	-	D10	D ⁵	F0	F ⁰
E5	0	NC	-	NC	-	D8	D ⁴	F2	F ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

ispMACH 4000V (3.3V) Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75T48E	32	3.3	7.5	TQFP	48	32	E
	LC4032V-75T44E	32	3.3	7.5	TQFP	44	30	E
LC4064V	LC4064V-75T100E	64	3.3	7.5	TQFP	100	64	E
	LC4064V-75T48E	64	3.3	7.5	TQFP	48	32	E
	LC4064V-75T44E	64	3.3	7.5	TQFP	44	30	E
LC4128V	LC4128V-75T144E	128	3.3	7.5	TQFP	144	96	E
	LC4128V-75T128E	128	3.3	7.5	TQFP	128	92	E
	LC4128V-75T100E	128	3.3	7.5	TQFP	100	64	E
LC4256V	LC4256V-75T176E	256	3.3	7.5	TQFP	176	128	E
	LC4256V-75T144E	256	3.3	7.5	TQFP	144	96	E
	LC4256V-75T100E	256	3.3	7.5	TQFP	100	64	E

Lead-Free Packaging**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices**

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
	LC4064B-75TN44C	64	2.5	7.5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC ¹	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC ¹	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC ¹	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC ¹	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC ¹	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC ¹	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
	LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C
	LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C

ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C ¹	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C ¹	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
	LC4384B-75TN176C	384	2.5	7.5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C ¹	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C ¹	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 μ A to -200 μ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.