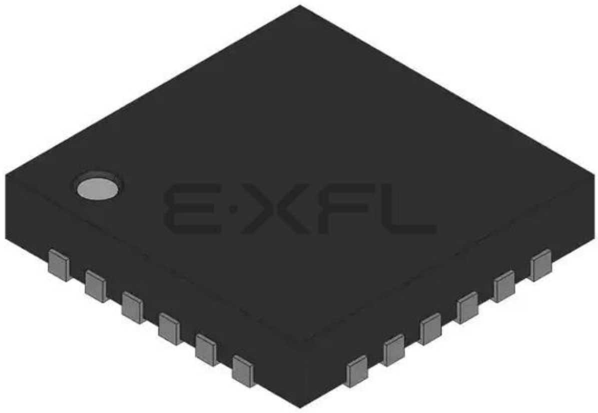

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 12x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VFQFN Exposed Pad |
| Supplier Device Package | 24-QFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl05z16vfk4 |

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PKL05 and MKL05

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KL## | Kinetis family | • KL05 |
| A | Key attribute | • Z = Cortex-M0+ |
| FFF | Program flash memory size | • 8 = 8 KB<br>• 16 = 16 KB<br>• 32 = 32 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |

*Table continues on the next page...*

## 4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{DIO}$ | Digital pin input voltage (except $\overline{\text{RESET}}$) | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{AIO}$ | Analog pins[1] and $\overline{\text{RESET}}$ pin input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

**Table 1. Voltage and current operating requirements (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $I_{ICIO}$ | I/O pin DC injection current — single pin<br>• $V_{IN} < V_{SS}$-0.3V (Negative current injection)<br>• $V_{IN} > V_{DD}$+0.3V (Positive current injection) | <br>-3<br>— | <br>—<br>+3 | mA | 1 |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins<br>• Negative current injection<br>• Positive current injection | <br>-25<br>— | <br>—<br>+25 | mA | |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |

1. All analog pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is greater than $V_{AIO\_MIN}$ (=$V_{SS}$-0.3V) and $V_{IN}$ is less than $V_{AIO\_MAX}$(=$V_{DD}$+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{AIO\_MIN}$-$V_{IN}$)/|$I_{IC}$|. The positive injection current limiting resistor is calcualted as R=($V_{IN}$-$V_{AIO\_MAX}$)/|$I_{IC}$|. Select the larger of these two calculated resistances.

### 5.2.2 LVD and POR operating requirements

**Table 2. $V_{DD}$ supply LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling $V_{DD}$ POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | |

*Table continues on the next page...*

## Table 5. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_RUN}$ | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash<br>• at 3.0 V<br>  • at 25 °C<br>  • at 125 °C | <br><br>—<br>— | <br><br>5.6<br>6 | <br><br>6.8<br>7.2 | <br><br>mA<br>mA | 2, 3 |
| $I_{DD\_WAIT}$ | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 3.0 | 4.2 | mA | 2 |
| $I_{DD\_WAIT}$ | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 2.4 | 3.36 | mA | 2 |
| $I_{DD\_PSTOP2}$ | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus<br>• at 3.0 V | — | 2.25 | 3.38 | mA | 2 |
| $I_{DD\_VLPRCO}$ | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 182 | 522 | µA | 4 |
| $I_{DD\_VLPR}$ | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 213.33 | 577.8 | µA | 4 |
| $I_{DD\_VLPR}$ | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 242.8 | 631.8 | µA | 3, 4 |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 106.1 | 399.42 | µA | 4 |

*Table continues on the next page...*

## Table 5. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLLS0}$ | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0)<br>• at 3.0 V<br>• at 25 °C<br>• at 50 °C<br>• at 70 °C<br>• at 85 °C<br>• at 105 °C | —<br>—<br>—<br>—<br>— | 449.6<br>1200<br>2900<br>5900<br>14800 | 959.2<br>12155.08<br>15323.29<br>16384.55<br>26773.45 | nA | |
| $I_{DD\_VLLS0}$ | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1)<br>• at 3.0 V<br>• at 25 °C<br>• at 50 °C<br>• at 70 °C<br>• at 85 °C<br>• at 105 °C | —<br>—<br>—<br>—<br>— | 221.7<br>1000<br>2600<br>5600<br>14400 | 894.24<br>3784.55<br>12018.39<br>18722.23<br>24665.06 | nA | 5 |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode.
3. Incremental current consumption from peripheral activity is not included.
4. MCG configured for BLPI mode.
5. No brownout

## Table 6. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{IREFSTEN4MHz}$ | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | µA |
| $I_{IREFSTEN32KHz}$ | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | µA |
| $I_{EREFSTEN4MHz}$ | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |

*Table continues on the next page...*

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz | |
| $f_{BUS}$ | Bus clock | — | 24 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz | |
| VLPR mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 1 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |
| $f_{LPTMR\_pin}$ | LPTMR clock | — | 24 | MHz | |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz | |
| $f_{TPM}$ | TPM asynchronous clock | — | 8 | MHz | |
| $f_{UART0}$ | UART0 asynchronous clock | — | 8 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and $I^2C$ signals.

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| | External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| | GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| | Port rise and fall time | — | 36 | ns | 3 |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shrtest pulse that is guaranteed to be recognized.
3. 75 pF load

# 5.4 Thermal specifications

## 5.4.1 Thermal operating requirements

**Table 8. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |

## 5.4.2 Thermal attributes

**Table 9. Thermal attributes**

| Board type | Symbol | Description | 48 LQFP | 32 LQFP | 32 QFN | 24 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 82 | 88 | 97 | 110 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 58 | 59 | 34 | 42 | °C/W | |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 70 | 74 | 81 | 92 | °C/W | |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 52 | 52 | 28 | 36 | °C/W | |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 36 | 35 | 13 | 18 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 27 | 26 | 2.3 | 3.7 | °C/W | 3 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 8 | 8 | 8 | 10 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.

**Table 12. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 13. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

#### 6.4.1.3 Flash high voltage current behaviors

**Table 16. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

#### 6.4.1.4 Reliability specifications

**Table 17. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ $T_j$ ≤ 125°C.

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

### 6.6.1.1 12-bit ADC operating conditions

**Table 18. 12-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$ - $V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$ - $V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | 3 |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | 3 |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $C_{ADIN}$ | Input capacitance | • 8-/10-/12-bit modes | — | 4 | 5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 12-bit mode | 1.0 | — | 18.0 | MHz | 5 |
| $C_{rate}$ | ADC conversion rate | ≤ 12 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 6 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins, $V_{REFH}$ is internally tied to $V_{DDA}$, and $V_{REFL}$ is internally tied to $V_{SSA}$.
4. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1ns.
5. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
6. For guidelines and examples of conversion rate calculation, download the ADC calculator tool

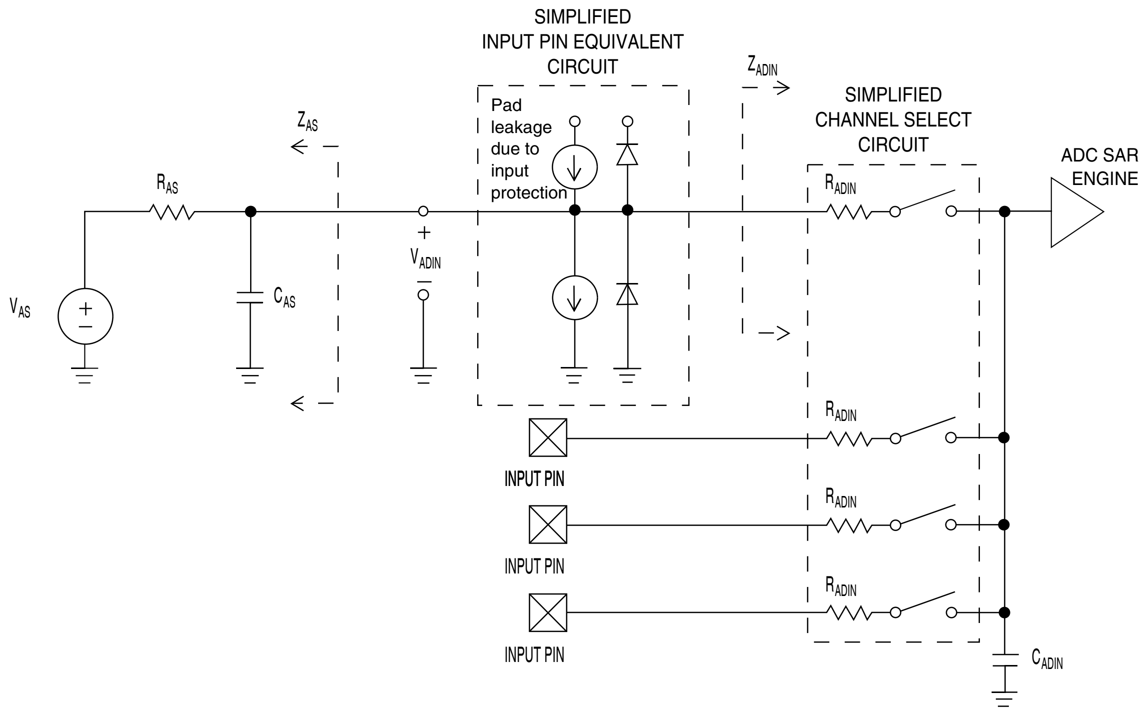


**Figure 6. ADC input impedance equivalency diagram**

### 6.6.1.2 12-bit ADC electrical characteristics

**Table 19. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0<br>• ADLPC = 1, ADHSC = 1<br>• ADLPC = 0, ADHSC = 0<br>• ADLPC = 0, ADHSC = 1 | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes<br>• <12-bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±0.7<br>±0.2 | -1.1 to +1.9<br>-0.3 to 0.5 | LSB[4] | 5 |
| INL | Integral non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±1.0<br>±0.5 | -2.7 to +1.9<br>-0.7 to +0.5 | LSB[4] | 5 |
| $E_{FS}$ | Full-scale error | • 12-bit modes<br>• <12-bit modes | —<br>— | -4<br>-1.4 | -5.4<br>-1.8 | LSB[4] | $V_{ADIN} = V_{DDA}$<br>5 |

*Table continues on the next page...*

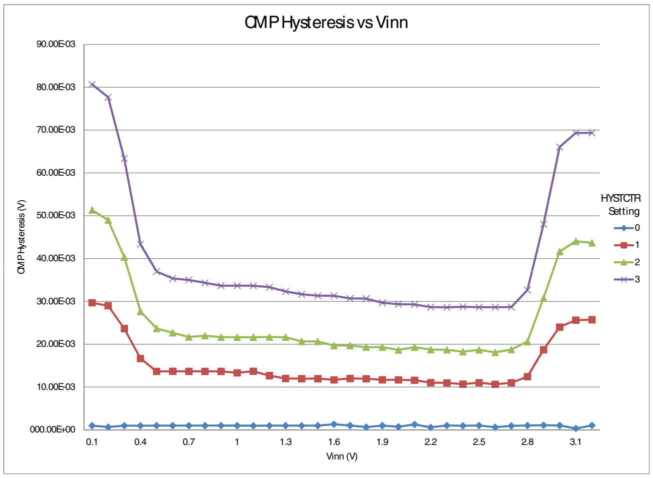


**Figure 8. Typical hysteresis vs. Vin level ($V_{DD}$ = 3.3 V, PMODE = 0)**

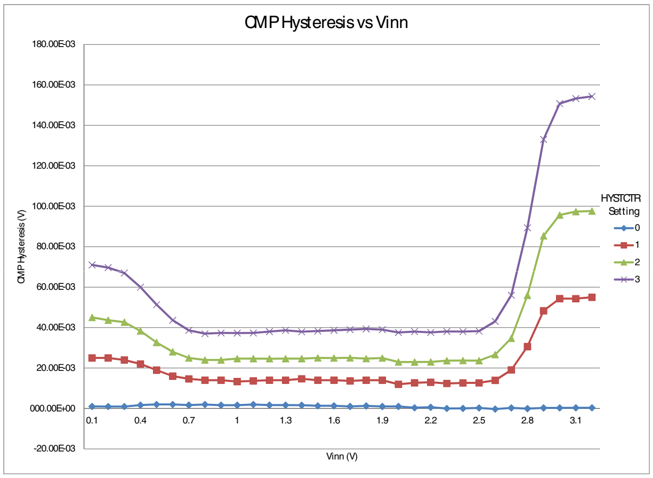


**Figure 9. Typical hysteresis vs. Vin level ($V_{DD}$ = 3.3 V, PMODE = 1)**

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

**Table 21. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $T_A$ | Temperature | Operating temperature range of the device | | °C | |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

**Table 22. 12-bit DAC operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 250 | μA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 900 | μA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | μs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4$ V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | μV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance load = 3 kΩ | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/μs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

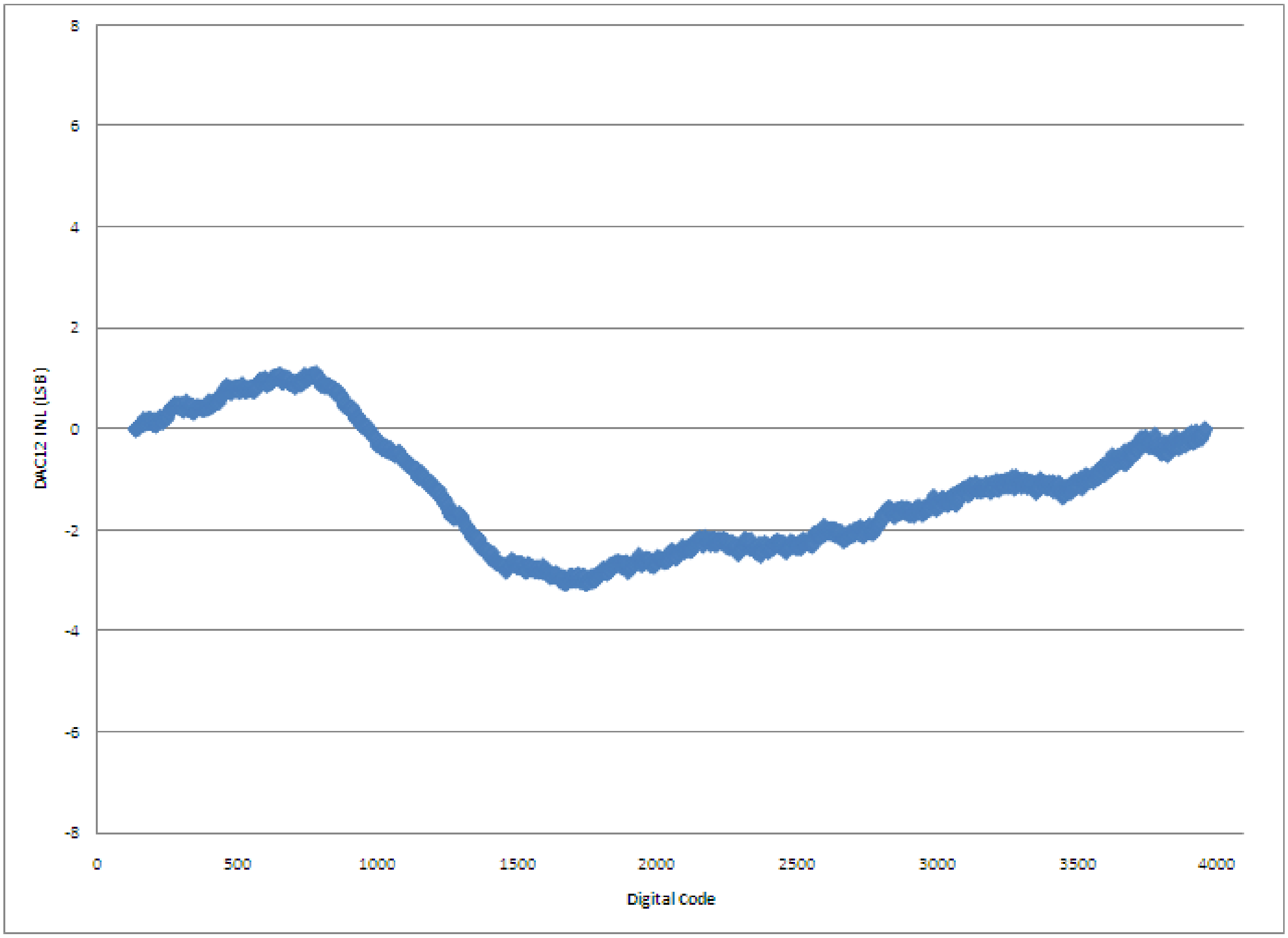


**Figure 10. Typical INL error vs. digital code**

## Table 25. SPI slave mode timing on slew rate disabled pads (continued)

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 6 | $t_{SU}$ | Data setup time (inputs) | 2 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 7 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 22 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

## Table 26. SPI slave mode timing on slew rate enabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 7 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 36 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0 $f_{periph}$ is the bus clock ($f_{BUS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

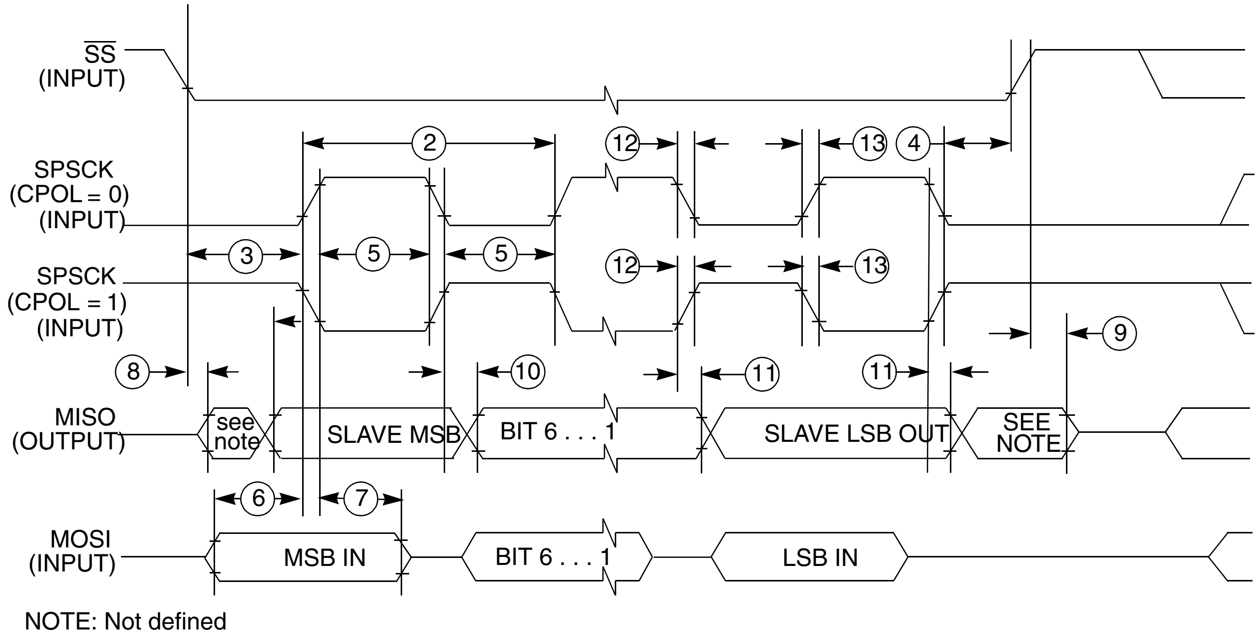


**Figure 14. SPI slave mode timing (CPHA = 0)**

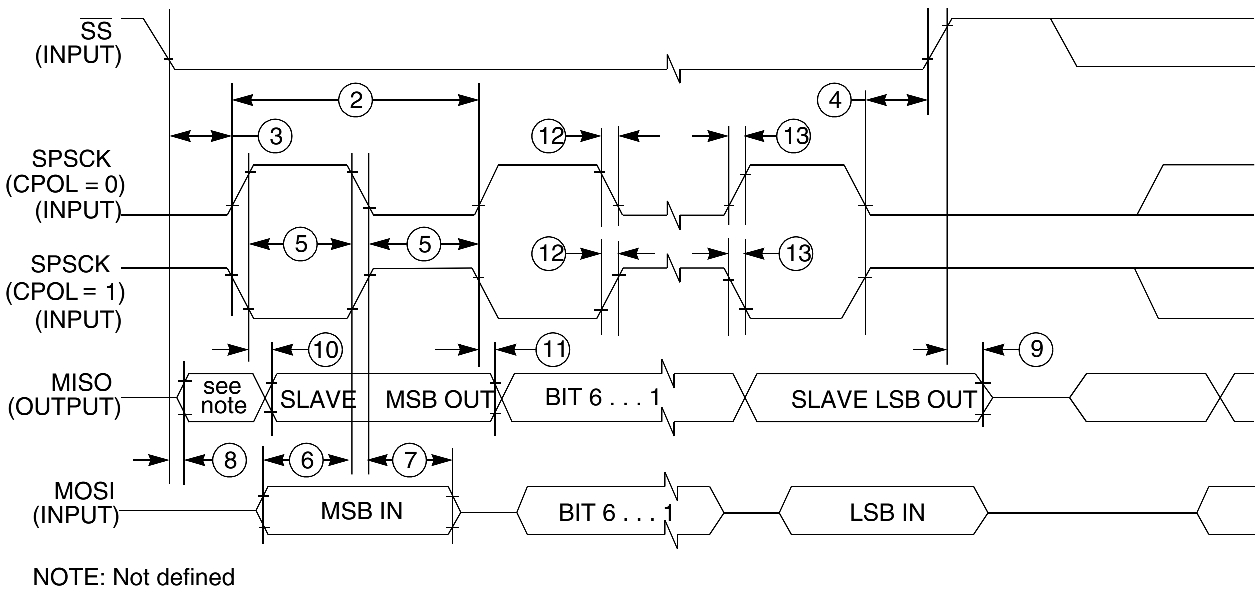


**Figure 15. SPI slave mode timing (CPHA = 1)**

## 6.8.2 I²C

See General switching specifications.

## 6.8.3 UART

See General switching specifications.

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

**Table 27. TSI electrical specifications**

| Symbol | Description | Min. | Type | Max | Unit |
|---|---|---|---|---|---|
| TSI_RUNF | Fixed power consumption in run mode | — | 100 | — | µA |
| TSI_RUNV | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0 | — | 128 | µA |
| TSI_EN | Power consumption in enable mode | — | 100 | — | µA |
| TSI_DIS | Power consumption in disable mode | — | 1.2 | — | µA |
| TSI_TEN | TSI analog enable time | — | 66 | — | µs |
| TSI_CREF | TSI reference capacitor | — | 1.0 | — | pF |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values | 0.19 | — | 1.03 | V |

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 24-pin QFN | 98ASA00474D |
| 32-pin QFN | 98ASA00473D |
| 32-pin LQFP | 98ASH70029A |
| 48-pin LQFP | 98ASH00962A |

# 8 Pinout

## 8.1 KL05 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | PTB6/ IRQ_2/ LPTMR0_ALT3 | DISABLED | DISABLED | PTB6/ IRQ_2/ LPTMR0_ALT3 | TPM0_CH3 | TPM_CLKIN1 |
| 2 | 2 | 2 | 2 | PTB7/ IRQ_3 | DISABLED | DISABLED | PTB7/ IRQ_3 | TPM0_CH2 | |
| 3 | — | — | — | PTA14 | DISABLED | DISABLED | PTA14 | | TPM_CLKIN0 |
| 4 | — | — | — | PTA15 | DISABLED | DISABLED | PTA15 | | CLKOUT |
| 5 | 3 | 3 | 3 | VDD | VDD | VDD | | | |
| 6 | 4 | 4 | 3 | VREFH | VREFH | VREFH | | | |
| 7 | 5 | 5 | 4 | VREFL | VREFL | VREFL | | | |
| 8 | 6 | 6 | 4 | VSS | VSS | VSS | | | |
| 9 | 7 | 7 | 5 | PTA3 | EXTAL0 | EXTAL0 | PTA3 | I2C0_SCL | I2C0_SDA |
| 10 | 8 | 8 | 6 | PTA4/ LLWU_P0 | XTAL0 | XTAL0 | PTA4/ LLWU_P0 | I2C0_SDA | I2C0_SCL |
| 11 | — | — | — | VSS | VSS | VSS | | | |
| 12 | — | — | — | PTB18 | DISABLED | DISABLED | PTB18 | | |
| 13 | — | — | — | PTB19 | DISABLED | DISABLED | PTB19 | | |
| 14 | 9 | 9 | 7 | PTA5/ LLWU_P1/ RTC_CLK_IN | DISABLED | DISABLED | PTA5/ LLWU_P1/ RTC_CLK_IN | TPM0_CH5 | SPI0_SS_b |
| 15 | 10 | 10 | 8 | PTA6/ LLWU_P2 | DISABLED | DISABLED | PTA6/ LLWU_P2 | TPM0_CH4 | SPI0_MISO |
| 16 | 11 | 11 | — | PTB8 | ADC0_SE11 | ADC0_SE11 | PTB8 | TPM0_CH3 | |
| 17 | 12 | 12 | — | PTB9 | ADC0_SE10 | ADC0_SE10 | PTB9 | TPM0_CH2 | |
| 18 | — | — | — | PTA16/ IRQ_4 | DISABLED | DISABLED | PTA16/ IRQ_4 | | |
| 19 | — | — | — | PTA17/ IRQ_5 | DISABLED | DISABLED | PTA17/ IRQ_5 | | |
| 20 | — | — | — | PTA18/ IRQ_6 | DISABLED | DISABLED | PTA18/ IRQ_6 | | |
| 21 | 13 | 13 | 9 | PTB10 | ADC0_SE9/ TSI0_IN7 | ADC0_SE9/ TSI0_IN7 | PTB10 | TPM0_CH1 | |
| 22 | 14 | 14 | 10 | PTB11 | ADC0_SE8/ TSI0_IN6 | ADC0_SE8/ TSI0_IN6 | PTB11 | TPM0_CH0 | |
| 23 | 15 | 15 | 11 | PTA7/ IRQ_7/ LLWU_P3 | ADC0_SE7/ TSI0_IN5 | ADC0_SE7/ TSI0_IN5 | PTA7/ IRQ_7/ LLWU_P3 | SPI0_MISO | SPI0_MOSI |
| 24 | 16 | 16 | 12 | PTB0/ IRQ_8/ LLWU_P4 | ADC0_SE6/ TSI0_IN4 | ADC0_SE6/ TSI0_IN4 | PTB0/ IRQ_8/ LLWU_P4 | EXTRG_IN | SPI0_SCK |

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 25 | 17 | 17 | 13 | PTB1/ IRQ_9 | ADC0_SE5/ TSI0_IN3/ DAC0_OUT/ CMP0_IN3 | ADC0_SE5/ TSI0_IN3/ DAC0_OUT/ CMP0_IN3 | PTB1/ IRQ_9 | UART0_TX | UART0_RX |
| 26 | 18 | 18 | 14 | PTB2/ IRQ_10/ LLWU_P5 | ADC0_SE4/ TSI0_IN2 | ADC0_SE4/ TSI0_IN2 | PTB2/ IRQ_10/ LLWU_P5 | UART0_RX | UART0_TX |
| 27 | 19 | 19 | 15 | PTA8 | ADC0_SE3/ TSI0_IN1 | ADC0_SE3/ TSI0_IN1 | PTA8 | | |
| 28 | 20 | 20 | 16 | PTA9 | ADC0_SE2/ TSI0_IN0 | ADC0_SE2/ TSI0_IN0 | PTA9 | | |
| 29 | — | — | — | PTB20 | DISABLED | DISABLED | PTB20 | | |
| 30 | — | — | — | VSS | VSS | VSS | | | |
| 31 | — | — | — | VDD | VDD | VDD | | | |
| 32 | — | — | — | PTB14/ IRQ_11 | DISABLED | DISABLED | PTB14/ IRQ_11 | EXTRG_IN | |
| 33 | 21 | 21 | — | PTA10/ IRQ_12 | DISABLED | TSI0_IN11 | PTA10/ IRQ_12 | | |
| 34 | 22 | 22 | — | PTA11/ IRQ_13 | DISABLED | TSI0_IN10 | PTA11/ IRQ_13 | | |
| 35 | 23 | 23 | 17 | PTB3/ IRQ_14 | DISABLED | DISABLED | PTB3/ IRQ_14 | I2C0_SCL | UART0_TX |
| 36 | 24 | 24 | 18 | PTB4/ IRQ_15/ LLWU_P6 | DISABLED | DISABLED | PTB4/ IRQ_15/ LLWU_P6 | I2C0_SDA | UART0_RX |
| 37 | 25 | 25 | 19 | PTB5/ IRQ_16 | NMI_b | ADC0_SE1/ CMP0_IN1 | PTB5/ IRQ_16 | TPM1_CH1 | NMI_b |
| 38 | 26 | 26 | 20 | PTA12/ IRQ_17/ LPTMR0_ALT2 | ADC0_SE0/ CMP0_IN0 | ADC0_SE0/ CMP0_IN0 | PTA12/ IRQ_17/ LPTMR0_ALT2 | TPM1_CH0 | TPM_CLKIN0 |
| 39 | 27 | 27 | — | PTA13 | TSI0_IN9 | TSI0_IN9 | PTA13 | | |
| 40 | 28 | 28 | — | PTB12 | TSI0_IN8 | TSI0_IN8 | PTB12 | | |
| 41 | — | — | — | PTA19 | DISABLED | DISABLED | PTA19 | | SPI0_SS_b |
| 42 | — | — | — | PTB15 | DISABLED | DISABLED | PTB15 | SPI0_MOSI | SPI0_MISO |
| 43 | — | — | — | PTB16 | DISABLED | DISABLED | PTB16 | SPI0_MISO | SPI0_MOSI |
| 44 | — | — | — | PTB17 | DISABLED | DISABLED | PTB17 | TPM_CLKIN1 | SPI0_SCK |
| 45 | 29 | 29 | 21 | PTB13 | ADC0_SE13 | ADC0_SE13 | PTB13 | TPM1_CH1 | RTC_CLKOUT |
| 46 | 30 | 30 | 22 | PTA0/ IRQ_0/ LLWU_P7 | SWD_CLK | ADC0_SE12/ CMP0_IN2 | PTA0/ IRQ_0/ LLWU_P7 | TPM1_CH0 | SWD_CLK |
| 47 | 31 | 31 | 23 | PTA1/ IRQ_1/ LPTMR0_ALT1 | RESET_b | DISABLED | PTA1/ IRQ_1/ LPTMR0_ALT1 | TPM_CLKIN0 | RESET_b |
| 48 | 32 | 32 | 24 | PTA2 | SWD_DIO | DISABLED | PTA2 | CMP0_OUT | SWD_DIO |

## 8.2 KL05 Pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

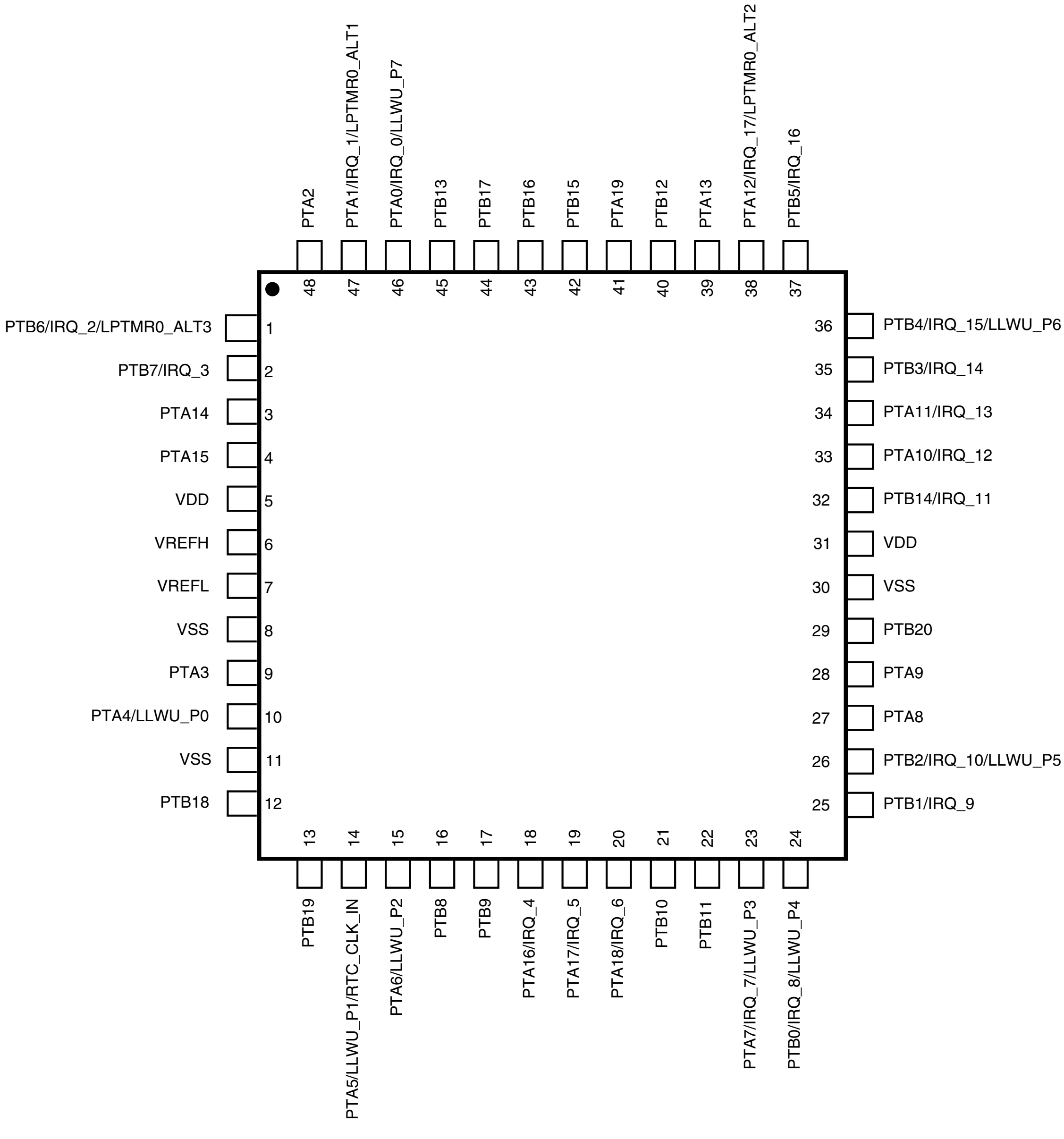


**Figure 16. KL05 48-pin LQFP pinout diagram**