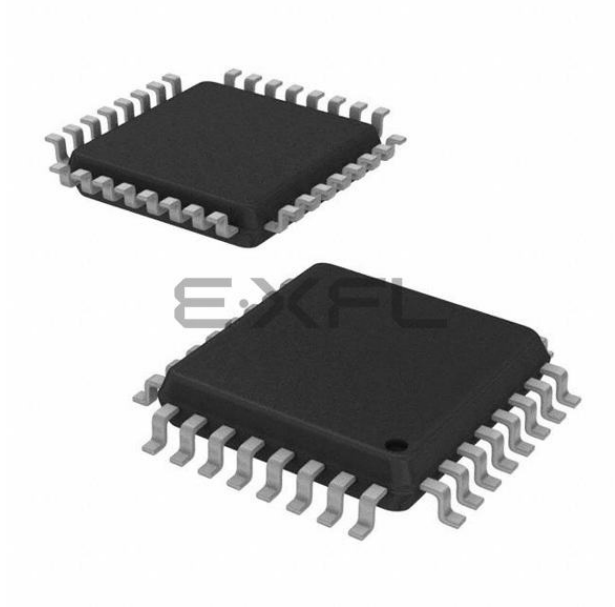

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl05z8vlc4

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICIO}	I/O pin DC injection current — single pin • $V_{IN} < V_{SS}$-0.3V (Negative current injection) • $V_{IN} > V_{DD}$+0.3V (Positive current injection)	 -3 —	 — +3	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} (=V_{SS}-0.3V) and V_{IN} is less than V_{AIO_MAX}(=V_{DD}+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calcualted as $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

5.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -1.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -18 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	0.5	V	
V_{OL}	Output low voltage — High drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	3

1. PTA12, PTA13, PTB0 and PTB1 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V_{DD} = 3.6 V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	95	115	µs	
	• VLLS1 → RUN	—	93	115	µs	
	• VLLS3 → RUN	—	42	53	µs	
	• LLS → RUN	—	4	4.6	µs	
	• VLPS → RUN	—	4	4.4	µs	
	• STOP → RUN	—	4	4.4	µs	

5.2.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V	—	4.1	5.2	mA	2
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V	—	4.9	5.6	mA	2

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_STOP}	Stop mode current • at 3.0 V					
	• at 25 °C	—	273	441		
	• at 50 °C	—	281.2	620	µA	
	• at 70 °C	—	301.6	647.64		
	• at 85 °C	—	331	710.64		
	• at 105 °C	—	406.6	1001.84		
I_{DD_VLPS}	Very-low-power stop mode current • at 3.0 V					
	• at 25 °C	—	3.08	16.01		
	• at 50 °C	—	5.46	34.73	µA	
	• at 70 °C	—	12.08	46.73		
	• at 85 °C	—	22.89	77.37		
	• at 105 °C	—	53.24	190.28		
I_{DD_LLS}	Low-leakage stop mode current • at 3.0 V					
	• at 25 °C	—	1.7	3.69		
	• at 50 °C	—	3	22	µA	
	• at 70 °C	—	5.8	28.19		
	• at 85 °C	—	10.4	40.29		
	• at 105 °C	—	24	65.5		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current • at 3.0 V				µA	
	• at 25 °C	—	1.3	3		
	• at 50 °C	—	2.3	11.04		
	• at 70 °C	—	4.4	13.68		
	• at 85 °C	—	8	20.14		
	• at 105 °C	—	18.6	37.82		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current • at 3.0 V					
	• at 25°C	—	0.78	1.6		
	• at 50°C	—	1.5	13.61	µA	
	• at 70°C	—	3.3	15.59		
	• at 85°C	—	6.3	16.68		
	• at 105°C	—	15.2	26.40		

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

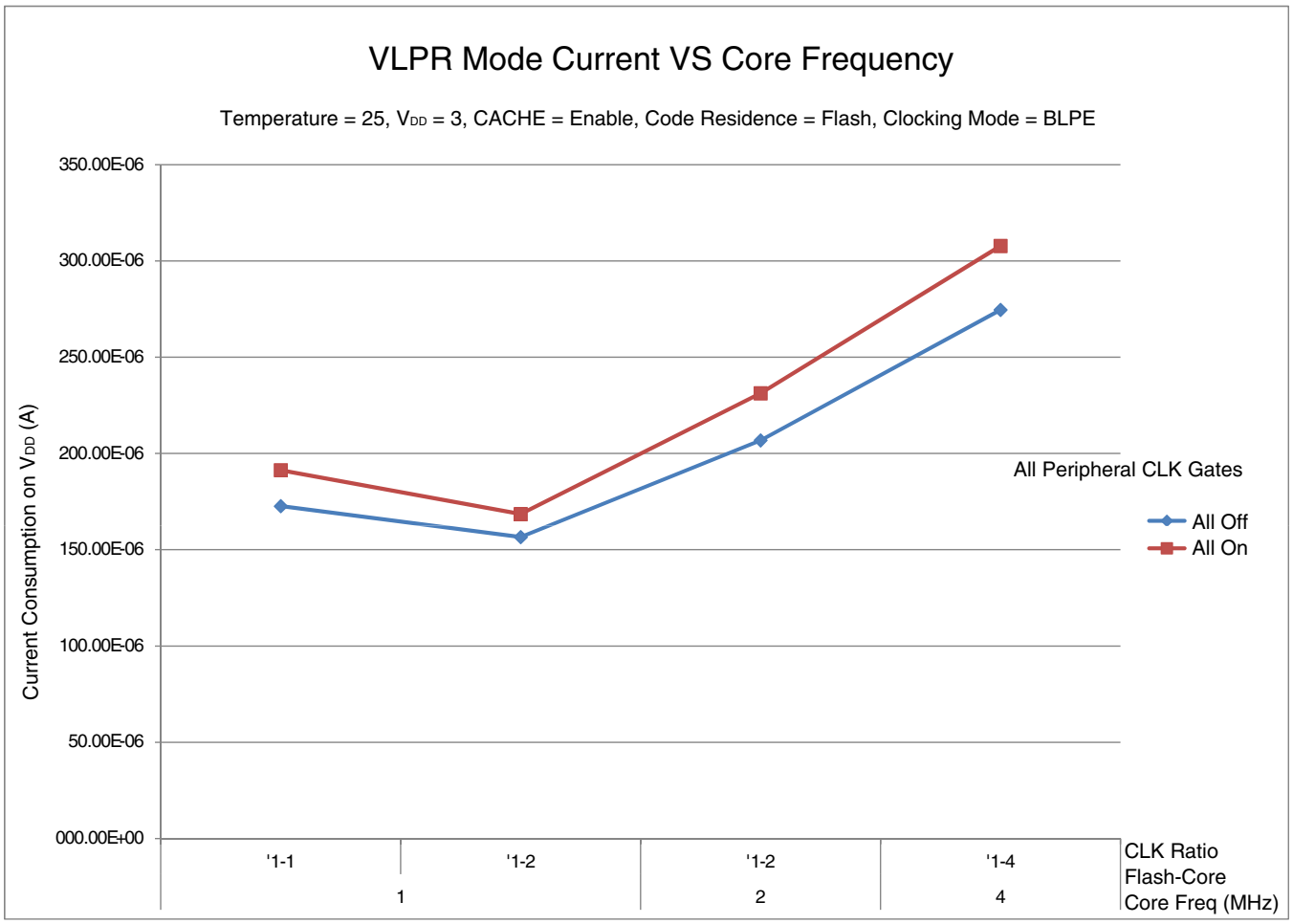


Figure 3. VLPR mode current vs. core frequency

5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

Table 11. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) 1280 × f_{fll_ref}	40	41.94	48	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz		—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

Table 19. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_Q	Quantization error	• 12-bit modes	—	—	±0.5	LSB[4]	
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)

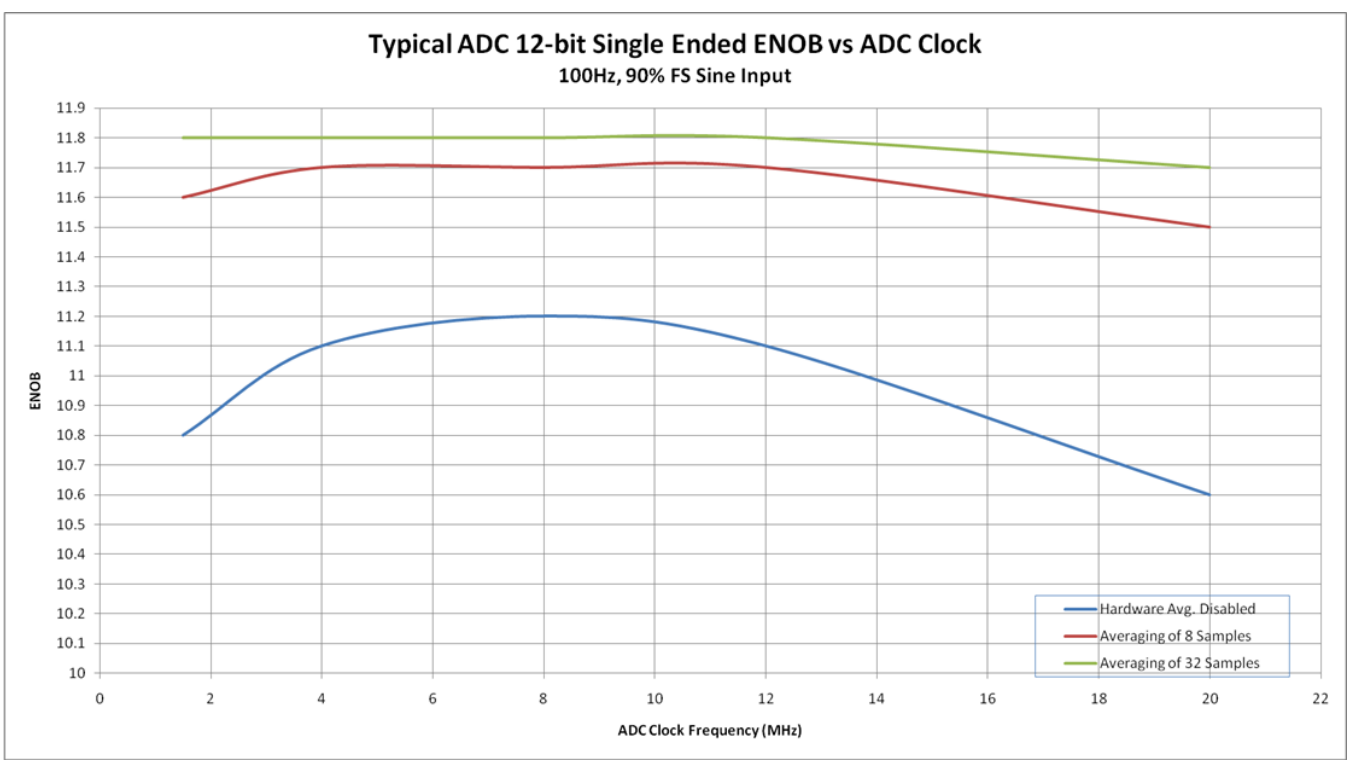


Figure 7. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

6.6.2 CMP and 6-bit DAC electrical specifications

Table 20. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} – 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD} – 0.7$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

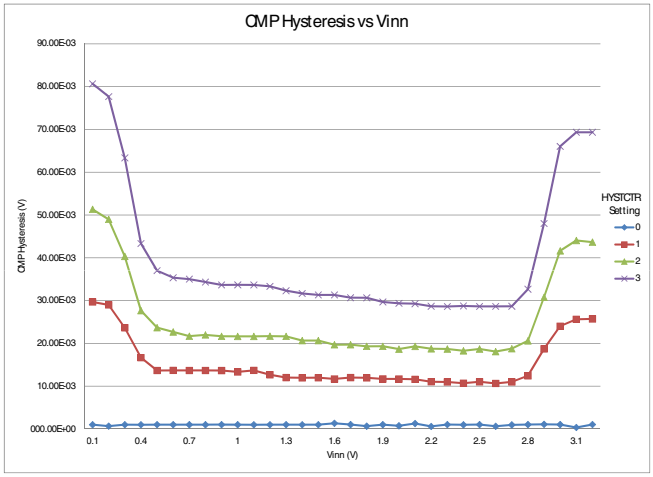


Figure 8. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

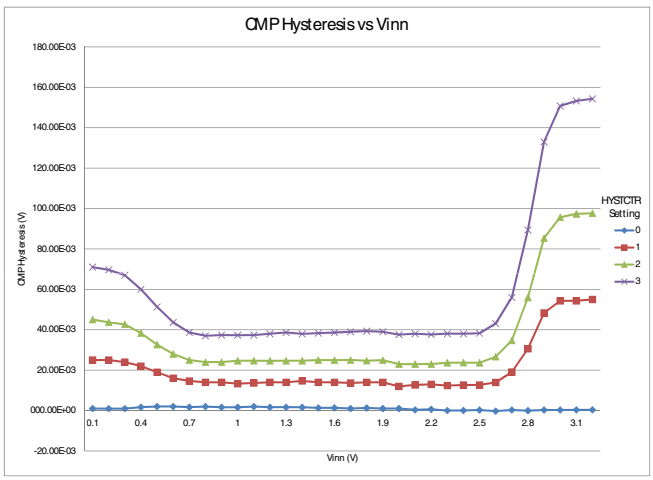


Figure 9. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 21. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

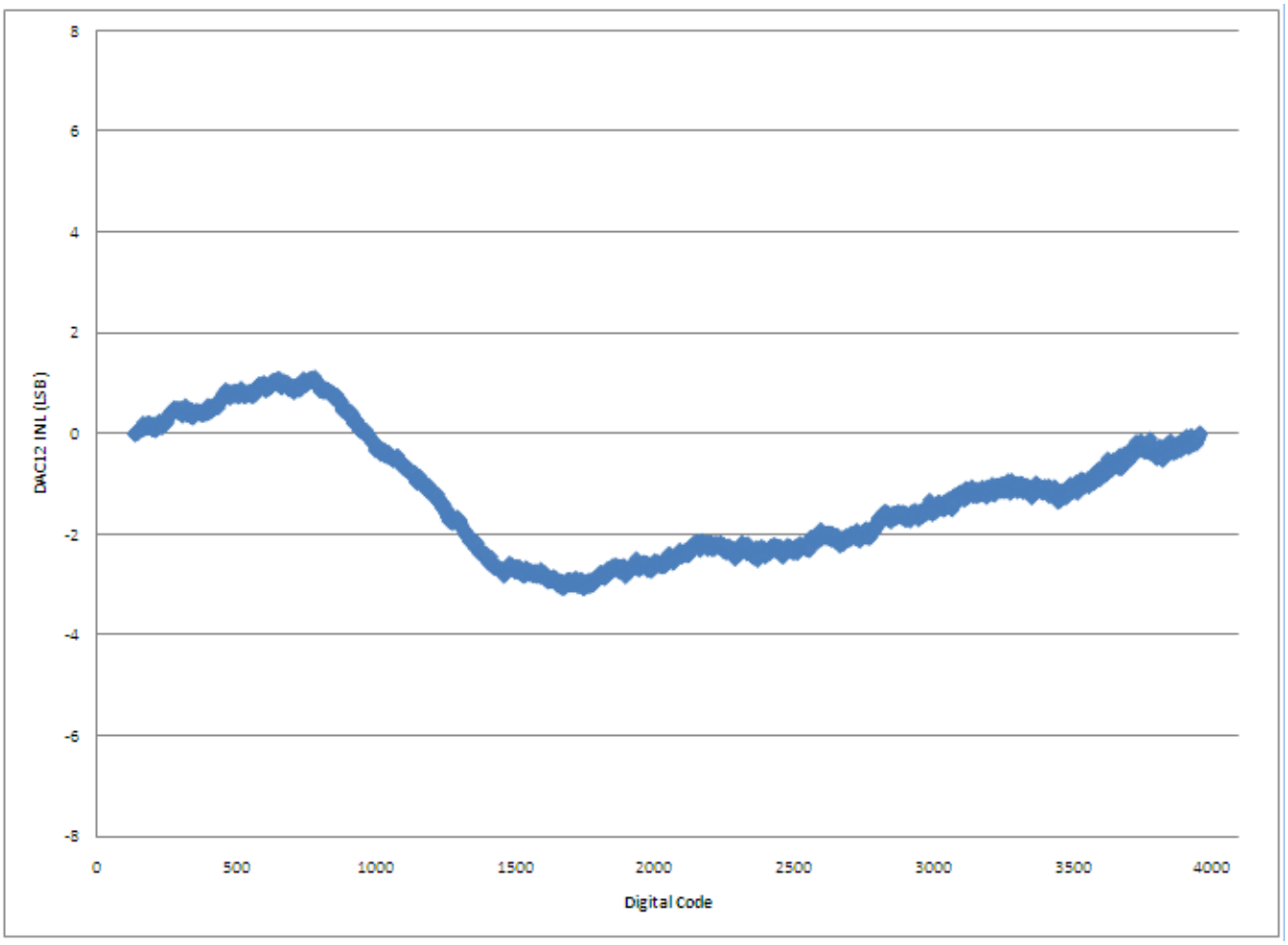


Figure 10. Typical INL error vs. digital code

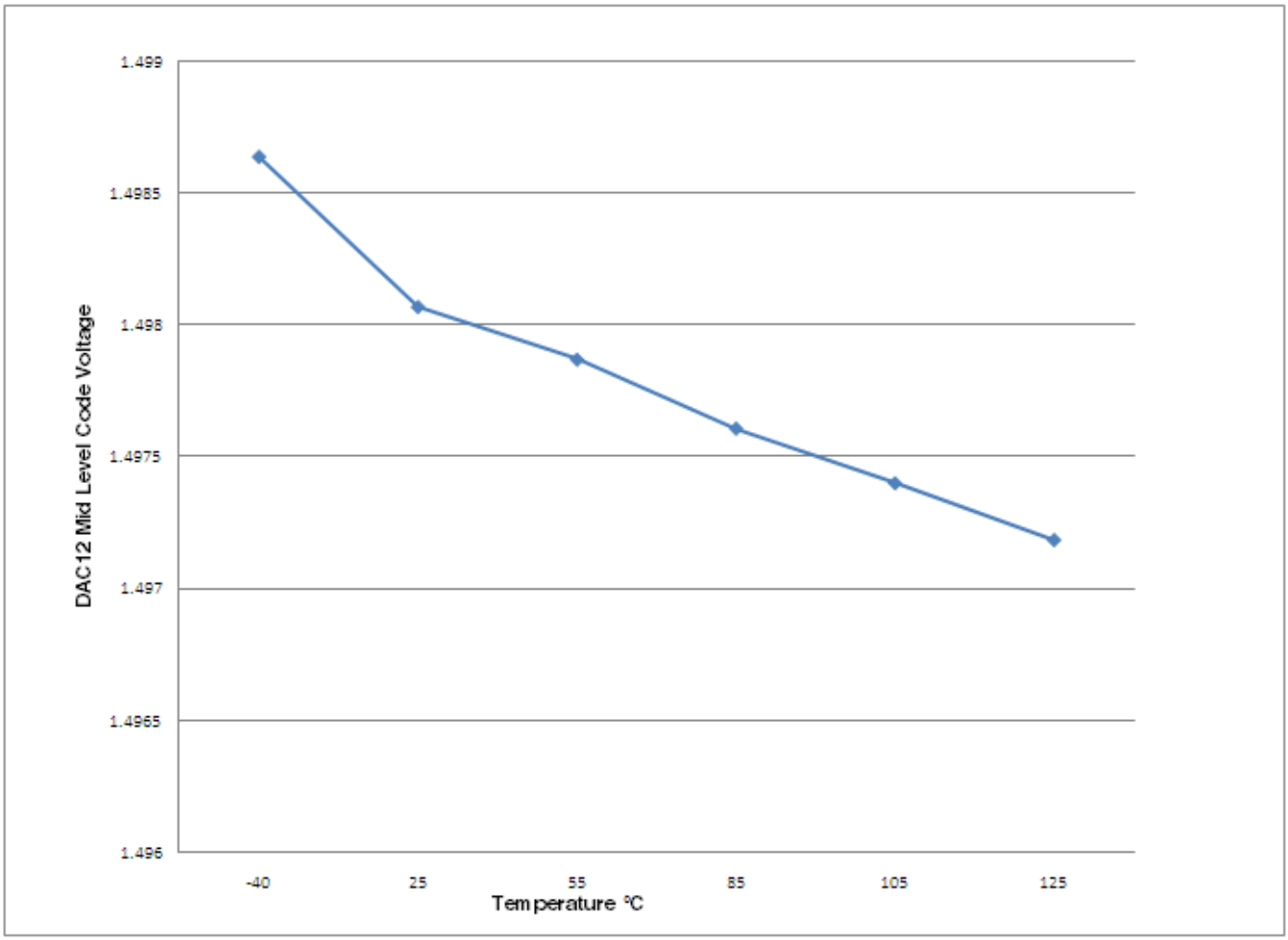


Figure 11. Offset at half scale vs. temperature

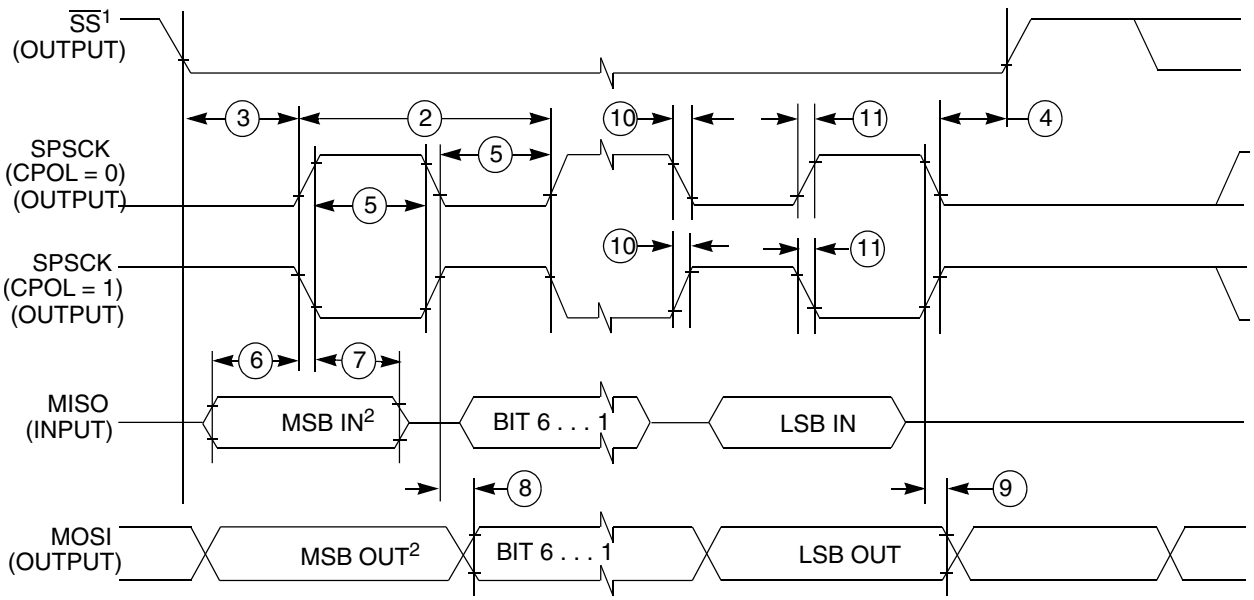
6.7 Timers

See General switching specifications.

6.8 Communication interfaces

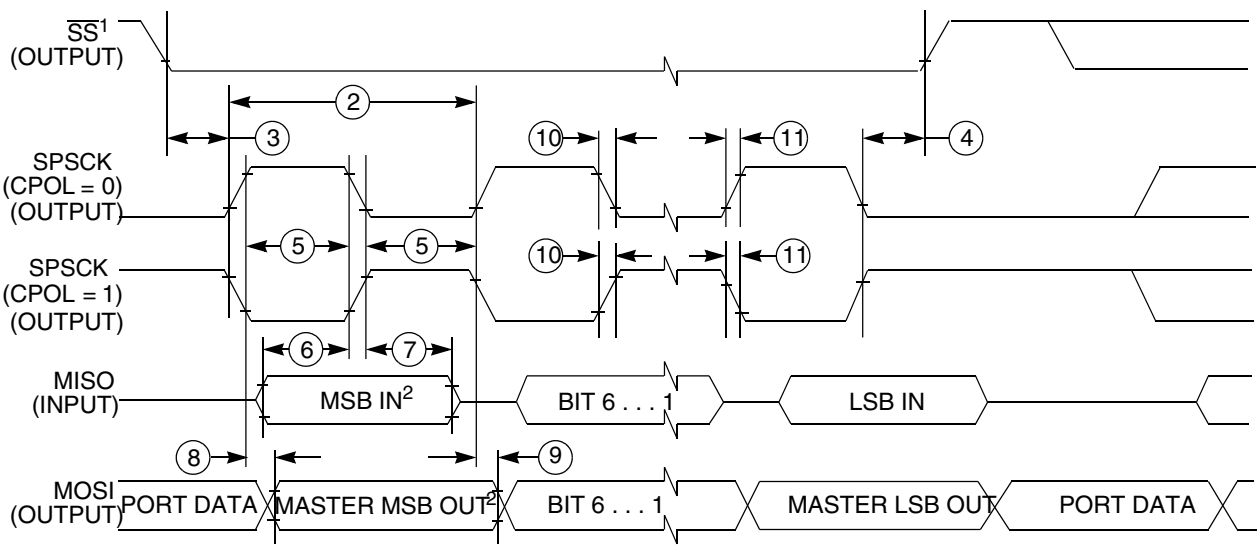
6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 13. SPI master mode timing (CPHA = 1)

Table 25. SPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—

Table continues on the next page...

Table 25. SPI slave mode timing on slew rate disabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	22	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 26. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

8.1 KL05 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

48 LQFP	32 QFN	32 LQFP	24 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	1	PTB6/ IRQ_2/ LPTMR0_ALT3	DISABLED	DISABLED	PTB6/ IRQ_2/ LPTMR0_ALT3	TPM0_CH3	TPM_CLKIN1
2	2	2	2	PTB7/ IRQ_3	DISABLED	DISABLED	PTB7/ IRQ_3	TPM0_CH2	
3	—	—	—	PTA14	DISABLED	DISABLED	PTA14		TPM_CLKIN0
4	—	—	—	PTA15	DISABLED	DISABLED	PTA15		CLKOUT
5	3	3	3	VDD	VDD	VDD			
6	4	4	3	VREFH	VREFH	VREFH			
7	5	5	4	VREFL	VREFL	VREFL			
8	6	6	4	VSS	VSS	VSS			
9	7	7	5	PTA3	EXTAL0	EXTAL0	PTA3	I2C0_SCL	I2C0_SDA
10	8	8	6	PTA4/ LLWU_P0	XTAL0	XTAL0	PTA4/ LLWU_P0	I2C0_SDA	I2C0_SCL
11	—	—	—	VSS	VSS	VSS			
12	—	—	—	PTB18	DISABLED	DISABLED	PTB18		
13	—	—	—	PTB19	DISABLED	DISABLED	PTB19		
14	9	9	7	PTA5/ LLWU_P1/ RTC_CLK_IN	DISABLED	DISABLED	PTA5/ LLWU_P1/ RTC_CLK_IN	TPM0_CH5	SPI0_SS_b
15	10	10	8	PTA6/ LLWU_P2	DISABLED	DISABLED	PTA6/ LLWU_P2	TPM0_CH4	SPI0_MISO
16	11	11	—	PTB8	ADC0_SE11	ADC0_SE11	PTB8	TPM0_CH3	
17	12	12	—	PTB9	ADC0_SE10	ADC0_SE10	PTB9	TPM0_CH2	
18	—	—	—	PTA16/ IRQ_4	DISABLED	DISABLED	PTA16/ IRQ_4		
19	—	—	—	PTA17/ IRQ_5	DISABLED	DISABLED	PTA17/ IRQ_5		
20	—	—	—	PTA18/ IRQ_6	DISABLED	DISABLED	PTA18/ IRQ_6		
21	13	13	9	PTB10	ADC0_SE9/ TSI0_IN7	ADC0_SE9/ TSI0_IN7	PTB10	TPM0_CH1	
22	14	14	10	PTB11	ADC0_SE8/ TSI0_IN6	ADC0_SE8/ TSI0_IN6	PTB11	TPM0_CH0	
23	15	15	11	PTA7/ IRQ_7/ LLWU_P3	ADC0_SE7/ TSI0_IN5	ADC0_SE7/ TSI0_IN5	PTA7/ IRQ_7/ LLWU_P3	SPI0_MISO	SPI0_MOSI
24	16	16	12	PTB0/ IRQ_8/ LLWU_P4	ADC0_SE6/ TSI0_IN4	ADC0_SE6/ TSI0_IN4	PTB0/ IRQ_8/ LLWU_P4	EXTRG_IN	SPI0_SCK

48 LQFP	32 QFN	32 LQFP	24 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
25	17	17	13	PTB1/ IRQ_9	ADC0_SE5/ TSI0_IN3/ DAC0_OUT/ CMP0_IN3	ADC0_SE5/ TSI0_IN3/ DAC0_OUT/ CMP0_IN3	PTB1/ IRQ_9	UART0_TX	UART0_RX
26	18	18	14	PTB2/ IRQ_10/ LLWU_P5	ADC0_SE4/ TSI0_IN2	ADC0_SE4/ TSI0_IN2	PTB2/ IRQ_10/ LLWU_P5	UART0_RX	UART0_TX
27	19	19	15	PTA8	ADC0_SE3/ TSI0_IN1	ADC0_SE3/ TSI0_IN1	PTA8		
28	20	20	16	PTA9	ADC0_SE2/ TSI0_IN0	ADC0_SE2/ TSI0_IN0	PTA9		
29	—	—	—	PTB20	DISABLED	DISABLED	PTB20		
30	—	—	—	VSS	VSS	VSS			
31	—	—	—	VDD	VDD	VDD			
32	—	—	—	PTB14/ IRQ_11	DISABLED	DISABLED	PTB14/ IRQ_11	EXTRG_IN	
33	21	21	—	PTA10/ IRQ_12	DISABLED	TSI0_IN11	PTA10/ IRQ_12		
34	22	22	—	PTA11/ IRQ_13	DISABLED	TSI0_IN10	PTA11/ IRQ_13		
35	23	23	17	PTB3/ IRQ_14	DISABLED	DISABLED	PTB3/ IRQ_14	I2C0_SCL	UART0_TX
36	24	24	18	PTB4/ IRQ_15/ LLWU_P6	DISABLED	DISABLED	PTB4/ IRQ_15/ LLWU_P6	I2C0_SDA	UART0_RX
37	25	25	19	PTB5/ IRQ_16	NMI_b	ADC0_SE1/ CMP0_IN1	PTB5/ IRQ_16	TPM1_CH1	NMI_b
38	26	26	20	PTA12/ IRQ_17/ LPTMR0_ALT2	ADC0_SE0/ CMP0_IN0	ADC0_SE0/ CMP0_IN0	PTA12/ IRQ_17/ LPTMR0_ALT2	TPM1_CH0	TPM_CLKIN0
39	27	27	—	PTA13	TSI0_IN9	TSI0_IN9	PTA13		
40	28	28	—	PTB12	TSI0_IN8	TSI0_IN8	PTB12		
41	—	—	—	PTA19	DISABLED	DISABLED	PTA19		SPI0_SS_b
42	—	—	—	PTB15	DISABLED	DISABLED	PTB15	SPI0_MOSI	SPI0_MISO
43	—	—	—	PTB16	DISABLED	DISABLED	PTB16	SPI0_MISO	SPI0_MOSI
44	—	—	—	PTB17	DISABLED	DISABLED	PTB17	TPM_CLKIN1	SPI0_SCK
45	29	29	21	PTB13	ADC0_SE13	ADC0_SE13	PTB13	TPM1_CH1	RTC_CLKOUT
46	30	30	22	PTA0/ IRQ_0/ LLWU_P7	SWD_CLK	ADC0_SE12/ CMP0_IN2	PTA0/ IRQ_0/ LLWU_P7	TPM1_CH0	SWD_CLK
47	31	31	23	PTA1/ IRQ_1/ LPTMR0_ALT1	RESET_b	DISABLED	PTA1/ IRQ_1/ LPTMR0_ALT1	TPM_CLKIN0	RESET_b
48	32	32	24	PTA2	SWD_DIO	DISABLED	PTA2	CMP0_OUT	SWD_DIO

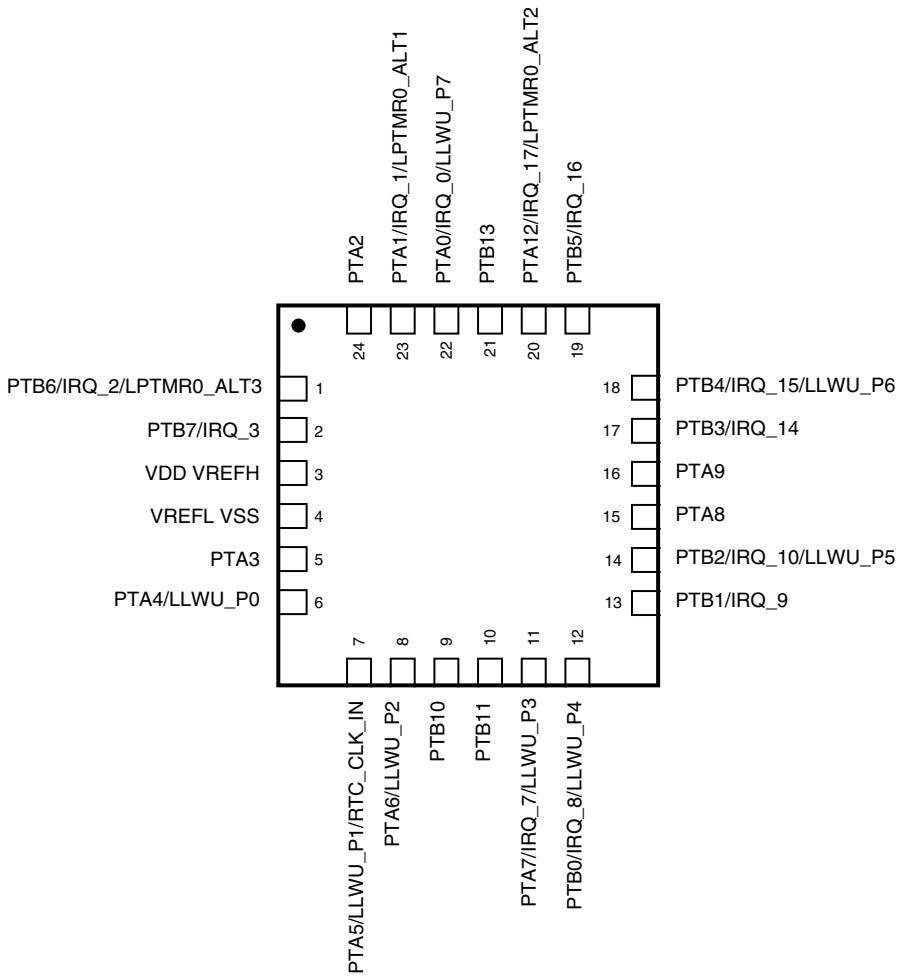


Figure 19. KL05 24-pin QFN pinout diagram

9 Revision History

The following table provides a revision history for this document.

Table 28. Revision History

Rev. No.	Date	Substantial Changes
1	7/2012	Initial NDA release.
2	9/2012	Initial public release.
3	11/2012	Completed all the TBDs.

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