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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36109fv

Figure B.13 Port 5 Block Diagram (P55, P54, P53, P52, P51, P50) 557
Figure B.14 Port 7 Block Diagram (P77) 558
Figure B.15 Port 7 Block Diagram (P76) 558
Figure B.16 Port 7 Block Diagram (P75) 559
Figure B.17 Port 7 Block Diagram (P74) 559
Figure B.18 Port 7 Block Diagram (P72) 560
Figure B.19 Port 7 Block Diagram (P71) 560
Figure B.20 Port 7 Block Diagram (P70) 561
Figure B.21 Port 8 Block Diagram (P87, P86, P85) 561
Figure B.22 Port C Block Diagram (PC3, PC2, PC1, PC0) 562
Figure B.23 Port D Block Diagram (PD7, PD6, PD5, PD4, PD3, PD2, PD1, PD0) 562
Figure B.24 Port E Block Diagram (PE7, PE6, PE5, PE4, PE3, PE2, PE1, PE0) 563
Figure B.25 Port F Block Diagram (PF7, PF6, PF5, PF4, PF3, PF2, PF1, PF0) 563
Figure B.26 Port G Block Diagram (PG7, PG6, PG5) 564
Figure B.27 Port G Block Diagram (PG4, PG3, PG2, PG1, PG0) 564
Figure B.28 Port H Block Diagram (PH7, PH6, PH5, PH4) 565
Figure B.29 Port H Block Diagram (PH3) 565
Figure B.30 Port H Block Diagram (PH2) 566
Figure B.31 Port H Block Diagram (PH1) 566
Figure B.32 Port H Block Diagram (PH0) 567
Figure B.33 Port J Block Diagram (PJ1) 567
Figure B.34 Port J Block Diagram (PJ0) 568
Figure D.1 FP-100A Package Dimensions 571
Figure D.2 FP-100U Package Dimensions 572

When the address break is specified in the data read cycle

Register setting
- ABRKCR = H'A0
- BAR = H'025A

Program

```
  0258  NOP
  025A  NOP
* 025C  MOV.W @H'025A,R0
  0260  NOP
  0262  NOP
    :     :
```

Underline indicates the address to be stacked.

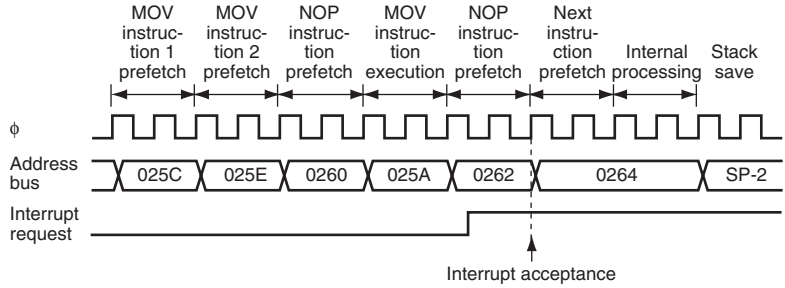
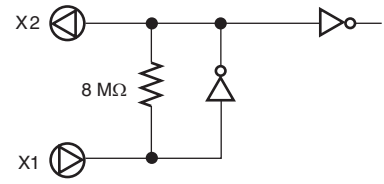


Figure 4.2 Address Break Interrupt Operation Example (2)

5.6 Subclock Generator

Figure 5.14 shows a block diagram of the subclock generator.

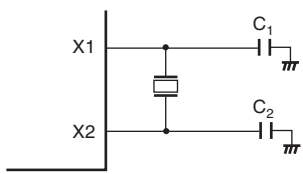


Note: Resistance is a reference value.

Figure 5.14 Block Diagram of Subclock Generator

5.6.1 Connecting 32.768-kHz Crystal Resonator

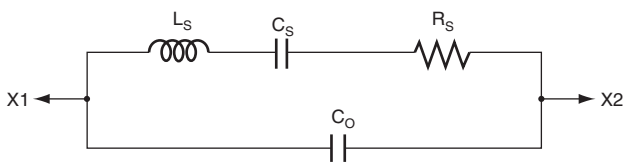
Clock pulses can be supplied to the subclock divider by connecting a 32.768-kHz crystal resonator, as shown in figure 5.15. Figure 5.16 shows the equivalent circuit of the 32.768-kHz crystal resonator.



$C_1 = C_2 = 15$ pF (typ.)

Capacitances are reference values.

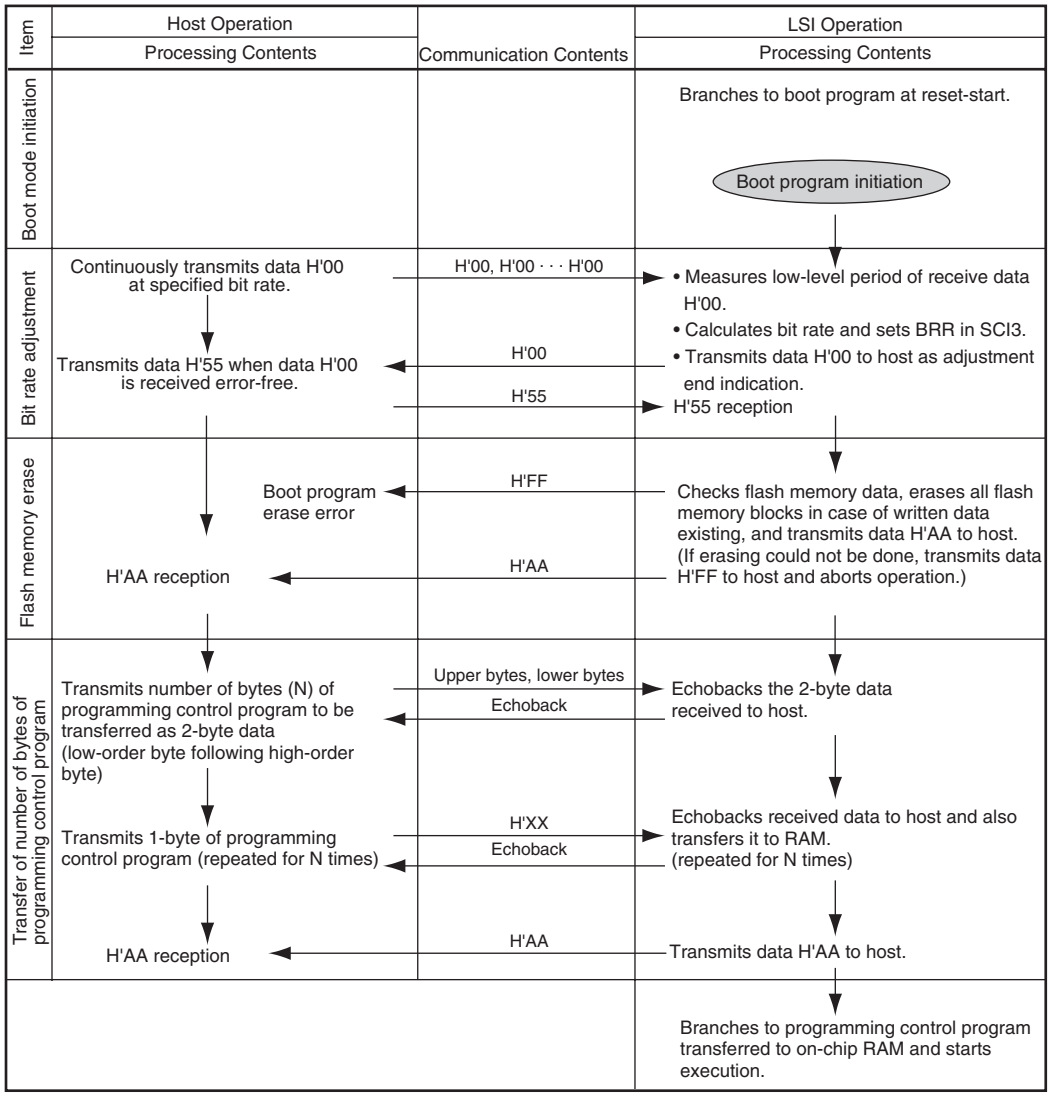
Figure 5.15 Typical Connection to 32.768-kHz Crystal Resonator



$C_O = 1.5$ pF (typ.)
$R_S = 14$ kΩ (typ.)
fW = 32.768 kHz
Note: Parameters are reference values.

Figure 5.16 Equivalent Circuit of 32.768-kHz Crystal Resonator

Table 7.2 Boot Mode Operation



9.1.4 Port Pull-Up Control Register 1 (PUCR1)

PUCR1 controls the pull-up MOS in bit units of the pins set as the input ports.

Bit	Bit Name	Initial Value	R/W	Description
7	PUCR17	0	R/W	Only bits for which PCR1 is cleared are valid. The pull-up MOSs of P17 to P14 and P12 to P10 pins enter the on-state when these bits are set to 1, while they enter the off-state when these bits are cleared to 0. Bit 3 is a reserved bit. This bit is always read as 1.
6	PUCR16	0	R/W	
5	PUCR15	0	R/W	
4	PUCR14	0	R/W	
3	—	1	—	
2	PUCR12	0	R/W	
1	PUCR11	0	R/W	
0	PUCR10	0	R/W	

9.1.5 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P17/$\overline{\text{IRQ3}}$/TRGV pin

Register	PMR1	PCR1	
Bit Name	IRQ3	PCR17	Pin Function
Setting value	0	0	P17 input pin
		1	P17 output pin
	1	X	$\overline{\text{IRQ3}}$ input/TRGV input pin

[Legend] X: Don't care.

- PE3/FTIOD2 pin

Register	TRDOER1_23	TRDFCR_23		TRDPMR_23	TRDIORC_2	PCRE	
Bit Name	ED0	CMD1 and CMD0	PWM3	PWMD0	IOD3 to IOD0	PCRE3	Pin Function
Setting Value	1	XX	X	X	XXXX	0	PE3 input/FTIOD2 input pin
						1	PE3 output pin
	0	00	0	X	XXXX	0	PE3 input/FTIOD2 input pin
						1	PE3 output pin
			1	1	XXXX	X	FTIOD2 output pin
				0	0XXX	0	PE3 input/FTIOD2 input pin
						1	PE3 output pin
					101X or 1001	X	FTIOD2 output pin
					11XX or 1000	0	PE3 input/FTIOD2 input pin
						1	PE3 output pin
		Other than 00	X	X	XXXX	X	FTIOD2 output pin

[Legend] X: Don't care.

Bit	Bit Name	Initial Value	R/W	Description
5	OVF	0	R/W	Timer Overflow Flag Setting condition: When TCNTV overflows from H'FF to H'00 Clearing condition: After reading OVF = 1, cleared by writing 0 to OVF
4	—	1	—	Reserved This bit is always read as 1.
3	OS3	0	R/W	Output Select 3 and 2
2	OS2	0	R/W	These bits select an output method for the TOMV pin by the compare match of TCORB and TCNTV. 00: No change 01: 0 output 10: 1 output 11: Output toggles
1	OS1	0	R/W	Output Select 1 and 0
0	OS0	0	R/W	These bits select an output method for the TOMV pin by the compare match of TCORA and TCNTV. 00: No change 01: 0 output 10: 1 output 11: Output toggles

OS3 and OS2 select the output level for compare match B. OS1 and OS0 select the output level for compare match A. The two output levels can be controlled independently. After a reset, the timer output is 0 until the first compare match.

Figure 14.12 illustrates periodic count operation.

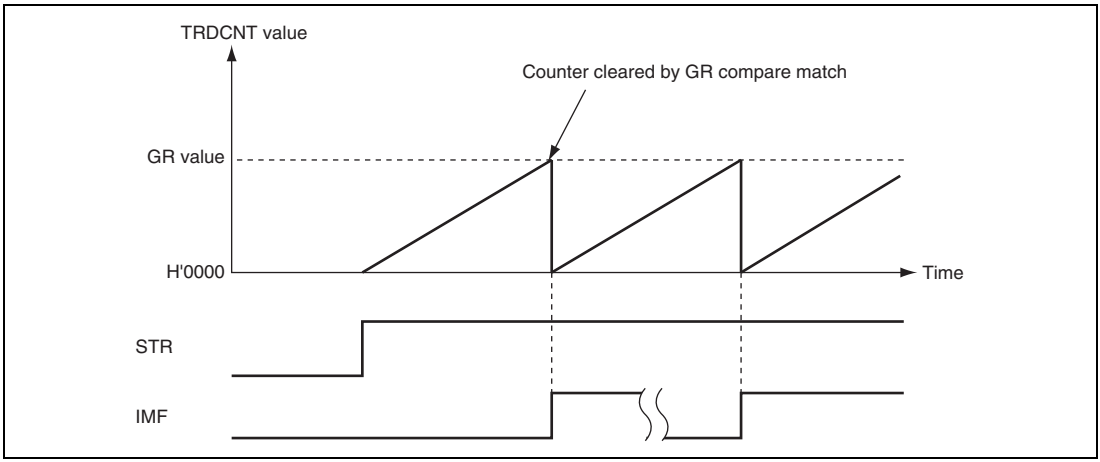


Figure 14.12 Periodic Counter Operation

(2) TRDCNT Count Timing

- Internal clock operation

  A system clock (ϕ), four types of clocks (ϕ/2, ϕ/4, ϕ/8, or ϕ/32) that are generated by dividing the system clock, or on-chip oscillator clock (ϕ40M) can be selected by bits TPSC2 to TPSC0 in TRDCR.

  Figure 14.13 illustrates this timing.

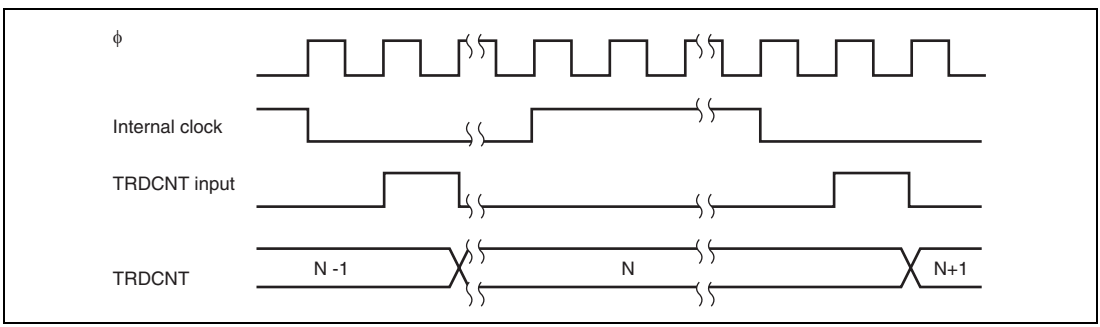


Figure 14.13 Count Timing at Internal Clock Operation

Section 16 14-Bit PWM

The 14-bit PWM is a pulse division type PWM that can be used for electronic tuner control, etc. Figure 16.1 shows a block diagram of the 14-bit PWM.

16.1 Features

- Choice of two conversion periods
  A conversion period of 32768/ϕ with a minimum modulation width of 2/ϕ, or a conversion period of 16384/ϕ with a minimum modulation width of 1/ϕ, can be selected.
- Pulse division method for less ripple

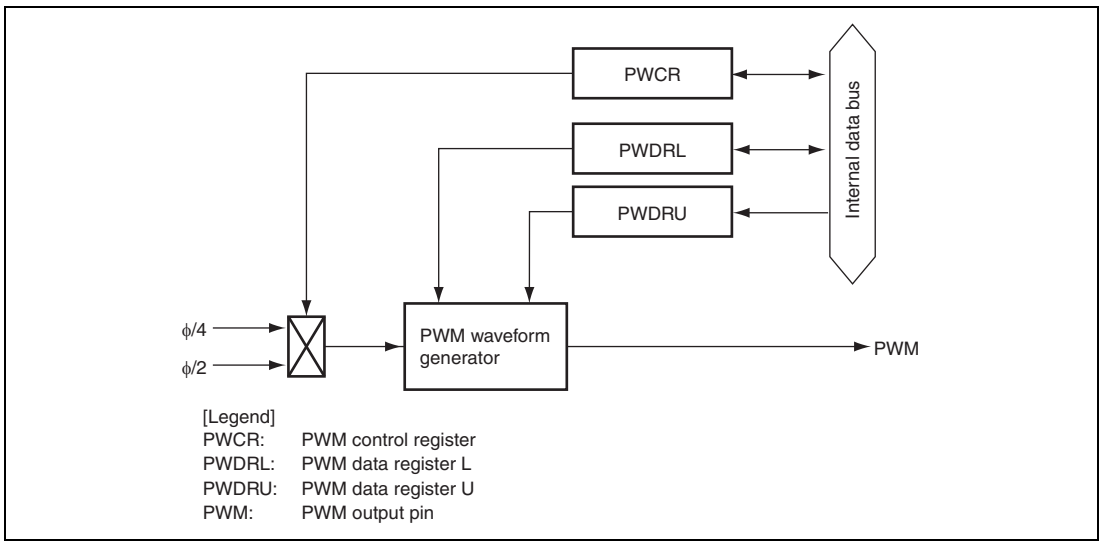


Figure 16.1 Block Diagram of 14-Bit PWM

16.2 Input/Output Pin

Table 16.1 shows the 14-bit PWM pin configuration.

Table 16.1 Pin Configuration

Name	Abbreviation	I/O	Function
14-bit PWM square-wave output	PWM	Output	14-bit PWM square-wave output pin

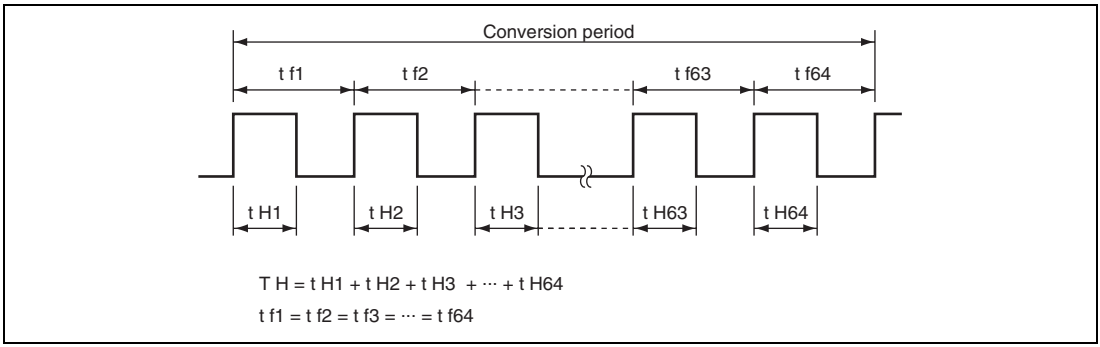


Figure 16.2 Waveform Output by 14-Bit PWM

Table 17.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (1)

	Operating Frequency ϕ (MHz)											
	4			4.9152			5			6		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	70	0.03	2	86	0.31	2	88	–0.25	2	106	–0.44
150	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16
300	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16
600	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16
1200	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16
2400	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16
4800	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16
9600	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34
19200	0	6	–6.99	0	7	0.00	0	7	1.73	0	9	–2.34
31250	0	3	0.00	0	4	–1.70	0	4	0.00	0	5	0.00
38400	0	2	8.51	0	3	0.00	0	3	1.73	0	4	–2.34

	Operating Frequency ϕ (MHz)											
	6.144			7.3728			8			9.8304		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	108	0.08	2	130	–0.07	2	141	0.03	2	174	–0.26
150	2	79	0.00	2	95	0.00	2	103	0.16	2	127	0.00
300	1	159	0.00	1	191	0.00	1	207	0.16	1	255	0.00
600	1	79	0.00	1	95	0.00	1	103	0.16	1	127	0.00
1200	0	159	0.00	0	191	0.00	0	207	0.16	0	255	0.00
2400	0	79	0.00	0	95	0.00	0	103	0.16	0	127	0.00
4800	0	39	0.00	0	47	0.00	0	51	0.16	0	63	0.00
9600	0	19	0.00	0	23	0.00	0	25	0.16	0	31	0.00
19200	0	9	0.00	0	11	0.00	0	12	0.16	0	15	0.00
31250	0	5	2.40	0	6	5.33	0	7	0.00	0	9	–1.70
38400	0	4	0.00	0	5	0.00	0	6	-6.99	0	7	0.00

[Legend]

—: A setting is available but error occurs

17.4.3 Data Transmission

Figure 17.5 shows an example of operation for transmission in asynchronous mode. In transmission, the SCI3 operates as described below.

1. The SCI3 monitors the TDRE flag in SSR. If the flag is cleared to 0, the SCI3 recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI3 sets the TDRE flag to 1 and starts transmission. If the TIE bit is set to 1 at this time, a TXI interrupt request is generated. Continuous transmission is possible because the TXI interrupt routine writes next transmit data to TDR before transmission of the current transmit data has been completed.
3. The SCI3 checks the TDRE flag at the timing for sending the stop bit.
4. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
5. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the "mark state" is entered, in which 1 is output. If the TEIE bit in SCR3 is set to 1 at this time, a TEI interrupt request is generated.
6. Figure 17.6 shows a sample flowchart for transmission in asynchronous mode.

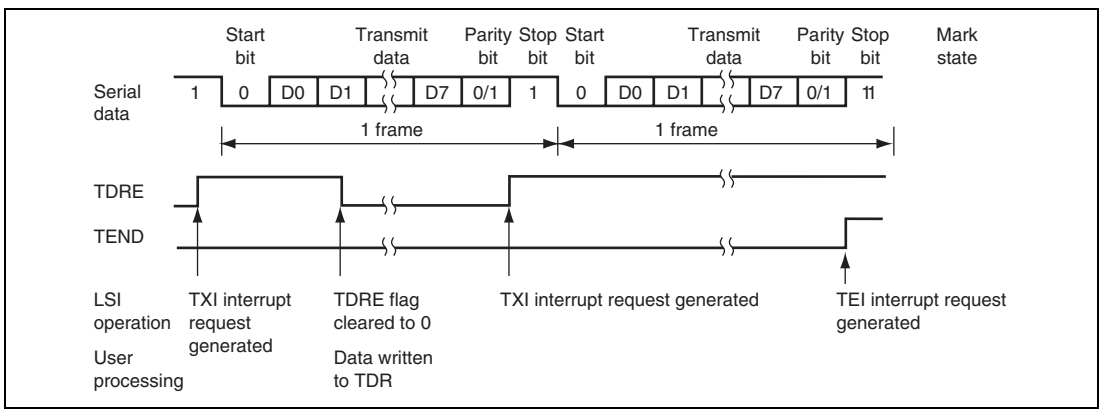


Figure 17.5 Example of SCI3 Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

17.8.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 17.19. Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ (0.5 - \frac{1}{2N}) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%)$$

... Formula (1)

[Legend]

N: Ratio of bit rate to clock (N = 16)

D: Clock duty (D = 0.5 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

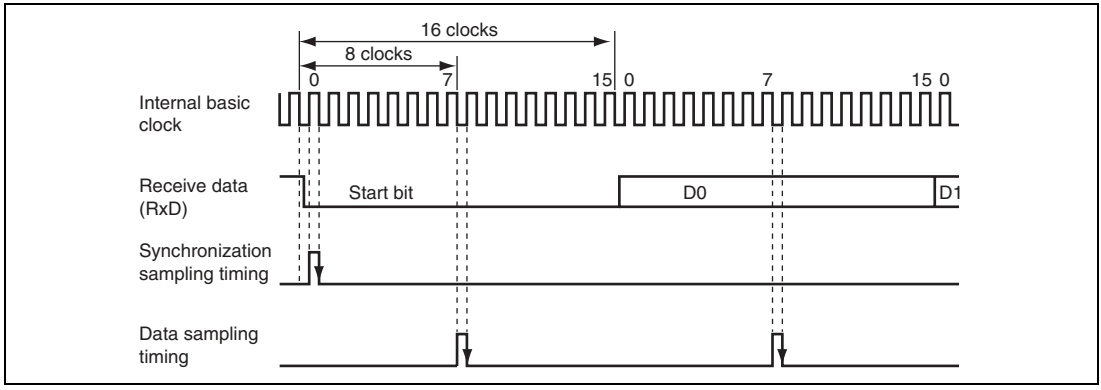


Figure 17.19 Receive Data Sampling Timing in Asynchronous Mode

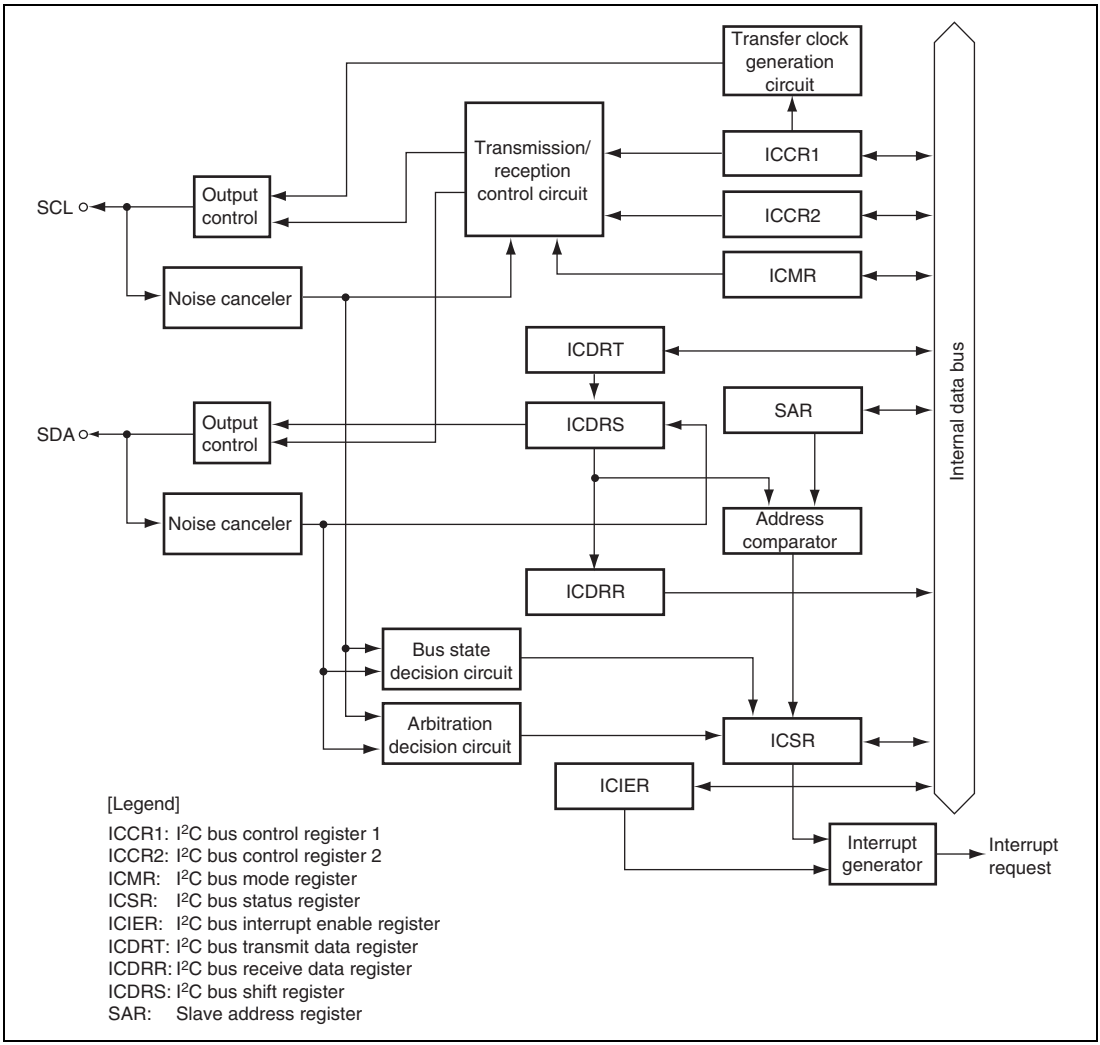


Figure 18.1 Block Diagram of I²C Bus Interface 2

18.3.3 I²C Bus Mode Register (ICMR)

ICMR selects whether the MSB or LSB is transferred first, performs master mode wait control, and selects the transfer bit count.

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I²C bus format is used.
6	WAIT	0	R/W	Wait Insertion Bit In master mode with the I²C bus format, this bit selects whether to insert a wait after data transfer except the acknowledge bit. When WAIT is set to 1, after the fall of the clock for the final data bit, low period is extended for two transfer clocks. If WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted. The setting of this bit is invalid in slave mode with the I²C bus format or with the clocked synchronous serial format.
5	—	1	—	Reserved
4	—	1	—	These bits are always read as 1.
3	BCWP	1	R/W	BC Write Protect This bit controls the BC2 to BC0 modifications. When modifying BC2 to BC0, this bit should be cleared to 0 and use the MOV instruction. In clock synchronous serial mode, BC should not be modified. 0: When writing, values of BC2 to BC0 are set. 1: When reading, 1 is always read. When writing, settings of BC2 to BC0 are invalid.

Register Name	Abbreviation	Bit No.	Address	Module Name	Data Bus Width	Access State
Port mode register 3	PMR3	8	H'FFFFE2	I/O Port	8	2
Port control register 1	PCR1	8	H'FFFFE4	I/O Port	8	2
Port control register 2	PCR2	8	H'FFFFE5	I/O Port	8	2
Port control register 3	PCR3	8	H'FFFFE6	I/O Port	8	2
Port control register 5	PCR5	8	H'FFFFE8	I/O Port	8	2
Port control register 7	PCR7	8	H'FFFFEA	I/O Port	8	2
Port control register 8	PCR8	8	H'FFFFEB	I/O Port	8	2
Port control register C	PCRC	8	H'FFFFEE	I/O Port	8	2
System control register 3	SYSCR3	8	H'FFFFEF	Power-down modes	8	2
System control register 1	SYSCR1	8	H'FFFFF0	Power-down modes	8	2
System control register 2	SYSCR2	8	H'FFFFF1	Power-down modes	8	2
Interrupt edge select register 1	IEGR1	8	H'FFFFF2	Interrupt	8	2
Interrupt edge select register 2	IEGR2	8	H'FFFFF3	Interrupt	8	2
Interrupt enable register 1	IENR1	8	H'FFFFF4	Interrupt	8	2
Interrupt enable register 2	IENR2	8	H'FFFFF5	Interrupt	8	2
Interrupt flag register 1	IRR1	8	H'FFFFF6	Interrupt	8	2
Interrupt flag register 2	IRR2	8	H'FFFFF7	Interrupt	8	2
Wakeup interrupt flag register	IWPR	8	H'FFFFF8	Interrupt	8	2
Module standby control register 1	MSTCR1	8	H'FFFFF9	Power-down modes	8	2
Module standby control register 2	MSTCR2	8	H'FFFFFA	Power-down modes	8	2

Notes: 1. These registers can be accessed by word size only.
2. WDT: Watchdog timer

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
JMP	JMP @ERn	—			2							PC ← ERn	—	—	—	—	—	—	4	
	JMP @aa:24	—						4				PC ← aa:24	—	—	—	—	—	—	6	
	JMP @@aa:8	—								2		PC ← @aa:8	—	—	—	—	—	—	8	10
BSR	BSR d:8	—							2			PC → @–SP PC ← PC+d:8	—	—	—	—	—	—	6	8
	BSR d:16	—							4			PC → @–SP PC ← PC+d:16	—	—	—	—	—	—	8	10
JSR	JSR @ERn	—			2							PC → @–SP PC ← ERn	—	—	—	—	—	—	6	8
	JSR @aa:24	—						4				PC → @–SP PC ← aa:24	—	—	—	—	—	—	8	10
	JSR @@aa:8	—								2		PC → @–SP PC ← @aa:8	—	—	—	—	—	—	8	12
RTS	RTS	—									2	PC ← @SP+	—	—	—	—	—	—	8	10

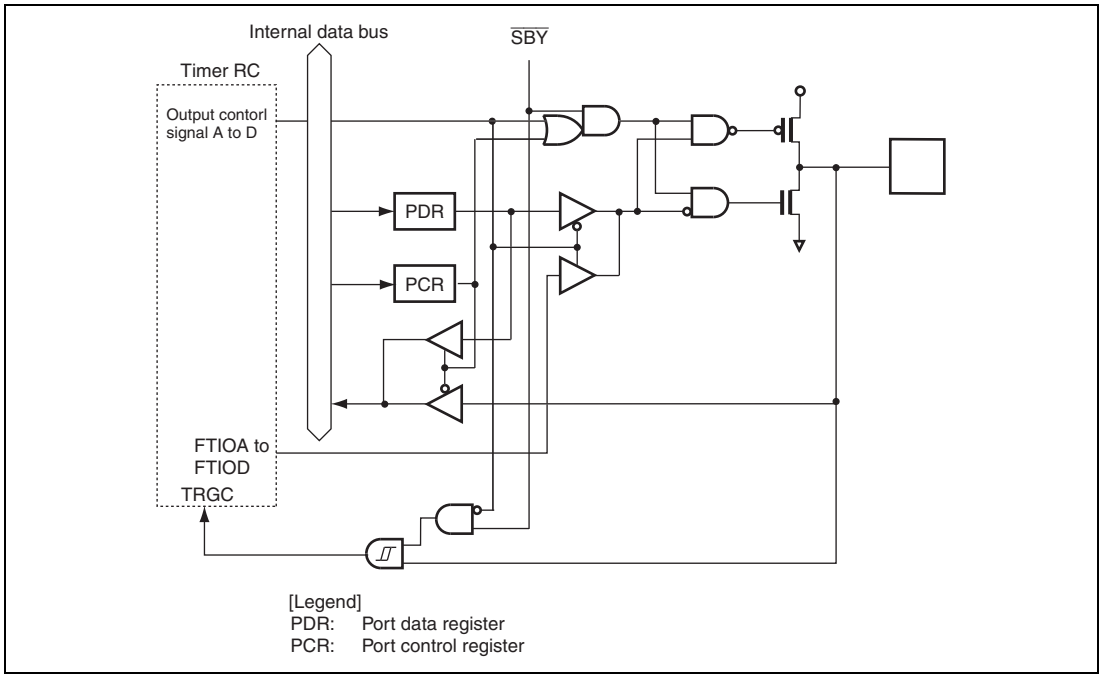


Figure B.28 Port H Block Diagram (PH7, PH6, PH5, PH4)

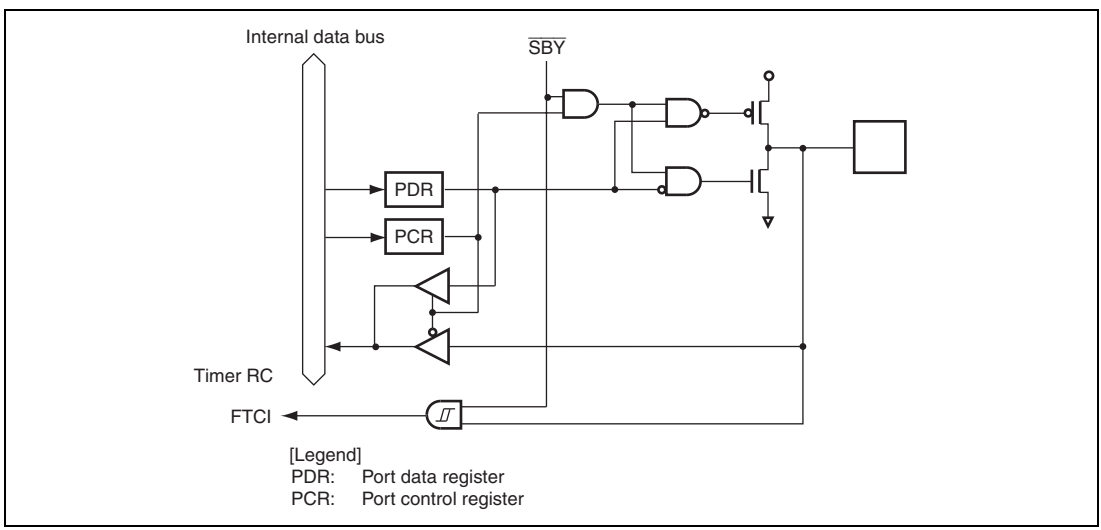


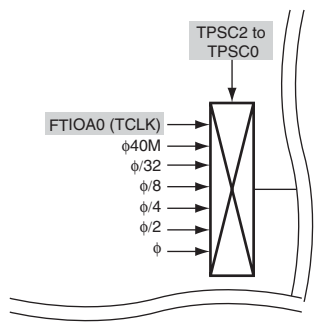
Figure B.29 Port H Block Diagram (PH3)

Main Revisions and Additions in this Edition

Item	Page	Revisions (See Manual for Details)
Section 5 Clock Pulse Generators 5.2.4 Clock Control/Status Register (CKCSR)	76	Amended

Bit	Bit Name	Description			
7	PMRJ1	OSC Pin Function Select 1 and 0			
6	PMRJ0	PMRJ1	PMRJ0	OSC2	OSC1
		0	0	I/O	I/O
		1	0	CLKOUT	I/O
		0	1	Hi-Z	OSC1 (external clock input)
		1	1	OSC2	OSC1

Section 14 Timer RD Figure 14.54 Block Diagram of Digital Filter	346	Amended



Section 17 Serial Communication Interface 3 (SCI3) 17.8.2 Mark State and Break Sending	404	Amended When the TXD or TXD2 bit in PMR1 or the TXD_3 bit in SMCR is 1, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1 and also set the TXD bit to 1. Then, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then set the TXD bit to 1. At this time, regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.