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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b SAR; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36109gfv

Section 1 Overview

1.1 Features

- High-speed H8/300H central processing unit with an internal 16-bit architecture
  Upward-compatible with H8/300 CPU on an object level
  Sixteen 16-bit general registers
  62 basic instructions
- Various peripheral functions
  RTC (can be used as a free running counter)
  Timer B1 (8-bit timer)
  Timer V (8-bit timer)
  Timer RC (16-bit timer)
  Timer RD (16-bit timer)
  14-bit PWM
  Watchdog timer
  SCI3 (Asynchronous or clock synchronous serial communication interface)
  I^2C bus interface 2 (conforms to the I^2C bus interface format that is advocated by Philips Electronics)
  10-bit A/D converter
  POR/LVD (Power-on reset and low-voltage detection circuit) (optional)
- On-chip memory

		Model				
Product Classification		Standard Version	On-Chip Power-On Reset and Low-Voltage Detection Circuit Version	ROM	RAM	Remark
Flash memory version (F-ZTAT™ version)	H8/36109F	HD64F36109	HD64F36109G	128 kbytes	5 kbytes	

Note: F-ZTAT™ is a trademark of Renesas Technology Corp.

2.5 Addressing Modes and Effective Address Calculation

2.5.1 Addressing Modes

The H8/300H CPU supports the eight addressing modes listed in table 2.10. Each instruction uses a subset of these addressing modes. Addressing modes that can be used differ depending on the instruction. For details, refer to appendix A.4, Combinations of Instructions and Addressing Modes.

Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit-manipulation instructions use register direct, register indirect, or the absolute addressing mode (@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

(1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

(2) Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn), the lower 24 bits of which contain the address of the operand on memory.

5.8 Usage Notes

5.8.1 Note on Resonators

Resonator characteristics are closely related to board design and should be carefully evaluated by the user, referring to the examples shown in this section. Resonator circuit parameters will differ depending on the resonator element, stray capacitance of the PCB, and other factors. Suitable values should be determined in consultation with the resonator element manufacturer. Design the circuit so that the resonator element never receives voltages exceeding its maximum rating.

5.8.2 Notes on Board Design

When using a crystal resonator (ceramic resonator), place the resonator and its load capacitors as close as possible to pins OSC1 and OSC2. Other signal lines should be routed away from the oscillator circuit to prevent induction from interfering with correct oscillation (see figure 5.18).

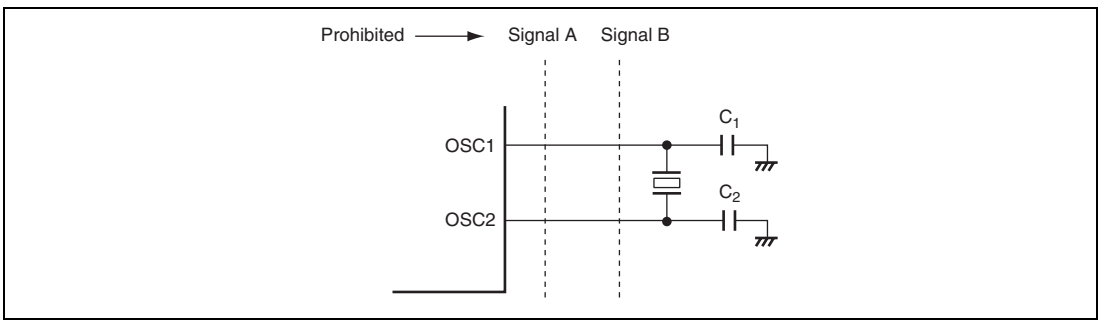


Figure 5.18 Example of Incorrect Board Design

10.3.4 Day-of-Week Data Register (RWKDR)

RWKDR counts the BCD-coded day-of-week value on the carry generated once per day by RHRDR. The setting range is decimal 0 to 6 using bits WK2 to WK0.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—	R	RTC Busy This bit is set to 1 when the RTC is updating (operating) the values of second, minute, hour, and day-of-week data registers. When this bit is 0, the values of second, minute, hour, and day-of-week data registers must be adopted.
6	—	0	—	Reserved
5	—	0	—	These bits are always read as 0.
4	—	0	—	
3	—	0	—	
2	WK2	—	R/W	Day-of-Week Counting
1	WK1	—	R/W	Day-of-week is indicated with a binary code
0	WK0	—	R/W	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday 111: Reserved (setting prohibited)

10.3.7 Clock Source Select Register (RTCCSR)

RTCCSR selects clock source. A free running counter controls start/stop of counter operation by the RUN bit in RTCCR1. When a clock other than 32.768 kHz is selected, the RTC is disabled and operates as an 8-bit free running counter. When the RTC operates as an 8-bit free running counter, RSECDR enables counter values to be read. An interrupt can be generated by setting 1 to the FOIE bit in RTCCR2 and enabling an overflow interrupt of the free running counter. A clock in which the system clock is divided by 32, 16, 8, or 4 is output in active or sleep mode.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	Selects a clock output from the TMOW pin when setting TMOW in PMR1 to 1. 00: ϕ/4 01: ϕ/8 10: ϕ/16 11: ϕ/32
4	—	0	—	Reserved This bit is always read as 0.
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: ϕ/8····· Free running counter operation
1	RCS1	0	R/W	0001: ϕ/32····· Free running counter operation
0	RCS0	0	R/W	0010: ϕ/128····· Free running counter operation 0011: ϕ/256····· Free running counter operation 0100: ϕ/512····· Free running counter operation 0101: ϕ/2048····· Free running counter operation 0110: ϕ/4096····· Free running counter operation 0111: ϕ/8192····· Free running counter operation 1XXX: 32.768 kHz···RTC operation

[Legend]
X: Don't care

Table 12.2 Clock Signals to Input to TCNTV and Counting Conditions

	TCRV0		TCRV1	
Bit 2	Bit 1	Bit 0	Bit 0	
CKS2	CKS1	CKS0	ICKS0	Description
0	0	0	—	Clock input prohibited
		1	0	Internal clock: counts on ϕ/4, falling edge
			1	Internal clock: counts on ϕ/8, falling edge
	1	0	0	Internal clock: counts on ϕ/16, falling edge
			1	Internal clock: counts on ϕ/32, falling edge
		1	0	Internal clock: counts on ϕ/64, falling edge
			1	Internal clock: counts on ϕ/128, falling edge
1	0	0	—	Clock input prohibited
		1	—	External clock: counts on rising edge
	1	0	—	External clock: counts on falling edge
		1	—	External clock: counts on rising and falling edge

12.3.4 Timer Control/Status Register V (TCSRV)

TCSRV indicates the status flag and controls outputs by using a compare match.

Bit	Bit Name	Initial Value	R/W	Description
7	CMFB	0	R/W	Compare Match Flag B Setting condition: When the TCNTV value matches the TCORB value Clearing condition: After reading CMFB = 1, cleared by writing 0 to CMFB
6	CMFA	0	R/W	Compare Match Flag A Setting condition: When the TCNTV value matches the TCORA value Clearing condition: After reading CMFA = 1, cleared by writing 0 to CMFA

13.3.1 Timer RC Mode Register (TRCMR)

TRCMR selects the general register functions and the timer output mode.

Bit	Bit Name	Initial Value	R/W	Description
7	CTS	0	R/W	Counter Start TRCCNT stops counting when this bit is 0, while it performs counting when this bit is 1. [Setting condition] • When 1 is written in CTS [Clearing conditions] • When 0 is written in CTS • In PWM2 mode, when the CSTP bit in TRCCR2 is set to 1 and a compare match signal is generated
6	—	1	—	Reserved This bit is always read as 1.
5	BUFEB	0	R/W	Buffer Operation B Selects the GRD function. 0: GRD functions as an input capture/output compare register 1: GRD functions as the buffer register for GRB
4	BUFEA	0	R/W	Buffer Operation A Selects the GRC function. 0: GRC functions as an input capture/output compare register 1: GRC functions as the buffer register for GRA
3	PWM2	1	R/W	PWM2 Mode Selects the output mode of the FTIOB pin. 0: Functions in PWM2 mode. The following settings are invalid: TRCIOR0, TRCIOR1, and the PWMB, PWMC, and PWMD bits in TRCMR. 1: Functions in timer mode or PWM mode. The following settings are valid: TRCIOR0, TRCIOR1, and the PWMB, PWMC, and PWMD bits in TRCMR.

13.3.10 Timer RC Counter (TRCCNT)

TRCCNT is a 16-bit readable/writable up-counter. The input clock is selected by bits CKS2 to CKS0 in TRCCR1. TRCCNT can be cleared to H'0000 through a compare match of GRA by setting the CCLR bit in TRCCR1 to 1. When TRCCNT overflows (changes from H'FFFF to H'0000), the OVF flag in TRCSR is set to 1. If the OVIE bit in TRCIER is set to 1 at this time, an interrupt request is generated. TRCCNT must always be read from or written to in units of 16 bits; 8-bit accesses are not allowed. TRCCNT is initialized to H'0000 by a reset.

13.3.11 General Registers A, B, C, and D (GRA, GRB, GRC, and GRD)

Each general register is a 16-bit readable/writable register that can function as either an output-compare register or an input-capture register. The function is selected by settings in TRCIOR0 and TRCIOR1.

When a general register is used as an input-compare register, its value is constantly compared with the TRCCNT value. When the two values match (a compare match), the corresponding flag (the IMFA, IMFB, IMFC, or IMFD bit) in TRCSR is set to 1. An interrupt request is generated at this time, when the IMIEA, IMIEB, IMIEC, or IMIED bit in TRCIER is set to 1. A compare match output can be selected in TRCIOR.

When a general register is used as an input-capture register, an external input-capture signal is detected and the current TRCCNT value is stored in the general register. The corresponding flag (the IMFA, IMFB, IMFC, or IMFD bit) in TRCSR is set to 1. If the corresponding interrupt-enable bit (the IMIEA, IMIEB, IMIEC, or IMIED bit) in TRIER is set to 1 at this time, an interrupt request is generated. The edge of the input-capture signal is selected in TRCIOR.

GRC and GRD can be used as buffer registers of GRA and GRB, respectively, by setting BUFEA and BUFEB in TRCMR.

For example, when GRA is set as an output-compare register and GRC is set as the buffer register for GRA, the value in the buffer register GRC is sent to GRA whenever compare match A is generated.

When GRA is set as an input-capture register and GRC is set as the buffer register for GRA, the value in TRCCNT is transferred to GRA and the value in the buffer register GRC is transferred to GRA whenever an input capture is generated.

GRA to GRD must be written or read in 16-bit units; 8-bit access is not allowed. GRA to GRD are initialized to H'FFFF by a reset.

13.5.2 Output Compare Output Timing

The compare match signal is generated in the last state in which TRCCNT and GR match (when TRCCNT changes from the matching value to the next value). When the compare match signal is generated, the output value selected in TRCIOR is output on the compare match output pin (FTIOA, FTIOB, FTIOC, or FTIOD).

When TRCCNT matches GR, the compare match signal is generated only after the next counter clock pulse is input.

Figure 13.25 shows the output compare timing.

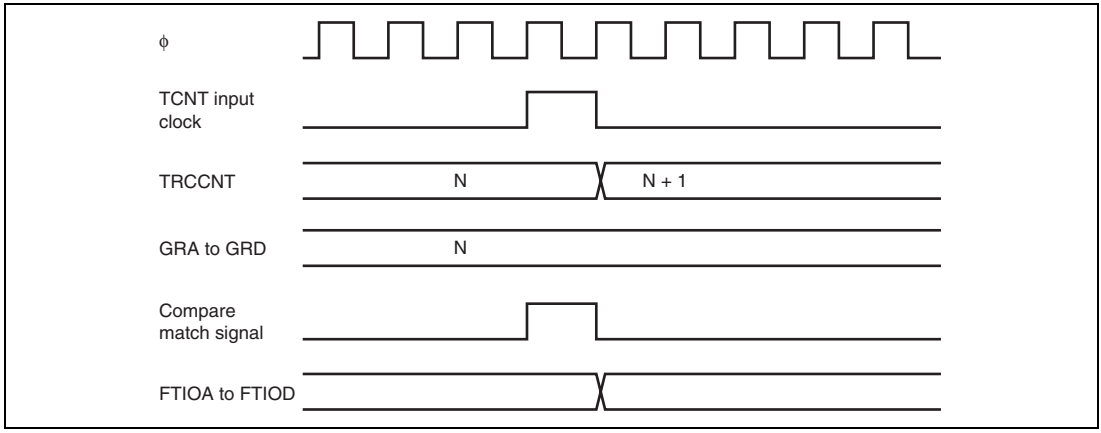


Figure 13.25 Output Compare Output Timing

Bit	Bit Name	Initial Value	R/W	Description
3	IOC3	1	R/W	I/O Control C3 Specifies GRC to be used as GR for the FTIOA or FTIOC pin. 0: GRC is used as GR for the FTIOA pin 1: GRC is used as GR for the FTIOC pin
2	IOC2	0	R/W	I/O Control C2 Selects the GRC function. 0: GRC functions as an output compare register 1: GRC functions as an input capture register
1	IOC1	0	R/W	I/O Control C1 and C0
0	IOC0	0	R/W	When IOC3 = 0, 00: No output at compare match 01: 0 output to the FTIOA pin at GRC compare match 10: 1 output to the FTIOA pin at GRC compare match 11: Output toggles to the FTIOA pin at GRC compare match When IOC3 = 1 and IOC2 = 0, 00: No output at compare match 01: 0 output to the FTIOC pin at GRC compare match 10: 1 output to the FTIOC pin at GRC compare match 11: Output toggles to the FTIOC pin at GRC compare match When IOC3 = 1 and IOC2 = 1, 00: Input capture to GRC at rising edge at the FTIOC pin 01: Input capture to GRC at falling edge at the FTIOC pin 1X: Input capture to GRC at rising and falling edges at the FTIOC pin

[Legend]

X: Don't care.

Note: When a GR register functions as a buffer register for a paired GR register, the settings in the IOA2 and IOB2 bits in TRDIORA and the IOC2 and IOD2 bits in TRDIORC of both registers should be the same.

14.4.1 Counter Operation

When one of bits STR0 and STR1 in TRDSTR is set to 1, the TRDCNT counter for the corresponding channel begins counting. TRDCNT can operate as a free-running counter, periodic counter, for example. Figure 14.10 shows an example of the counter operation setting procedure.

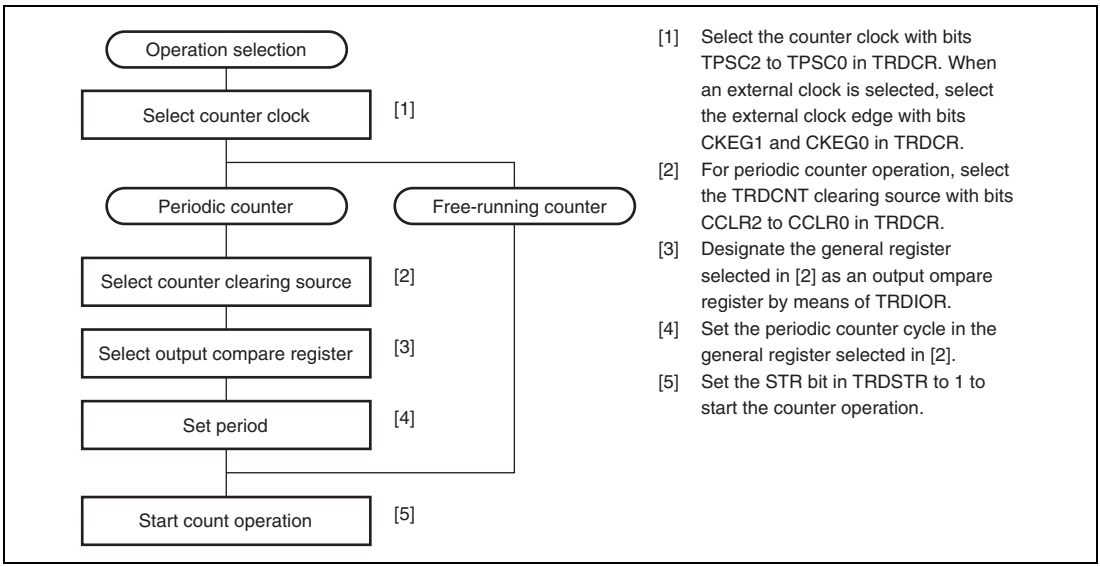


Figure 14.10 Example of Counter Operation Setting Procedure

(1) Examples of Waveform Output Operation

Figure 14.16 shows an example of 0 output/1 output.

In this example, TRDCNT has been designated as a free-running counter, and settings have been made such that 0 is output by compare match A, and 1 is output by compare match B. When the set level and the pin level coincide, the pin level does not change.

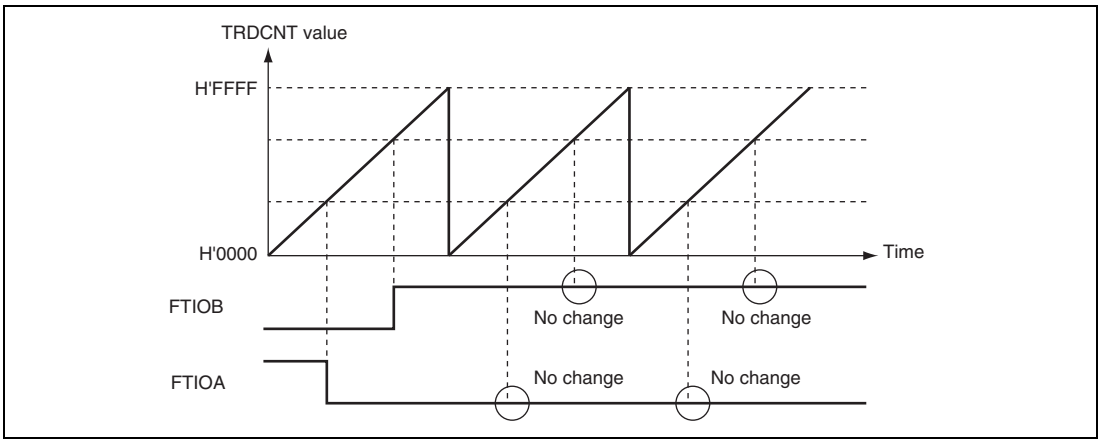


Figure 14.16 Example of 0 Output/1 Output Operation

Figure 14.17 shows an example of toggle output.

In this example, TRDCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made such that the output is toggled by both compare match A and compare match B.

14.4.3 Input Capture Function

The TRDCNT value can be transferred to GR on detection of the input edge of the input capture/output compare pin (FTIOA, FTIOB, FTIOC, or FTIOD). Rising edge, falling edge, or both edges can be selected as the detected edge. When the input capture function is used, the pulse width or period can be measured.

Figure 14.19 shows an example of the input capture operation setting procedure.

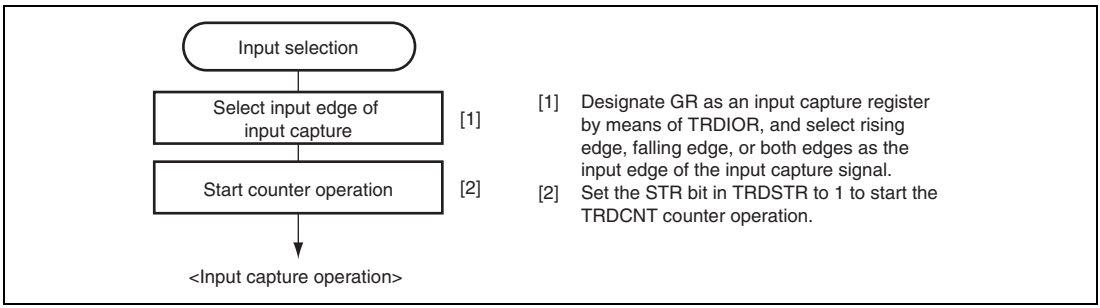


Figure 14.19 Example of Input Capture Operation Setting Procedure

14.5.2 Status Flag Clearing Timing

The status flag can be cleared by writing 0 after reading 1 from the CPU. Figure 14.61 shows the timing in this case.

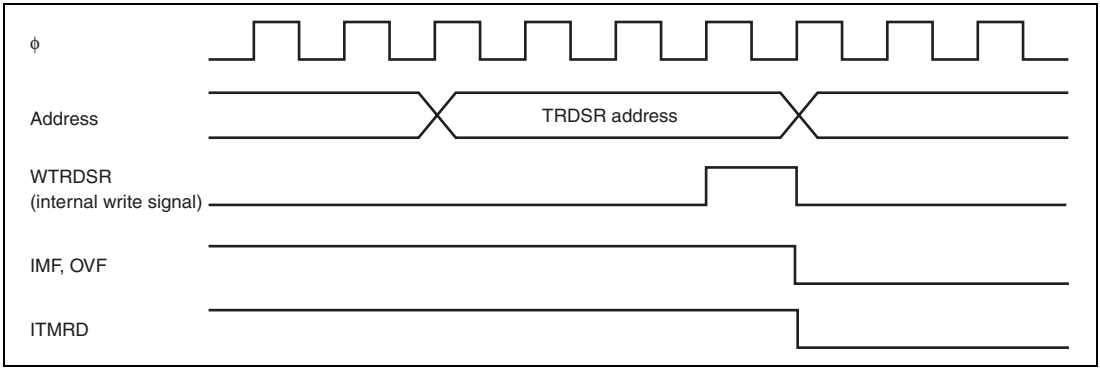


Figure 14.61 Status Flag Clearing Timing

14.6 Usage Notes

(1) Input Pulse Width of Input Clock Signal and Input Capture Signal

The pulse width of the input clock signal and the input capture signal must be at least three system clock (ϕ) cycles when bits TPSC2 to TPSC0 in TRDCR = B'0XX or B'10X, or at least three on-chip oscillator clock (ϕ40M) cycles when B'110; shorter pulses will not be detected correctly.

16.3.2 PWM Data Registers U, L (PWDRU, PWDRL)

PWDRU and PWDRL indicate high level width in one PWM waveform cycle. PWDRU and PWDRL are 14-bit write-only registers, with the upper 6 bits assigned to PWDRU and the lower 8 bits to PWDRL. When read, all bits are always read as 1.

Both PWDRU and PWDRL are accessible only in bytes. Note that the operation is not guaranteed if word access is performed. When 14-bit data is written in PWDRU and PWDRL, the contents are latched in the PWM waveform generator and the PWM waveform generation data is updated. When writing the 14-bit data, the order is as follows: PWDRL to PWDRU.

PWDRU and PWDRL are initialized to H'C000.

16.4 Operation

When using the 14-bit PWM, set the registers in this sequence:

1. Set the PWM bit in the port mode register 1 (PMR1) to set the P11/PWM pin to function as a PWM output pin.
2. Set the PWCR0 bit in PWCR to select a conversion period of either.
3. Set the output waveform data in PWDRU and PWDRL. Be sure to write byte data first to PWDRL and then to PWDRU. When the data is written in PWDRU, the contents of these registers are latched in the PWM waveform generator, and the PWM waveform generation data is updated in synchronization with internal signals.

One conversion period consists of 64 pulses, as shown in figure 16.2. The total high-level width during this period (T_H) corresponds to the data in PWDRU and PWDRL. This relation can be expressed as follows:

$$T_H = (\text{data value in PWDRU and PWDRL} + 64) \times t\phi/2$$

where $t\phi$ is the period of PWM clock input: $2/\phi$ (bit PWCR0 = 0) or $4/\phi$ (bit PWCR0 = 1).
If the data value in PWDRU and PWDRL is from H'FFC0 to H'FFFF, the PWM output stays high. When the data value is H'C000, T_H is calculated as follows:

$$T_H = 64 \times t\phi/2 = 32\ t\phi$$

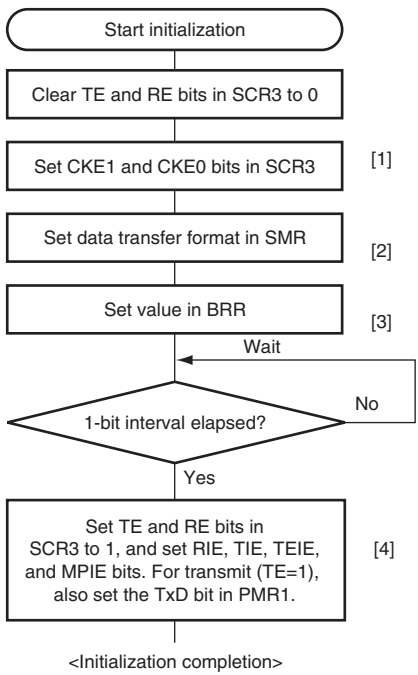
17.3.7 Serial Status Register (SSR)

SSR is a register containing status flags of the SCI3 and multiprocessor bits for transfer. 1 cannot be written to flags TDRE, RDRF, OER, PER, and FER; they can only be cleared.

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	1	R/W	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • When the TE bit in SCR3 is 0 • When data is transferred from TDR to TSR [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the transmit data is written to TDR
6	RDRF	0	R/W	Receive Data Register Full Indicates that the received data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When data is read from RDR
5	OER	0	R/W	Overrun Error [Setting condition] • When an overrun error occurs in reception [Clearing condition] • When 0 is written to OER after reading OER = 1

17.4.2 SCI3 Initialization

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR3 to 0, then initialize the SCI3 as described below. When the operating mode, or transfer format, is changed for example, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not initialize the contents of the RDRF, PER, FER, and OER flags, or the contents of RDR. When the external clock is used in asynchronous mode, the clock must be supplied even during initialization.



[1] Set the clock selection in SCR3. Be sure to clear bits RIE, TIE, TEIE, and MPIE, and bits TE and RE, to 0.

When the clock output is selected in asynchronous mode, clock is output immediately after CKE1 and CKE0 settings are made. When the clock output is selected at reception in clocked synchronous mode, clock is output immediately after CKE1, CKE0, and RE are set to 1.

[2] Set the data transfer format in SMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR3 to 1. RE settings enable the RXD pin to be used. For transmission, set the TXD bit in PMR1 to 1 to enable the TXD output pin to be used. Also set the RIE, TIE, TEIE, and MPIE bits, depending on whether interrupts are required. In asynchronous mode, the output pin level is in the mark state for transmission and the input in level is in the idle state for reception. SCI3 waites for a start bit in the idle state. SCI3 is ready for transmission after 1 is output for a signal frame.

Figure 17.4 Sample SCI3 Initialization Flowchart

Register Name	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
LVDCR	Initialized	—	—	—	—	—	LVD (optional)
LVDSR	Initialized	—	—	—	—	—	
CKCSR	Initialized	—	—	—	—	—	Clock pulse generator
RCCR	Initialized	—	—	—	—	—	On-chip oscillator
RCTRMDPR	Initialized	—	—	—	—	—	
RCTRMDR	Initialized	—	—	—	—	—	
ICRA	Initialized	—	—	—	—	—	Interrupt
ICRB	Initialized	—	—	—	—	—	
ICRC	Initialized	—	—	—	—	—	
ICRD	Initialized	—	—	—	—	—	
SMR_2	Initialized	—	—	Initialized	Initialized	Initialized	SCI3_2
BRR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3_2	Initialized	—	—	Initialized	Initialized	Initialized	
TDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SSR_2	Initialized	—	—	Initialized	Initialized	Initialized	
RDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
ICCR1	Initialized	—	—	—	—	—	IIC2
ICCR2	Initialized	—	—	—	—	—	
ICMR	Initialized	—	—	—	—	—	
ICIER	Initialized	—	—	—	—	—	
ICSR	Initialized	—	—	—	—	—	
SAR	Initialized	—	—	—	—	—	
ICDRT	Initialized	—	—	—	—	—	
ICDRR	Initialized	—	—	—	—	—	
TMB1	Initialized	—	—	—	—	—	Timer B1
TCB1	Initialized	—	—	—	—	—	
TLB1	Initialized	—	—	—	—	—	

Table A.4 Number of Cycles in Each Instruction

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ADD	ADD.B #xx:8, Rd	1					
	ADD.B Rs, Rd	1					
	ADD.W #xx:16, Rd	2					
	ADD.W Rs, Rd	1					
	ADD.L #xx:32, ERd	3					
	ADD.L ERs, ERd	1					
ADDS	ADDS #1/2/4, ERd	1					
ADDX	ADDX #xx:8, Rd	1					
	ADDX Rs, Rd	1					
AND	AND.B #xx:8, Rd	1					
	AND.B Rs, Rd	1					
	AND.W #xx:16, Rd	2					
	AND.W Rs, Rd	1					
	AND.L #xx:32, ERd	3					
	AND.L ERs, ERd	2					
ANDC	ANDC #xx:8, CCR	1					
BAND	BAND #xx:3, Rd	1					
	BAND #xx:3, @ERd	2			1		
	BAND #xx:3, @aa:8	2			1		
Bcc	BRA d:8 (BT d:8)	2					
	BRN d:8 (BF d:8)	2					
	BHI d:8	2					
	BLS d:8	2					
	BCC d:8 (BHS d:8)	2					
	BCS d:8 (BLO d:8)	2					
	BNE d:8	2					
	BEQ d:8	2					
	BVC d:8	2					
	BVS d:8	2					
	BPL d:8	2					
	BMI d:8	2					
	BGE d:8	2					

B. I/O Port Block Diagrams

B.1 I/O Port Block Diagrams

$\overline{RES}$ goes low in a reset, and $\overline{SBY}$ goes low at a reset and in standby mode.

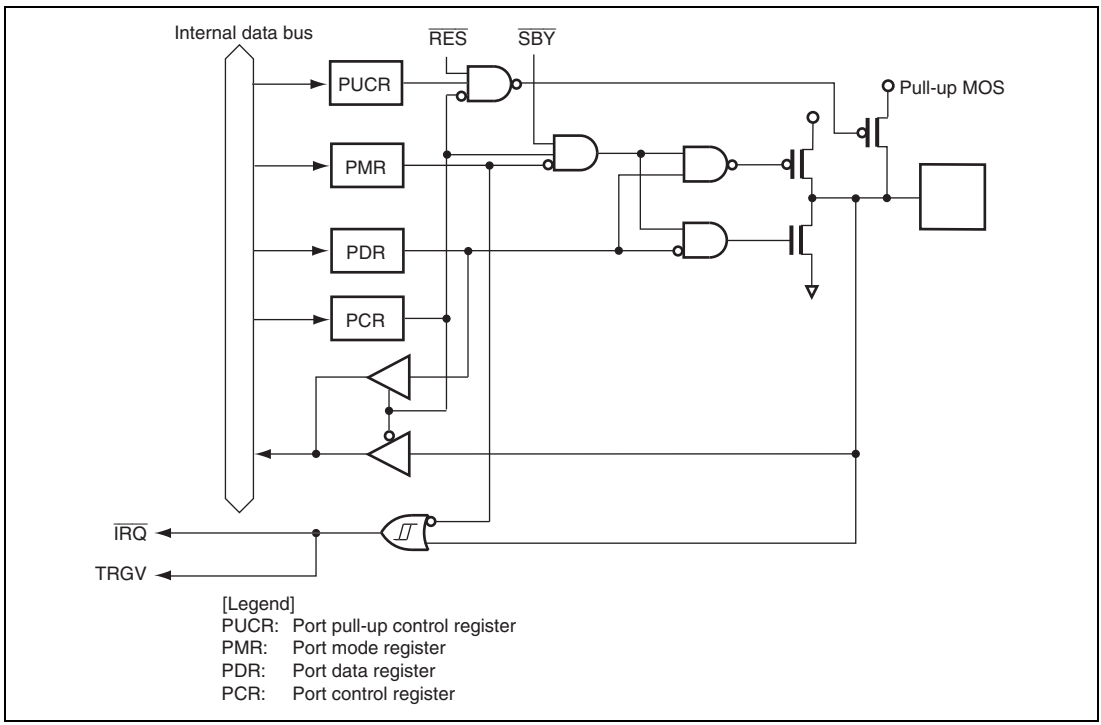


Figure B.1 Port 1 Block Diagram (P17)