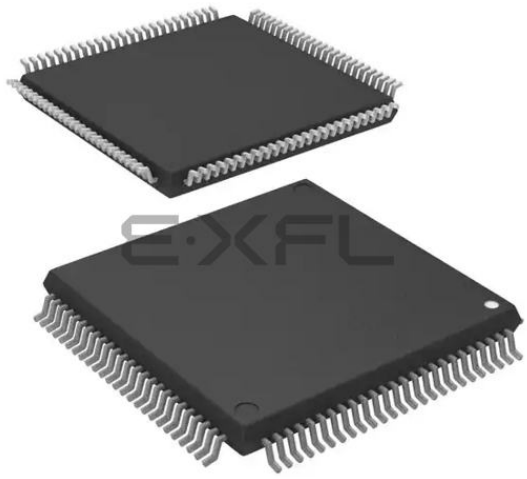

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b SAR; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36109ghv

6.4 Direct Transition

The CPU can execute programs in two modes: active and subactive modes. A direct transition is a transition between these two modes without stopping program execution. A direct transition can be made by executing the SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition also enables operating frequency modification in active or subactive mode. After the mode transition, direct transition interrupt exception handling starts.

If the direct transition interrupt is disabled in interrupt enable register 1, a transition is made instead to sleep or subsleep mode. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep or subsleep mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.

6.4.1 Direct Transition from Active Mode to Subactive Mode

The time from the start of the SLEEP instruction execution to the end of the interrupt exception handling (the direct transition time) is calculated by equation (1).

Direct transition time = {(number of SLEEP instruction execution cycles) + (number of internal clock cycles)}× (tcyc before transition) + (number of interrupt exception handling cycles) × (tsubcyc after transition) …. (1)

Example 1: Case when the CPU operating clock changes from ϕ_{osc} to $\phi_w/8$

$$\text{Direct transition time} = (2 + 1) \times t_{OSC} + 16 \times 8\ t_W = 3\ t_{OSC} + 128\ t_W$$

Example 2: Case when the system clock source is Rosc/4 and the division ratio is 16; the CPU operating clock changes from $\phi/16$ to $\phi_w/2$

$$\text{Direct transition time} = (2 + 1) \times 4\ t_{ROSC} \times 16 + 16 \times 2\ t_w = 192\ t_{ROSC} + 32\ t_w$$

[Legend]

t_{OSC}: OSC clock cycle time
t_{ROSC}: Period of oscillation of the on-chip oscillator
t_W: Watch clock cycle time
t_{cyc}: System clock (ϕ) cycle time
t_{subcyc}: Subclock (ϕ_{SUB}) cycle time

9.2.4 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P27 pin

Register	PCR2	
Bit Name	PCR27	Pin Function
Setting Value	0	P27 input pin
	1	P27 output pin

- P26 pin

Register	PCR2	
Bit Name	PCR26	Pin Function
Setting Value	0	P26 input pin
	1	P26 output pin

- P25 pin

Register	PCR2	
Bit Name	PCR25	Pin Function
Setting Value	0	P25 input pin
	1	P25 output pin

- P24 pin

Register	PCR2	
Bit Name	PCR24	Pin Function
Setting Value	0	P24 input pin
	1	P24 output pin

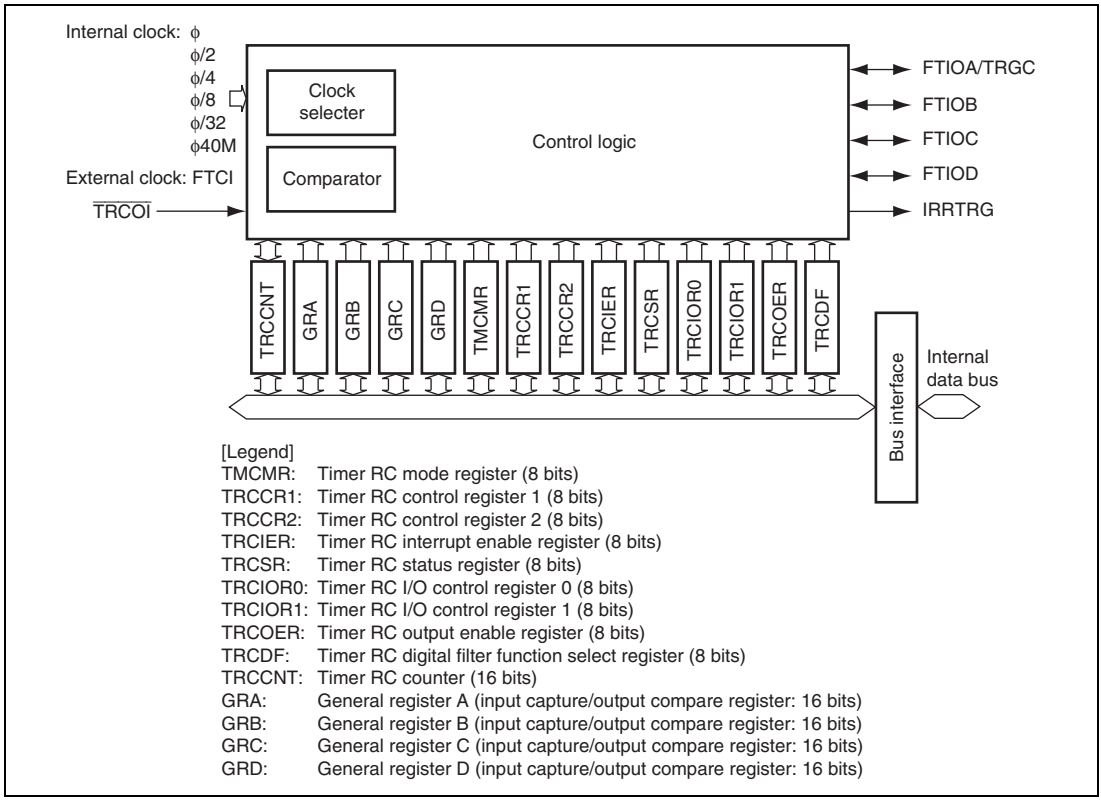

Figure 13.1 Timer RC Block Diagram

Figure 13.8 shows an example of buffer operation when GRA is set as an input-capture register and GRC is set as the buffer register for GRA. TRCCNT functions as a free-running counter and is captured at both rising and falling edges of the FTIOA signal. Due to the buffer operation, the GRA value is transferred to GRC on an input-capture A and the TRCCNT value is stored in GRA.

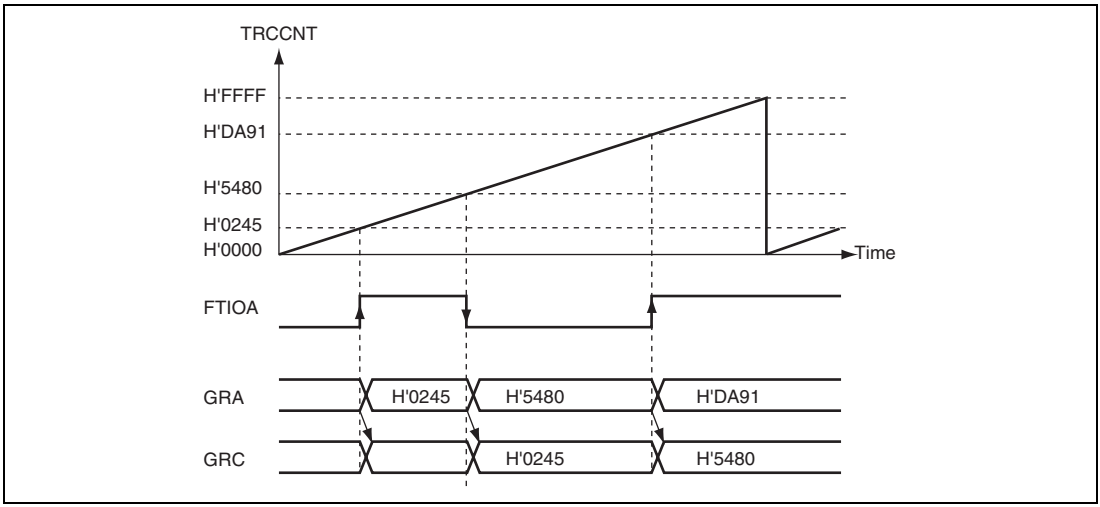

Figure 13.8 Buffer Operation Example (Input Capture)

13.4.3 PWM2 Mode Operation

In PWM2 mode, waveforms are output on the FTIOB pin when a compare match occurs on GRB or GRC. GRD functions as a buffer register for GRB by setting the BUFEB bit in TRCMR to 1. The output level of the FTIOB signal is specified by the TOB bit in TRCCR1. When TOB = 0, 1 is output on a compare match of GRC and 0 is output on a compare match of GRB. When TOB = 1, 0 is output on a compare match of GRC and 1 is output on a compare match of GRB.

Table 13.3 shows the correspondence between the pin configuration and GR registers and figure 13.14 is a block diagram of PWM2 mode.

Figures 13.15 and 13.16 show the GRD and GRB buffer operating timing in PWM2 mode.

In PWM2 mode, the value of GRD is transferred to GRB on a compare match of GRA and the counter is cleared. Note, however, that the counter is only cleared when the CCLR bit in TRCCR1 is set to 1. Moreover, when the trigger input is enabled by the TCEG1 and TCEG0 bits in TRCCR2, the value of GRD is transferred to GRB by the trigger signal and the counter is cleared. The input/output pins of timers which do not operate in PWM2 mode are only used as general I/O ports.

Table 13.3 Pin Configuration in PWM2 Mode and GR Registers

Pin Name	Input/Output	Compare Match Register	Buffer Register
FTIOA	I/O	Port/TRGC	Port/TRGC
FTIOB	Output	GRB	GRD
		GRC	—
FTIOC	I/O	Port	Port
FTIOD	I/O	Port	Port

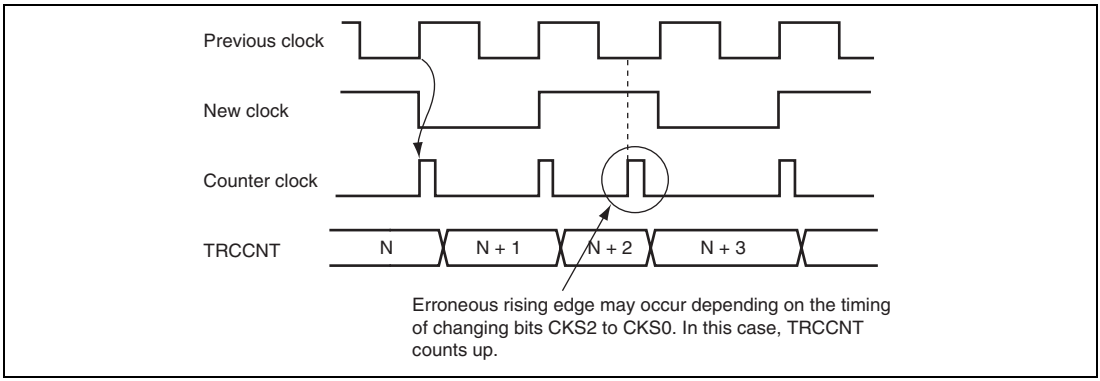

Figure 13.34 Internal Clock Switching and TRCCNT Operation

5. The TOA to TOD bits in TRCCR1 decide the value of the FTIO pin, which is output until the first compare match occurs. Once a compare match occurs and this compare match changes the values of FTIOA to FTIOD output, the values of the FTIOA to FTIOD pin output and the values read from the TOA to TOD bits may differ. Moreover, when the writing to TRCCR1 and the generation of the compare match A to D occur at the same timing, the writing to TRCCR1 has the priority. Thus, output change due to the compare match is not reflected to the FTIOA to FTIOD pins. Therefore, when bit manipulation instruction is used to write to TRCCR1, the values of the FTIOA to FTIOD pin output may result in an unexpected result. When TRCCR1 is to be written to while compare match is operating, stop the counter once before accessing to TRCCR1, read the port 8 state to reflect the values of FTIOA to FTIOD output, to TOA to TOD, and then restart the counter. Figure 13.35 shows an example when the compare match and the bit manipulation instruction to TRCCR1 occur at the same timing.

- Timer RD counter_1 (TRDCNT_1)
- General register A_1 (GRA_1)
- General register B_1 (GRB_1)
- General register C_1 (GRC_1)
- General register D_1 (GRD_1)

14.3.1 Timer RD Start Register (TRDSTR)

TRDSTR selects the operation/stop for the TRDCNT counter. Use a MOV instruction to modify this register.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1, and cannot be modified.
3	CSTPN1	1	R/W	Channel 1 Counter Stop 0: Counting is stopped on a compare match of TRDCNT_1 and GRA_1 1: Counting is continued on a compare match of TRDCNT_1 and GRA_1 Set this bit to 1 to restart counting after the counting has been stopped on a compare match.
2	CSTPN0	1	R/W	Channel 0 Counter Stop 0: Counting is stopped on a compare match of TRDCNT_0 and GRA_0 1: Counting is continued on a compare match of TRDCNT_0 and GRA_0 Set this bit to 1 to restart counting after the counting has been stopped on a compare match.

14.3.8 Timer RD Counter (TRDCNT)

Timer RD has two TRDCNT counters (TRDCNT_0 and TRDCNT_1), one for each channel. The TRDCNT counters are 16-bit readable/writable registers that increment/decrement according to input clocks. Input clocks can be selected by bits TPSC2 to TPSC0 in TRDCR. TRDCNT_0 and TRDCNT_1 increment/decrement in complementary PWM mode, while they only increment in other modes.

The TRDCNT counters are initialized to H'0000 by compare matches with corresponding GRA, GRB, GRC, or GRD, or input captures to GRA, GRB, GRC, or GRD (counter clearing function). When the TRDCNT counters overflow, an OVF flag in TRDSR for the corresponding channel is set to 1. When TRDCNT_1 underflows, an UDF flag in TRDSR is set to 1. The TRDCNT counters cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit. TRDCNT is initialized to H'0000 by a reset.

14.3.9 General Registers A, B, C, and D (GRA, GRB, GRC, and GRD)

GR are 16-bit registers. Timer RD has eight general registers (GR), four for each channel. The GR registers are dual function 16-bit readable/writable registers, functioning as either output compare or input capture registers. Functions can be switched by TRDIORA and TRDIORC.

The values in GR and TRDCNT are constantly compared with each other when the GR registers are used as output compare registers. When the both values match, the IMFA to IMFD flags in TSR are set to 1. Compare match outputs can be selected by TRDIORA and TRDIORC.

When the GR registers are used as input capture registers, the TRDCNT value is stored after detecting external signals. At this point, IMFA to IMFD flags in the corresponding TRDSR are set to 1. Detection edges for input capture signals can be selected by TRDIORA and TRDIORC.

When PWM mode, complementary PWM mode, or reset synchronous PWM mode is selected, the values in TRDIORA and TRDIORC are ignored. Upon reset, the GR registers are set as output compare registers (no output) and initialized to H'FFFF. The GR registers cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit.

14.3.10 Timer RD Control Register (TRDCR)

TRDCR selects a TRDCNT counter clock, an edge when an external clock is selected, and counter clearing sources. Timer RD has a total of two TRDCR registers, one for each channel.

Bit	Bit Name	Initial Value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	000: Disables TRDCNT clearing
5	CCLR0	0	R/W	001: Clears TRDCNT by GRA compare match/input capture*[1]
				010: Clears TRDCNT by GRB compare match/input capture*[1]
				011: Synchronization clear; Clears TRDCNT in synchronous with counter clearing of the other channel's timer*[2]
				100: Disables TRDCNT clearing
				101: Clears TRDCNT by GRC compare match/input capture*[1]
				110: Clears TRDCNT by GRD compare match/input capture*[1]
				111: Synchronization clear; Clears TRDCNT in synchronous with counter clearing of the other channel's timer*[2]
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	00: Count at rising edge
				01: Count at falling edge
				1X: Count at both edges

Figure 14.26 shows another example of operation in PWM mode. The output signals go to 0 and TRDCNT is reset at compare match A, and the output signals go to 1 at compare match B, C, and D (TOB, TOC, and TOD = 0, POLB, POLC, and POLD = 1).

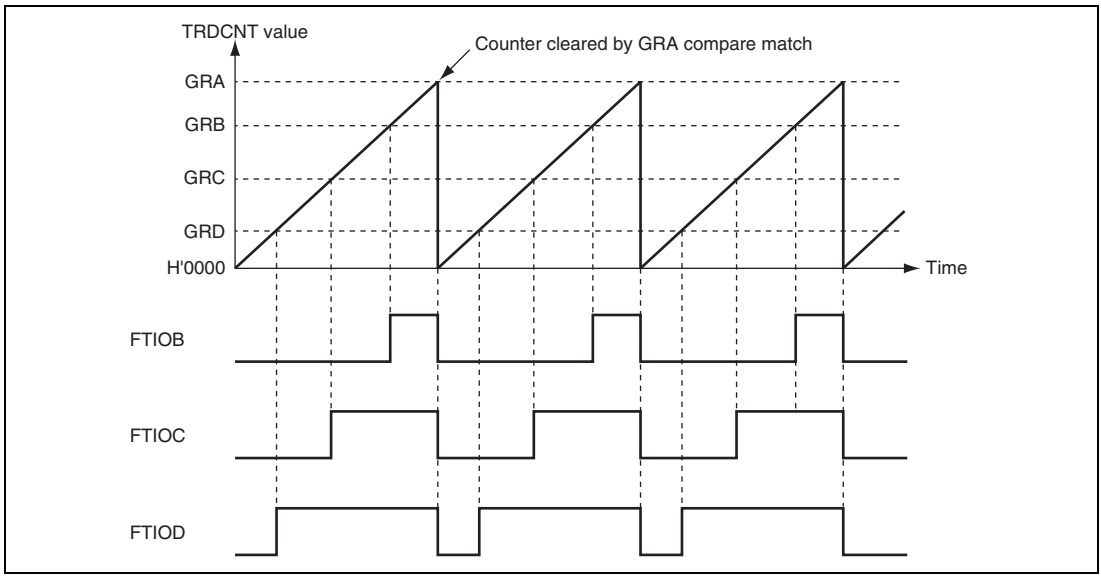

Figure 14.26 Example of PWM Mode Operation (2)

14.4.9 Buffer Operation

Buffer operation differs depending on whether GR has been designated for an input capture register or an output compare register, or in reset synchronous PWM mode or complementary PWM mode.

Table 14.10 shows the register combinations used in buffer operation.

Table 14.10 Register Combinations in Buffer Operation

General Register (GR)	Buffer Register
GRA	GRC
GRB	GRD

(1) When GR is an Output Compare Register

When a compare match occurs, the value in GR of the corresponding channel is transferred to the general register.

This operation is illustrated in figure 14.41.

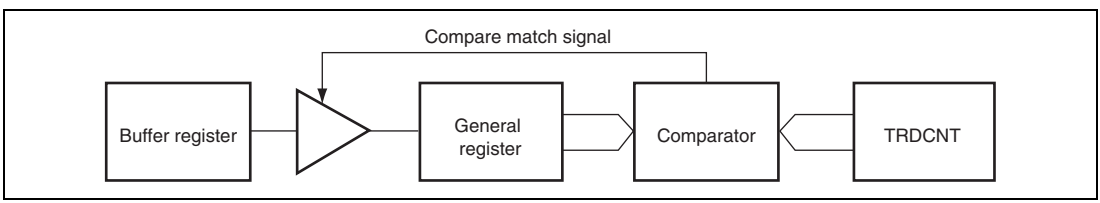

Figure 14.41 Compare Match Buffer Operation

Clock synchronous mode:

- Data length: 8 bits
- Receive error detection: Overrun errors

Table 17.1 Channel Configuration

Channel	Abbreviation	Pin	Register	Register Address	Noise Canceller
Channel 1	SCI3*[2]	SCK3 RXD TXD	SMR	H'FFFFA8	None
			BRR	H'FFFFA9	
			SCR3	H'FFFFAA	
			TDR	H'FFFFAB	
			SSR	H'FFFFAC	
			RDR	H'FFFFAD	
			RSR	—	
			TSR	—	
Channel 2	SCI3_2	SCK3_2 RXD_2 TXD_2	SMR_2	H'FFF740	None
			BRR_2	H'FFF741	
			SCR3_2	H'FFF742	
			TDR_2	H'FFF743	
			SSR_2	H'FFF744	
			RDR_2	H'FFF745	
			RSR_2	—	
			TSR_2	—	
Channel 3	SCI3_3	SCK3_3 RXD_3 TXD_3	SMR_3	H'FFF600	Yes
			BRR_3	H'FFF601	
			SCR3_3	H'FFF602	
			TDR_3	H'FFF603	
			SSR_3	H'FFF604	
			RDR_3	H'FFF605	
			RSR_3	—	
			TSR_3	—	
			SMCR_3*[1]	H'FFF608	

17.8.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 17.19. Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ (0.5 - \frac{1}{2N}) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%)$$

... Formula (1)

[Legend]

N: Ratio of bit rate to clock (N = 16)

D: Clock duty (D = 0.5 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

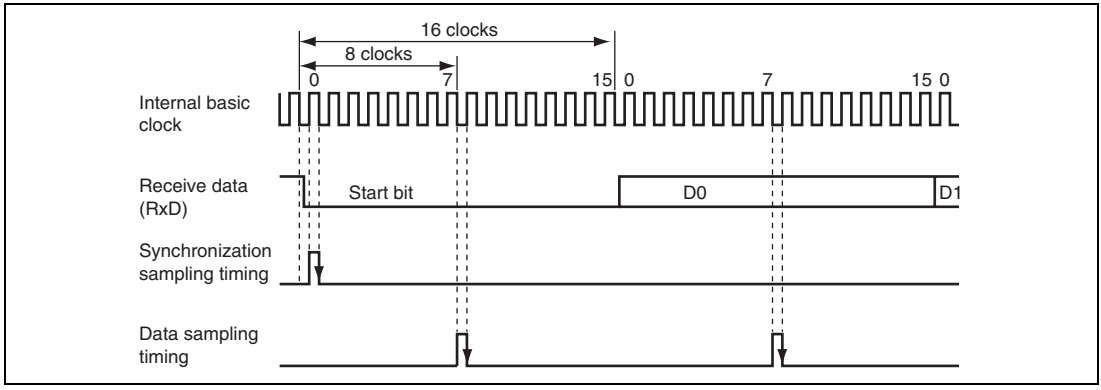

Figure 17.19 Receive Data Sampling Timing in Asynchronous Mode

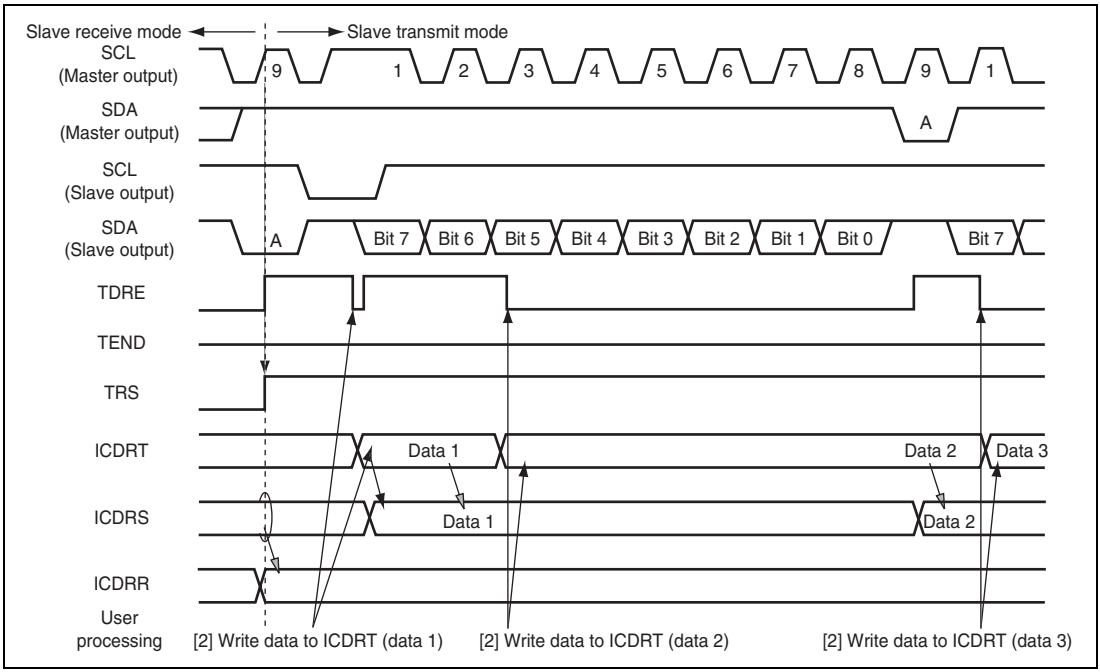

Figure 18.9 Slave Transmit Mode Operation Timing (1)

Section 22 List of Registers

The register list gives information on the on-chip I/O register addresses, how the register bits are configured, and the register states in each operating mode. The information is given as shown below.

1. Register addresses (address order)
- Registers are listed from the lower allocation addresses.
- Registers are classified by functional modules.
- The data bus width is indicated.
- The number of access states is indicated.

2. Register bits
- Bit configurations of the registers are described in the same order as the register addresses.
- Reserved bits are indicated by — in the bit name column.
- When registers consist of 16 bits, bits are described from the MSB side.

3. Register states in each operating mode
- Register states are described in the same order as the register addresses.
- The register states described here are for the basic operating modes. If there is a specific reset for an on-chip peripheral module, refer to the section on that on-chip peripheral module.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Output high voltage	V_{OH}	P10 to P12, P14 to P17, P20 to P27, P30 to P37, P50 to P55, P70 to P72, P74 to P77, P85 to P87, PC0 to PC3, PD0 to PD7, PE0 to PE7, PH0 to PH7, PJ0, PJ1	V_{CC} = 4.0 to 5.5 V $-I_{OH}$ = 5.0 mA	V_{CC} – 1.0	—	—	V	
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.5	—	—	V	
		PG0 to PG7	$-I_{OH}$ = 0.1 mA	AV_{CC} – 0.5	—	—	V	
		P56, P57	4.0 V ≤ V_{CC} ≤ 5.5 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.5	—	—	V	
			3.0 V ≤ V_{CC} < 4.0 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.2	—	—	V	
Output low voltage	V_{OL}	P10 to P12, P14 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P72, P74 to P77, P85 to P87, PC0 to PC3, PH0 to PH3, PJ0, PJ1	V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.6	V	
			I_{OL} = 0.2 mA	—	—	0.4	V	
		PG0 to PG7	I_{OL} = 0.2 mA	—	—	0.4	V	
		PD0 to PD7, PE0 to PE7, PH4 to PH7	V_{CC} = 4.0 to 5.5 V I_{OL} = 20.0 mA	—	—	1.5	V	
			V_{CC} = 4.0 to 5.5 V I_{OL} = 10.0 mA	—	—	1.0	V	
			V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.4	V	
			I_{OL} = 0.4 mA	—	—	0.4	V	
		SCL, SDA	V_{CC} = 4.0 to 5.5 V I_{OL} = 6.0 mA	—	—	0.6	V	
			I_{OL} = 3.0 mA	—	—	0.4	V	

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	|		I	H	N	Z	V	C	Normal	Advanced
BLD	BLD #xx:3, @ERd	B			4							(#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
	BLD #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BILD	BILD #xx:3, Rd	B		2								¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BILD #xx:3, @ERd	B			4							¬ (#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
	BILD #xx:3, @aa:8	B						4				¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BST	BST #xx:3, Rd	B		2								C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
	BST #xx:3, @ERd	B			4							C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
	BST #xx:3, @aa:8	B						4				C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BIST	BIST #xx:3, Rd	B		2								¬ C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
	BIST #xx:3, @ERd	B			4							¬ C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
	BIST #xx:3, @aa:8	B						4				¬ C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BAND	BAND #xx:3, Rd	B		2								C∧(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BAND #xx:3, @ERd	B			4							C∧(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BAND #xx:3, @aa:8	B						4				C∧(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIAND	BIAND #xx:3, Rd	B		2								C∧ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BIAND #xx:3, @ERd	B			4							C∧ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BIAND #xx:3, @aa:8	B						4				C∧ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BOR	BOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BOR #xx:3, @ERd	B			4							C∨(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIOR	BIOR #xx:3, Rd	B		2								C∨ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BIOR #xx:3, @ERd	B			4							C∨ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BIOR #xx:3, @aa:8	B						4				C∨ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BXOR	BXOR #xx:3, Rd	B		2								C⊕(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BXOR #xx:3, @ERd	B			4							C⊕(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BXOR #xx:3, @aa:8	B						4				C⊕(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIXOR	BIXOR #xx:3, Rd	B		2								C⊕ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BIXOR #xx:3, @ERd	B			4							C⊕ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BIXOR #xx:3, @aa:8	B						4				C⊕ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	

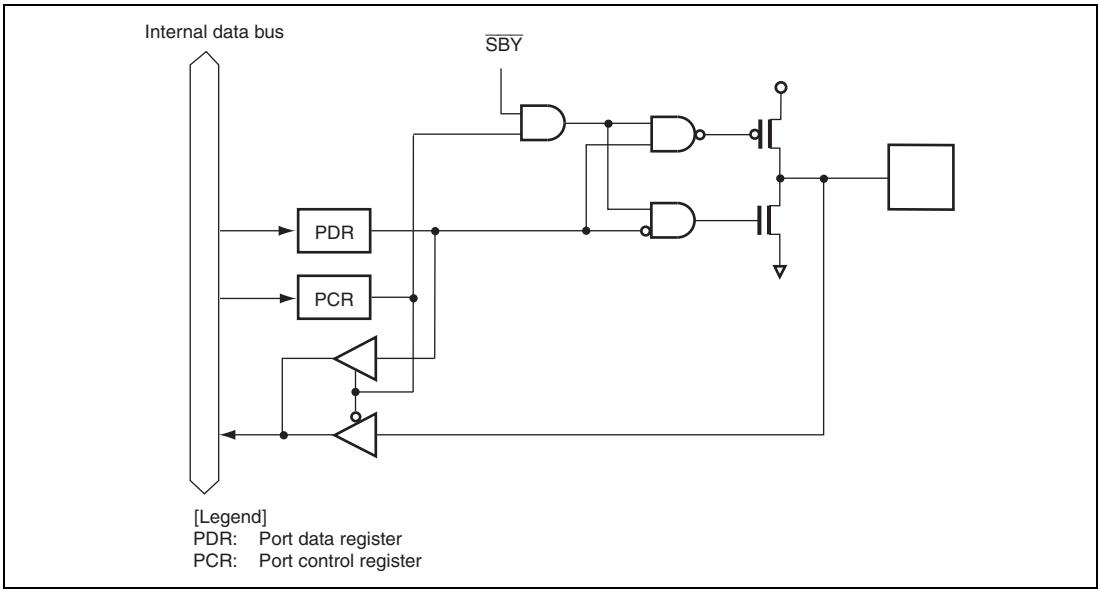

Figure B.14 Port 7 Block Diagram (P77)

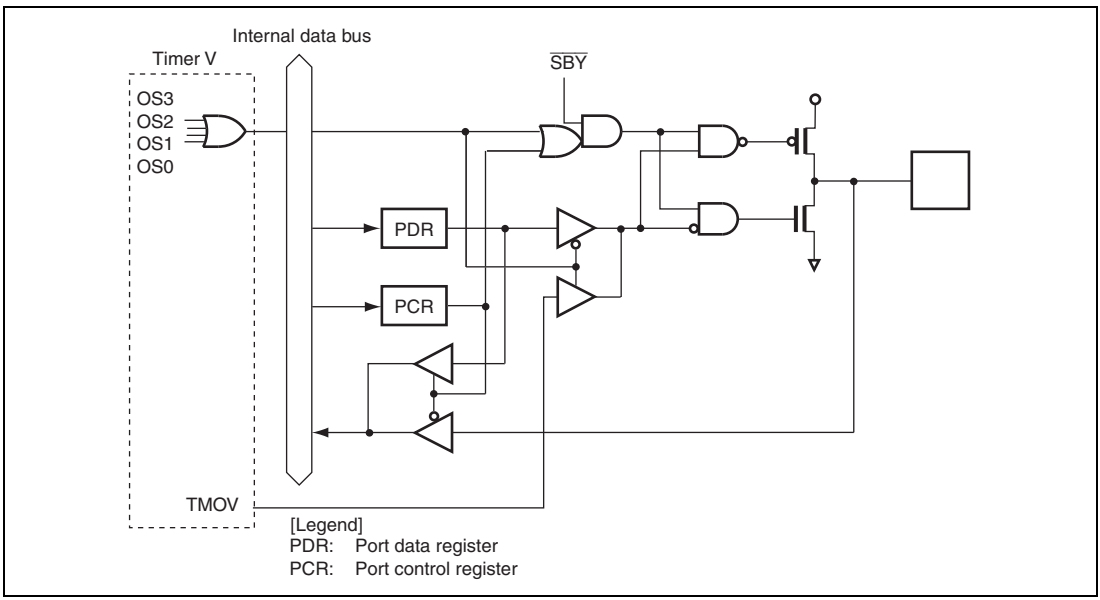

Figure B.15 Port 7 Block Diagram (P76)

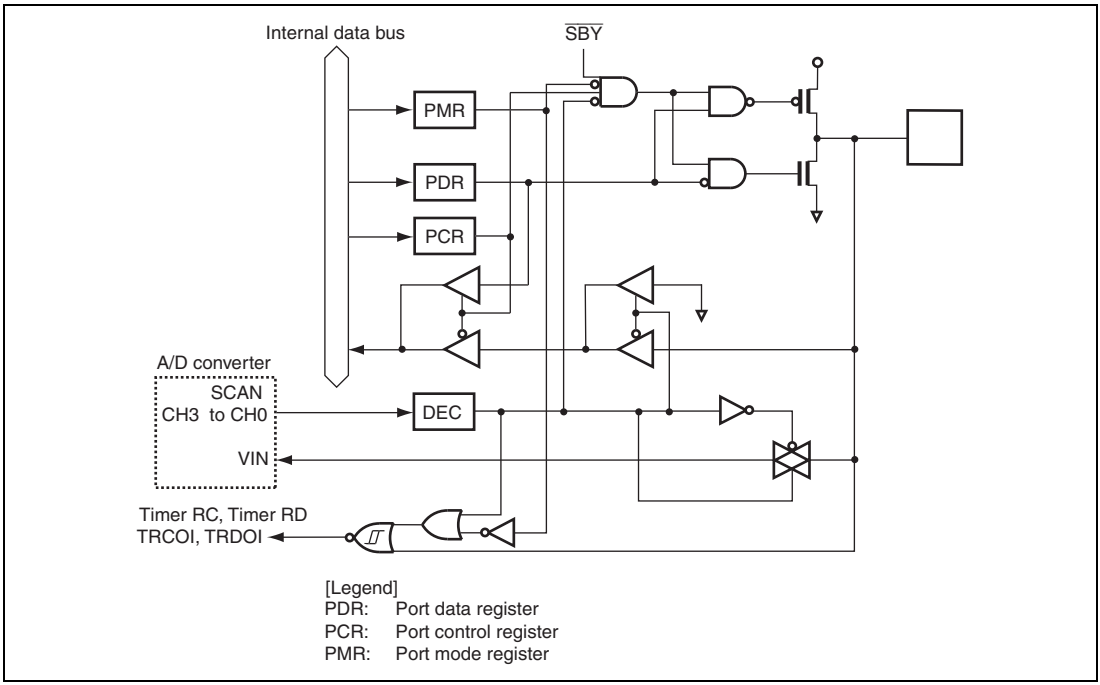

Figure B.26 Port G Block Diagram (PG7, PG6, PG5)

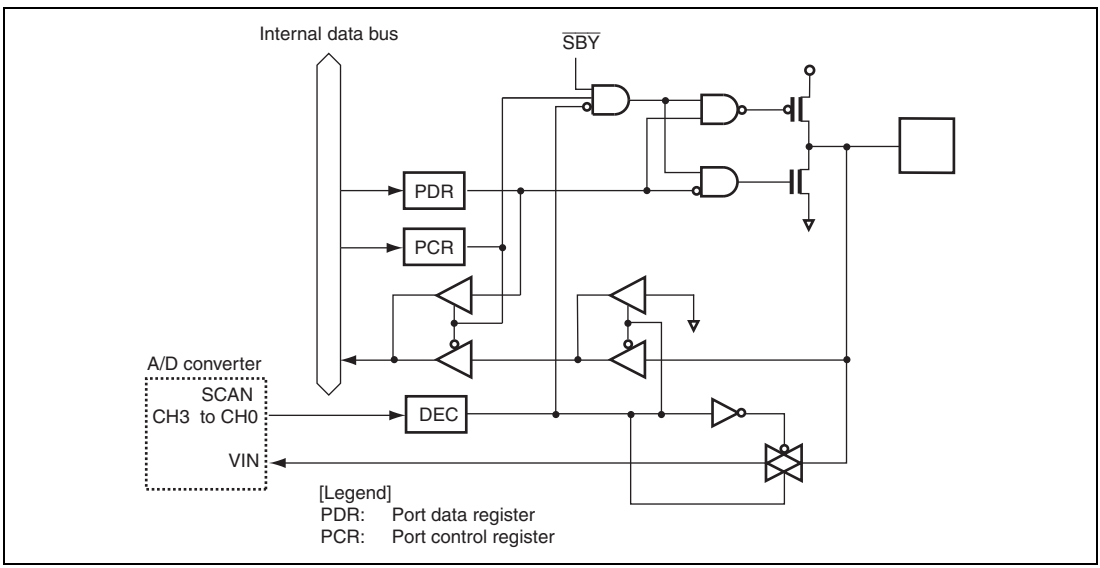

Figure B.27 Port G Block Diagram (PG4, PG3, PG2, PG1, PG0)

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