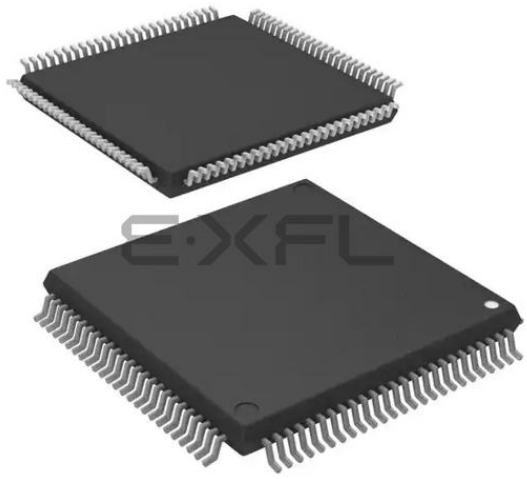

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36109hv

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Section 1 Overview

1.1 Features

- High-speed H8/300H central processing unit with an internal 16-bit architecture
  Upward-compatible with H8/300 CPU on an object level
  Sixteen 16-bit general registers
  62 basic instructions
- Various peripheral functions
  RTC (can be used as a free running counter)
  Timer B1 (8-bit timer)
  Timer V (8-bit timer)
  Timer RC (16-bit timer)
  Timer RD (16-bit timer)
  14-bit PWM
  Watchdog timer
  SCI3 (Asynchronous or clock synchronous serial communication interface)
  I^2C bus interface 2 (conforms to the I^2C bus interface format that is advocated by Philips Electronics)
  10-bit A/D converter
  POR/LVD (Power-on reset and low-voltage detection circuit) (optional)
- On-chip memory

		Model				
Product Classification		Standard Version	On-Chip Power-On Reset and Low-Voltage Detection Circuit Version	ROM	RAM	Remark
Flash memory version (F-ZTAT™ version)	H8/36109F	HD64F36109	HD64F36109G	128 kbytes	5 kbytes	

Note: F-ZTAT™ is a trademark of Renesas Technology Corp.

2.5 Addressing Modes and Effective Address Calculation

2.5.1 Addressing Modes

The H8/300H CPU supports the eight addressing modes listed in table 2.10. Each instruction uses a subset of these addressing modes. Addressing modes that can be used differ depending on the instruction. For details, refer to appendix A.4, Combinations of Instructions and Addressing Modes.

Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit-manipulation instructions use register direct, register indirect, or the absolute addressing mode (@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

(1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

(2) Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn), the lower 24 bits of which contain the address of the operand on memory.

When the address break is specified in the data read cycle

Register setting
- ABRKCR = H'A0
- BAR = H'025A

Program

```
  0258  NOP
  025A  NOP
* 025C  MOV.W @H'025A,R0
  0260  NOP
  0262  NOP
    :     :
```

Underline indicates the address to be stacked.

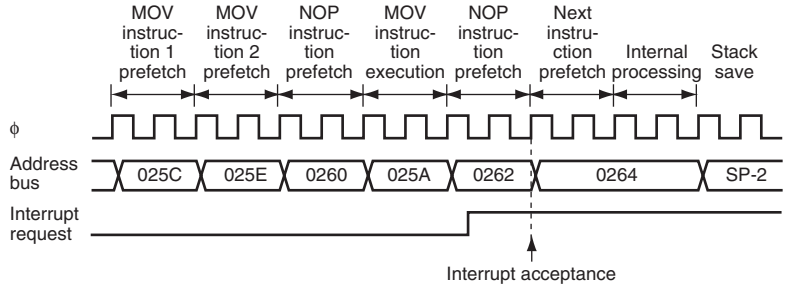


Figure 4.2 Address Break Interrupt Operation Example (2)

5.2.2 RC Trimming Data Protect Register (RCTRMDPR)

RCTRMDPR controls RCTRMDPR itself and writing to RCTRMDR. Use the MOV instruction to rewrite this register. Bit manipulation instruction cannot change the settings.

Bit	Bit Name	Initial Value	R/W	Description
7	WRI	1	W	Write Inhibit Only when writing 0 to this bit, this register can be written to. This bit is always read as 1.
6	PRWE	0	R/W	Protect Information Write Enable Bits 5 and 4 can be written to when this bit is set to 1. [Setting condition] • When writing 0 to the WRI bit and writing 1 to the PRWE bit [Clearing conditions] • Reset • When writing 0 to the WRI bit and writing 0 to the PRWE bit
5	LOCKDW	0	R/W	Trimming Data Register Lock Down The RC trimming data register (RCTRMDR) cannot be written to when this bit is set to 1. Once this bit is set to 1, this register cannot be written to until a reset is input even if 0 is written to this bit. [Setting condition] • When writing 0 to the WRI bit and writing 1 to the TRMDRWE bit while the PRWE bit is 1. [Clearing condition] • Reset

Section 9 I/O Ports

This LSI has seventy-nine general I/O ports and eight general input-only ports. Twenty ports are large current ports, which can drive 20 mA ($@V_{OL}$ = 1.5 V) when a low level signal is output. Any of these ports can become an input port immediately after a reset. They can also be used as I/O pins of the on-chip peripheral modules or external interrupt input pins, and these functions can be switched depending on the register settings. The registers for selecting these functions can be divided into two types: those included in I/O ports and those included in each on-chip peripheral module. General I/O ports are comprised of the port control register for controlling inputs/outputs and the port data register for storing output data and can select inputs/outputs in bit units.

For functions in each port, see appendix B.1, I/O Port Block Diagrams. For the execution of bit-manipulation instructions to the port control register and port data register, see section 2.8.3, Bit Manipulation Instruction.

9.1 Port 1

Port 1 is a general I/O port also functioning as IRQ interrupt input pins, an RTC output pin, a 14-bit PWM output pin, a timer B1 input pin, and a timer V input pin. Figure 9.1 shows its pin configuration.

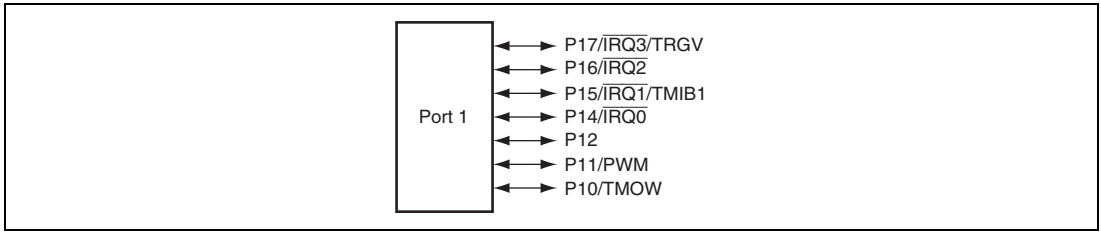


Figure 9.1 Port 1 Pin Configuration

Port 1 has the following registers.

- Port mode register 1 (PMR1)
- Port control register 1 (PCR1)
- Port data register 1 (PDR1)
- Port pull-up control register 1 (PUCR1)

- P30 pin

Register	PCR3	
Bit Name	**PCR30**	**Pin Function**
Setting Value	0	P30 input pin
	1	P30 output pin

9.4 Port 5

Port 5 is a general I/O port also functioning as an I^2C bus interface I/O pin and a wakeup interrupt input pin. Each pin of port 5 is shown in figure 9.4. The register setting of the I^2C bus interface has priority for functions of the pins P57/SCL and P56/SDA. Since the output buffer for pins P56 and P57 has the NMOS push-pull structure, it differs from an output buffer with the CMOS structure in the high-level output characteristics (see section 23, Electrical Characteristics).

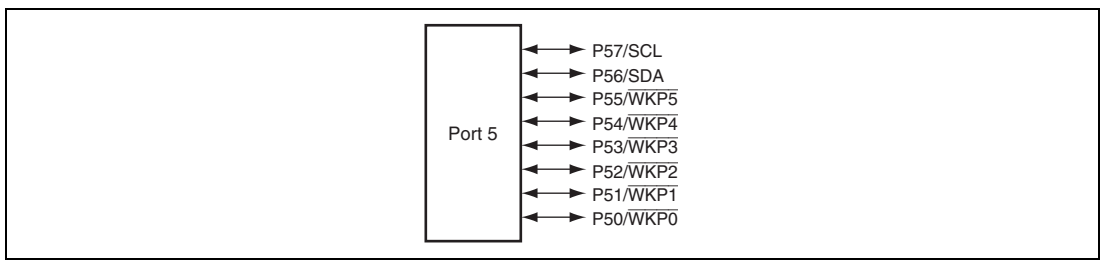


Figure 9.4 Port 5 Pin Configuration

Port 5 has the following registers.

- Port mode register 5 (PMR5)
- Port control register 5 (PCR5)
- Port data register 5 (PDR5)
- Port pull-up control register 5 (PUCR5)

10.4.3 Data Reading Procedure

When the seconds, minutes, hours, or day-of-week datum is updated while time data is being read, the data obtained may not be correct, and so the time data must be read again. Figure 10.4 shows an example in which correct data is not obtained. In this example, since only RSECDR is read after data update, about 1-minute inconsistency occurs.

To avoid reading in this timing, the following processing must be performed.

1. Check the setting of the BSY bit, and when the BSY bit changes from 1 to 0, read from the second, minute, hour, and day-of-week registers. When about 62.5 ms is passed after the BSY bit is set to 1, the registers are updated, and the BSY bit is cleared to 0.
2. Making use of interrupts, read from the second, minute, hour, and day-of week registers after the IRRTA flag in IRR1 is set to 1 and the BSY bit is confirmed to be 0.
3. Read from the second, minute, hour, and day-of week registers twice in a row, and if there is no change in the read data, the read data is used.

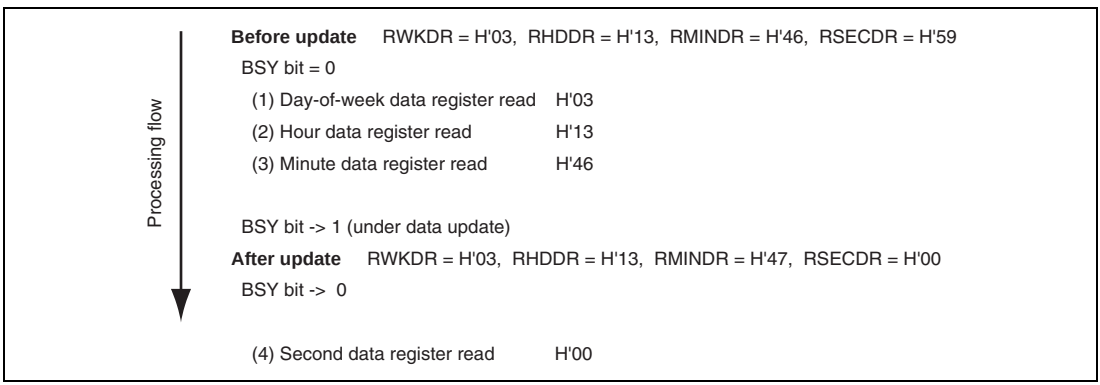


Figure 10.4 Example: Reading of Inaccurate Time Data

Bit	Bit Name	Initial Value	R/W	Description
3	—	1	—	Reserved 0 should not be written to this bit.
2	IOA2	0	R/W	I/O Control A2 Selects the GRA function. 0: GRA functions as an output compare register 1: GRA functions as an input capture register
1	IOA1	0	R/W	I/O Control A1 and A0
0	IOA0	0	R/W	When IOA2 = 0, 00: No output at compare match 01: 0 output to the FTIOA pin at GRA compare match 10: 1 output to the FTIOA pin at GRA compare match 11: Output toggles to the FTIOA pin at GRA compare match When IOA2 = 1, 00: Input capture to GRA at rising edge at the FTIOA pin 01: Input capture to GRA at falling edge at the FTIOA pin 1X: Input capture to GRA at rising and falling edges at the FTIOA pin

[Legend]

X: Don't care.

Note: When a GR register functions as a buffer register for a paired GR register, the settings in the IOA2 and IOB2 bits in TRDIORA and the IOC2 and IOD2 bits in TRDIORC of both registers should be the same.

16.3 Register Descriptions

The 14-bit PWM has the following registers.

- PWM control register (PWCR)
- PWM data register U (PWDRU)
- PWM data register L (PWDRL)

16.3.1 PWM Control Register (PWCR)

PWCR selects the conversion period.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved
6	—	1	—	These bits are always read as 1, and cannot be modified.
5	—	1	—	
4	—	1	—	
3	—	1	—	
2	—	1	—	
1	—	1	—	
0	PWCR0	0	R/W	Clock Select 0: The input clock is $\phi/2$ ($t\phi = 2/\phi$) — The conversion period is $16384/\phi$, with a minimum modulation width of $1/\phi$ 1: The input clock is $\phi/4$ ($t\phi = 4/\phi$) — The conversion period is $32768/\phi$, with a minimum modulation width of $2/\phi$

[Legend] $t\phi$: Period of PWM clock input

17.4 Operation in Asynchronous Mode

Figure 17.2 shows the general format for asynchronous serial communication. One character (or frame) consists of a start bit (low level), followed by data (in LSB-first order), a parity bit (high or low level), and finally stop bits (high level). Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

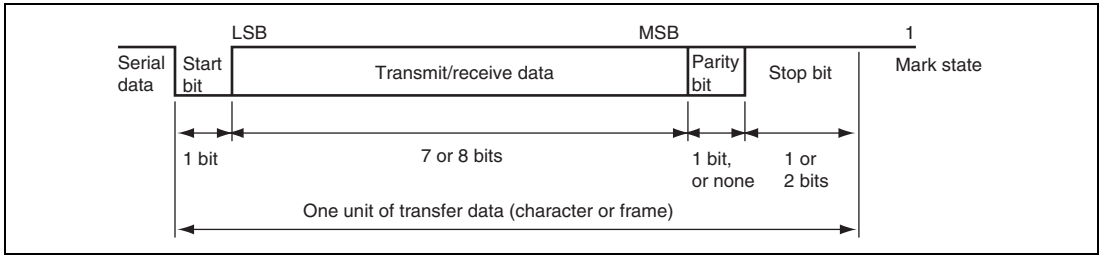


Figure 17.2 Data Format in Asynchronous Communication

17.4.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK3 pin can be selected as the SCI3's serial clock, according to the setting of the COM bit in SMR and the CKE0 and CKE1 bits in SCR3. When an external clock is input at the SCK3 pin, the clock frequency should be 16 times the bit rate used.

When the SCI3 is operated on an internal clock, the clock can be output from the SCK3 pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 17.3.

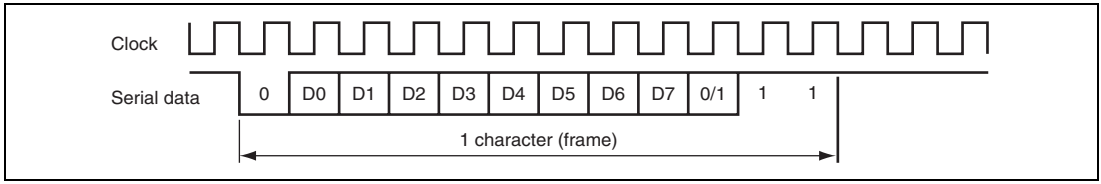
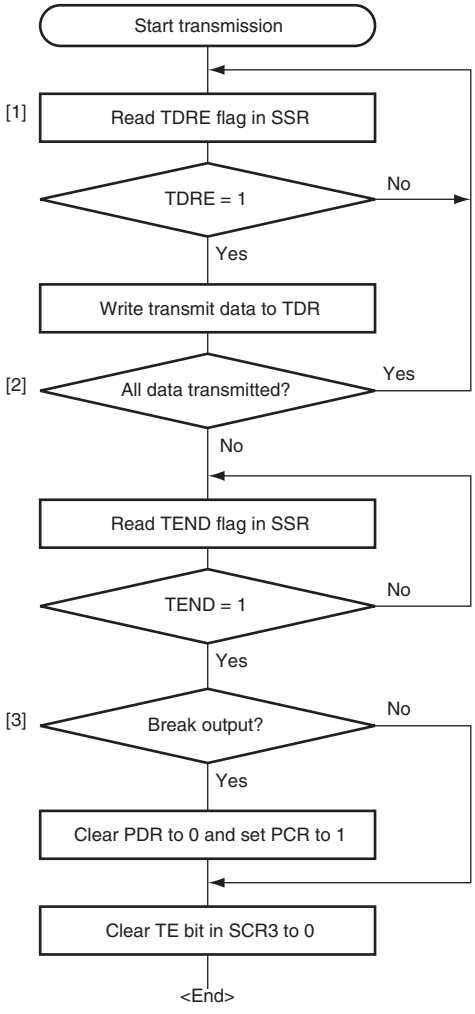


Figure 17.3 Relationship between Output Clock and Transfer Data Phase (Asynchronous Mode)(Example with 8-Bit Data, Parity, Two Stop Bits)



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automaticaly cleared to 0.

[2] To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automaticaly cleared to 0.

[3] To output a break in serial transmission, after setting PCR to 1 and PDR to 0, clear TxD in PMR1 to 0, then clear the TE bit in SCR3 to 0.

Figure 17.6 Sample Serial Transmission Data Flowchart (Asynchronous Mode)

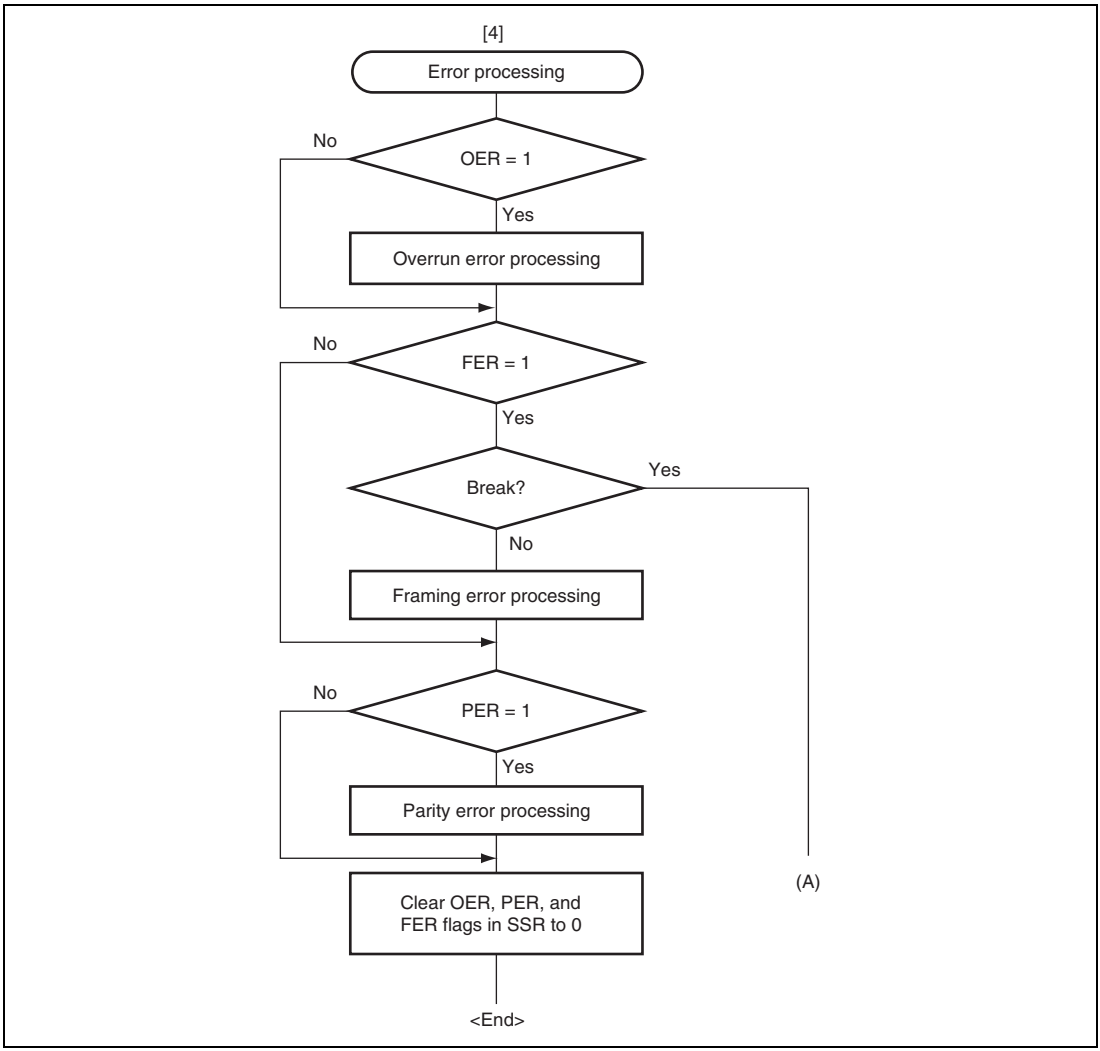


Figure 17.8 Sample Serial Reception Data Flowchart (Asynchronous Mode) (2)

17.5 Operation in Clock Synchronous Mode

Figure 17.9 shows the general format for clock synchronous communication. In clock synchronous mode, data is transmitted or received synchronous with clock pulses. A single character in the transmit data consists of the 8-bit data starting from the LSB. In clock synchronous serial communication, data on the transmission line is output from one falling edge of the synchronization clock to the next. In clock synchronous mode, the SCI3 receives data in synchronous with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the MSB state. In clock synchronous mode, no parity or multiprocessor bit is added. Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex communication through the use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

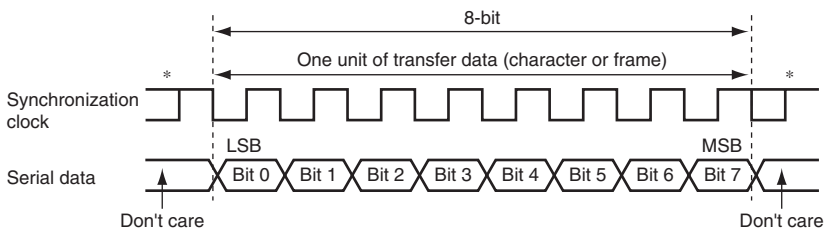


Figure 17.9 Data Format in Clock Synchronous Communication

17.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK3 pin can be selected, according to the setting of the COM bit in SMR and CKE0 and CKE1 bits in SCR3. When the SCI3 is operated on an internal clock, the synchronization clock is output from the SCK3 pin. Eight synchronization clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

17.5.2 SCI3 Initialization

Before transmitting and receiving data, the SCI3 should be initialized as described in a sample flowchart in figure 17.4.

19.5 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 19.4).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001 (see figure 19.5).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111 (see figure 19.5).
- Nonlinearity error

  The deviation from the ideal A/D conversion characteristic as the voltage changes from zero to full scale. This does not include the offset error, full-scale error, or quantization error.
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
TRDFCR_23	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0	Timer RD (Channel 2 and 3 common)
TRDOER1_23	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0	
TRDOER2_23	PTO	—	—	—	—	—	—	—	
TRDOCR_23	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0	
TRCMR	CTS	—	BUFEB	BUFEA	PWM2	PWMD	PWMC	PWMB	Timer RC
TRCCR1	CCLR	CKS2	CKS1	CKS0	TOD	TOC	TOB	TOA	
TRCIER	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA	
TRCSR	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA	
TRCIOR0	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
TRCIOR1	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0	
TRCCR2	TCEG1	TCEG0	CSTP	—	—	—	—	—	
TRCDF	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA	
TRCOER	PTO	—	—	—	ED	EC	EB	EA	
RSECDR	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00	RTC
RMINDR	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00	
RHRDR	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00	
RWKDR	BSY	—	—	—	—	WK2	WK1	WK0	
RTCCR1	RUN	12/24	PM	RST	INT	—	—	—	
RTCCR2	—	—	FOIE	WKIE	DYIE	HRIE	MNIE	SEIE	
RTCCSR	—	RCS6	RCS5	—	RCS3	RCS2	RCS1	RCS0	
LVDCR	—	—	—	—	LVDSEL	—	LVDDE	LVDUE	LVD (optional)
LVDSR	—	—	—	—	—	—	LVDDF	LVDUF	
CKCSR	PMRJ1	PMRJ0	—	OSCSEL	CKSWIE	CKSWIF	—	CKSTA	Clock pulse generator
RCCR	RCSTP	FSEL	VCLSEL	—	—	—	RCPSC1	RCPSC0	On-chip oscillator
RCTRMDPR	WRI	PRWE	LOCKDW	TRMDRWE	—	—	—	—	
RCTRMDR	TRMD7	TRMD6	TRMD5	TRMD4	TRMD3	TRMD2	TRMD1	TRMD0	
ICRA	ICRA7	ICRA6	ICRA5	ICRA4	ICRA3	ICRA2	ICRA1	—	Interrupt
ICRB	—	ICRB6	ICRB5	ICRB4	—	—	—	—	
ICRC	ICRC7	—	—	ICRC4	—	ICRC2	ICRC1	ICRC0	
ICRD	ICRD7	ICRD6	ICRD5	ICRD4	ICRD3	—	—	—	

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
NEG	NEG.B Rd	B		2								0–Rd8 → Rd8	—	↕	↕	↕	↕	↕	2	
	NEG.W Rd	W		2								0–Rd16 → Rd16	—	↕	↕	↕	↕	↕	2	
	NEG.L ERd	L		2								0–ERd32 → ERd32	—	↕	↕	↕	↕	↕	2	
EXTU	EXTU.W Rd	W		2								0 → (<bits 15 to 8> of Rd16)	—	—	0	↕	0	—	2	
	EXTU.L ERd	L		2								0 → (<bits 31 to 16> of ERd32)	—	—	0	↕	0	—	2	
EXTS	EXTS.W Rd	W		2								(<bit 7> of Rd16) → (<bits 15 to 8> of Rd16)	—	—	↕	↕	0	—	2	
	EXTS.L ERd	L		2								(<bit 15> of ERd32) → (<bits 31 to 16> of ERd32)	—	—	↕	↕	0	—	2	

Item	Page	Revisions (See Manual for Details)
Table 23.2 DC Characteristics (1)	503, 505, 506	Added

Item	Test Condition	Values			Unit	Notes
		Min.	Typ.	Max.		
Output high voltage	3.0 V ≤ V_{CC} < 4.0 V $-I_{OH}$ = 0.1 mA	V_{CC} – 2.2	—	—	V	
Active mode supply current	Active mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	33.0	40.0	mA	*
	Active mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	15.0	—		* Reference value
	Active mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	6.0	7.5	mA	*
	Active mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	4.5	—		* Reference value
Sleep mode supply current	Sleep mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	22.0	30.0	mA	*
	Sleep mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	12.0	—		* Reference value
	Sleep mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	5.0	6.5	mA	*
	Sleep mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	4.5	—		* Reference value
Subactive mode supply current	V_{CC} = 3.0 V 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/2)	—	130	150	µA	* Optional
		—	50	70		*
	V_{CC} = 3.0 V 32-kHz crystal resonator not used (ϕ_{SUB} = ϕ_W/8)	—	100	—		Reference value Optional *
		—	40	—		*
Subsleep mode supply current	Subsleep mode 1 V_{CC} = 3.0 V 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/2)	—	110	140	µA	* Optional
		—	40	50		*
	Subsleep mode 2 V_{CC} = 3.0 V 32-kHz crystal resonator not used	—	110	135		* Optional
		—	—	6.0		*
Standby mode supply current	32-kHz crystal resonator not used	—	—	135	µA	* Optional
		—	—	5.0		*

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