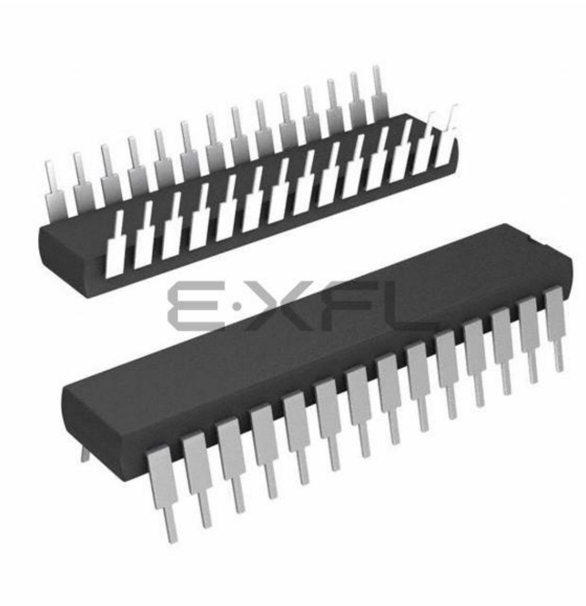
# Microchip Technology - PIC16C73A-04/SP Datasheet



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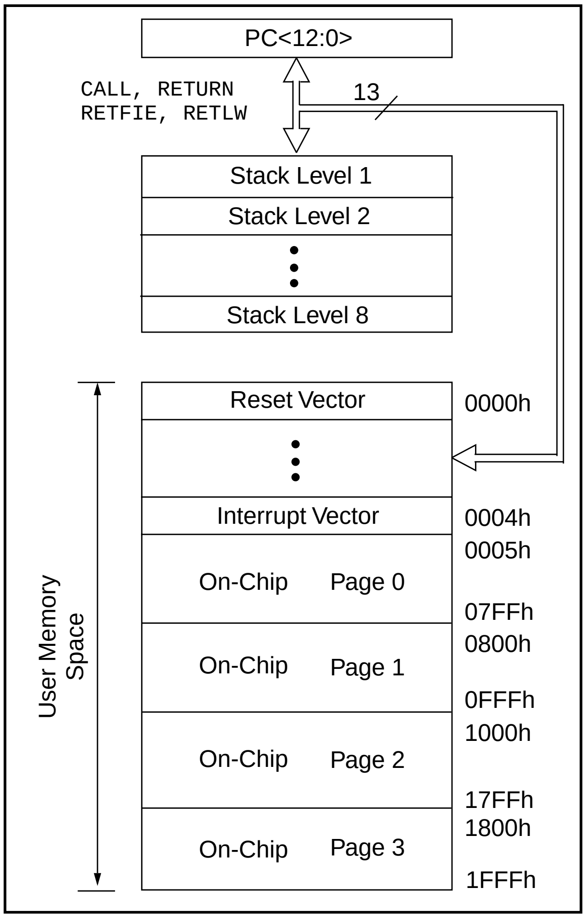
## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 192 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 6V |
| Data Converters | A/D 5x8b |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c73a-04-sp |

**FIGURE 4-3: PIC16C76/77 PROGRAM MEMORY MAP AND STACK**



## 4.2 Data Memory Organization

| Applicable Devices | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1:RP0 (STATUS<6:5>)
= 00 → Bank0
= 01 → Bank1
= 10 → Bank2
= 11 → Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some "high use" special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

### 4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

### 4.2.2.6 PIE2 REGISTER

| Applicable Devices | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

This register contains the individual enable bit for the CCP2 peripheral interrupt.

**FIGURE 4-14: PIE2 REGISTER (ADDRESS 8Dh)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | CCP2IE |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IE**: CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

## 11.4 I$^2$C™ Overview

This section provides an overview of the Inter-Integrated Circuit (I$^2$C) bus, with Section 11.5 discussing the operation of the SSP module in I$^2$C mode.

The I$^2$C bus is a two-wire serial interface developed by the Philips Corporation. The original specification, or standard mode, was for data transfers of up to 100 Kbps. The enhanced specification (fast mode) is also supported. This device will communicate with both standard and fast mode devices if attached to the same bus. The clock will determine the data rate.

The I$^2$C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the “master” which initiates transfer on the bus and generates the clock signals to permit that transfer, while the other device(s) acts as the “slave.” All portions of the slave protocol are implemented in the SSP module’s hardware, except general call support, while portions of the master protocol need to be addressed in the PIC16CXX software. Table 11-3 defines some of the I$^2$C bus terminology. For additional information on the I$^2$C interface specification, refer to the Philips document “*The I$^2$C bus and how to use it.*”#939839340011, which can be obtained from the Philips Corporation.

In the I$^2$C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to “talk” to. All devices “listen” to see if this is their address. Within this address, a bit specifies if the master wishes to read-from/write-to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of as operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I$^2$C bus is limited only by the maximum bus loading specification of 400 pF.

### 11.4.1 INITIATING AND TERMINATING DATA TRANSFER

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure 11-14 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

FIGURE 11-14: START AND STOP CONDITIONS

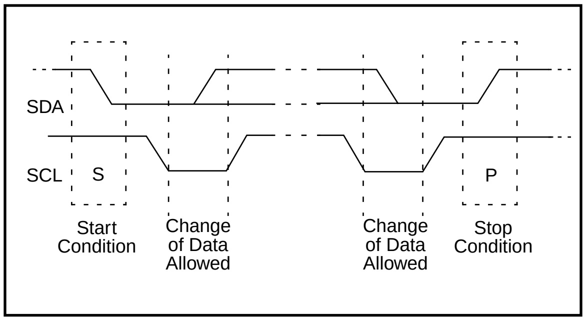


TABLE 11-3: I$^2$C BUS TERMINOLOGY

| Term | Description |
|---|---|
| Transmitter | The device that sends the data to the bus. |
| Receiver | The device that receives the data from the bus. |
| Master | The device which initiates the transfer, generates the clock and terminates the transfer. |
| Slave | The device addressed by a master. |
| Multi-master | More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message. |
| Arbitration | Procedure that ensures that only one of the master devices will control the bus. This ensure that the transfer data does not get corrupted. |
| Synchronization | Procedure where the clock signals of two or more devices are synchronized. |

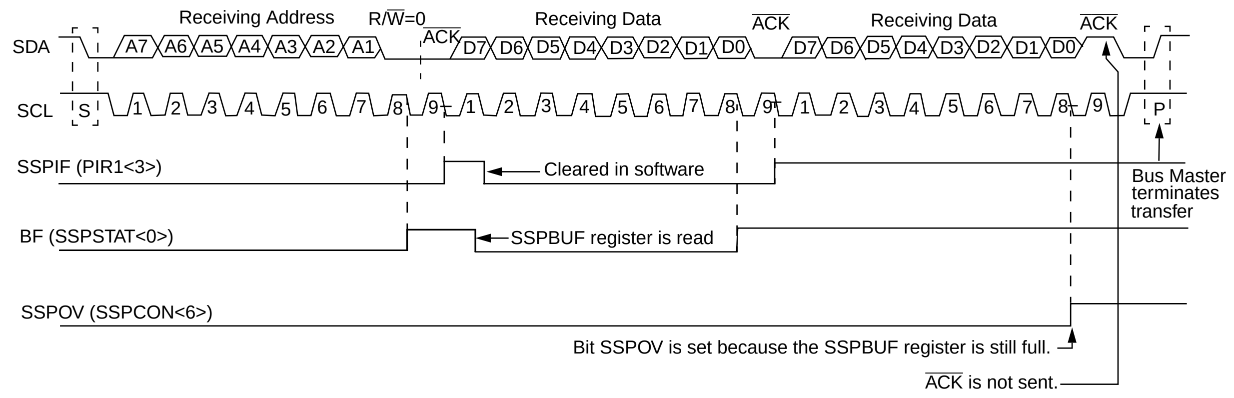
### 11.5.1.2 RECEPTION

When the $R/\overline{W}$ bit of the address byte is clear and an address match occurs, the $R/\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

**FIGURE 11-25: $I^2C$ WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)**



### TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

| BAUD RATE (K) | FOSC = 20 MHz |  |  | 16 MHz |  |  | 10 MHz |  |  | 7.16 MHz |  |  |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) |
| 9.6 | 9.615 | +0.16 | 129 | 9.615 | +0.16 | 103 | 9.615 | +0.16 | 64 | 9.520 | -0.83 | 46 |
| 19.2 | 19.230 | +0.16 | 64 | 19.230 | +0.16 | 51 | 18.939 | -1.36 | 32 | 19.454 | +1.32 | 22 |
| 38.4 | 37.878 | -1.36 | 32 | 38.461 | +0.16 | 25 | 39.062 | +1.7 | 15 | 37.286 | -2.90 | 11 |
| 57.6 | 56.818 | -1.36 | 21 | 58.823 | +2.12 | 16 | 56.818 | -1.36 | 10 | 55.930 | -2.90 | 7 |
| 115.2 | 113.636 | -1.36 | 10 | 111.111 | -3.55 | 8 | 125 | +8.51 | 4 | 111.860 | -2.90 | 3 |
| 250 | 250 | 0 | 4 | 250 | 0 | 3 | NA | - | - | NA | - | - |
| 625 | 625 | 0 | 1 | NA | - | - | 625 | 0 | 0 | NA | - | - |
| 1250 | 1250 | 0 | 0 | NA | - | - | NA | - | - | NA | - | - |

| BAUD RATE (K) | FOSC = 5.068 MHz |  |  | 4 MHz |  |  | 3.579 MHz |  |  | 1 MHz |  |  | 32.768 kHz |  |  |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) |
| 9.6 | 9.6 | 0 | 32 | NA | - | - | 9.727 | +1.32 | 22 | 8.928 | -6.99 | 6 | NA | - | - |
| 19.2 | 18.645 | -2.94 | 16 | 1.202 | +0.17 | 207 | 18.643 | -2.90 | 11 | 20.833 | +8.51 | 2 | NA | - | - |
| 38.4 | 39.6 | +3.12 | 7 | 2.403 | +0.13 | 103 | 37.286 | -2.90 | 5 | 31.25 | -18.61 | 1 | NA | - | - |
| 57.6 | 52.8 | -8.33 | 5 | 9.615 | +0.16 | 25 | 55.930 | -2.90 | 3 | 62.5 | +8.51 | 0 | NA | - | - |
| 115.2 | 105.6 | -8.33 | 2 | 19.231 | +0.16 | 12 | 111.860 | -2.90 | 1 | NA | - | - | NA | - | - |
| 250 | NA | - | - | NA | - | - | 223.721 | -10.51 | 0 | NA | - | - | NA | - | - |
| 625 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1250 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |

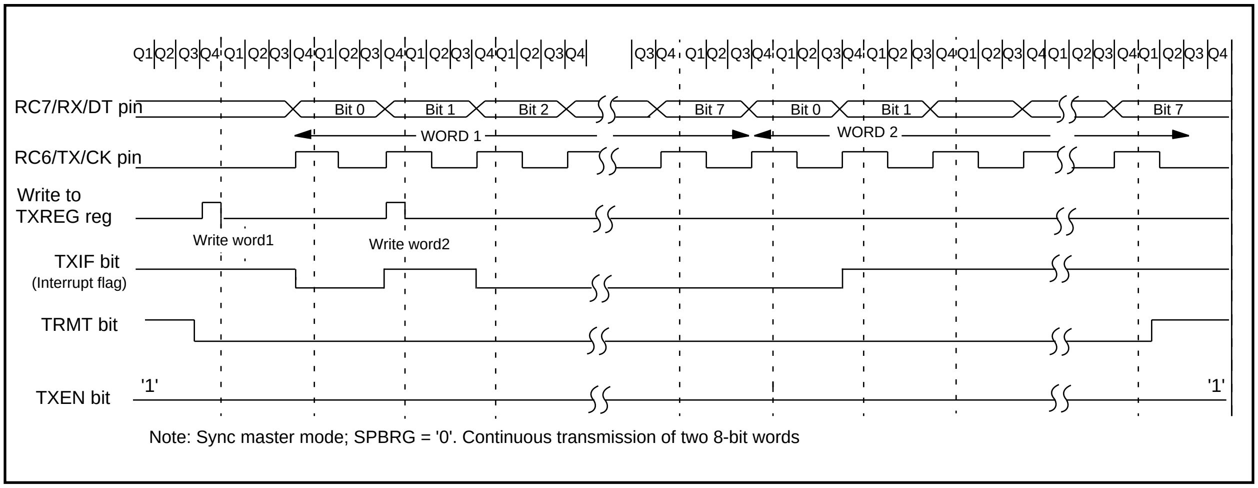
**Note:** For the PIC16C73/73A/74/74A, the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information, or use the PIC16C76/77.

### TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | PIR1 | PSPIF[(1)] | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | `0000 0000` | `0000 0000` |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | — | FERR | OERR | RX9D | `0000 -00x` | `0000 -00x` |
| 19h | TXREG | USART Transmit Register | | | | | | | | `0000 0000` | `0000 0000` |
| 8Ch | PIE1 | PSPIE[(1)] | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | `0000 0000` | `0000 0000` |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | `0000 -010` | `0000 -010` |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | `0000 0000` | `0000 0000` |

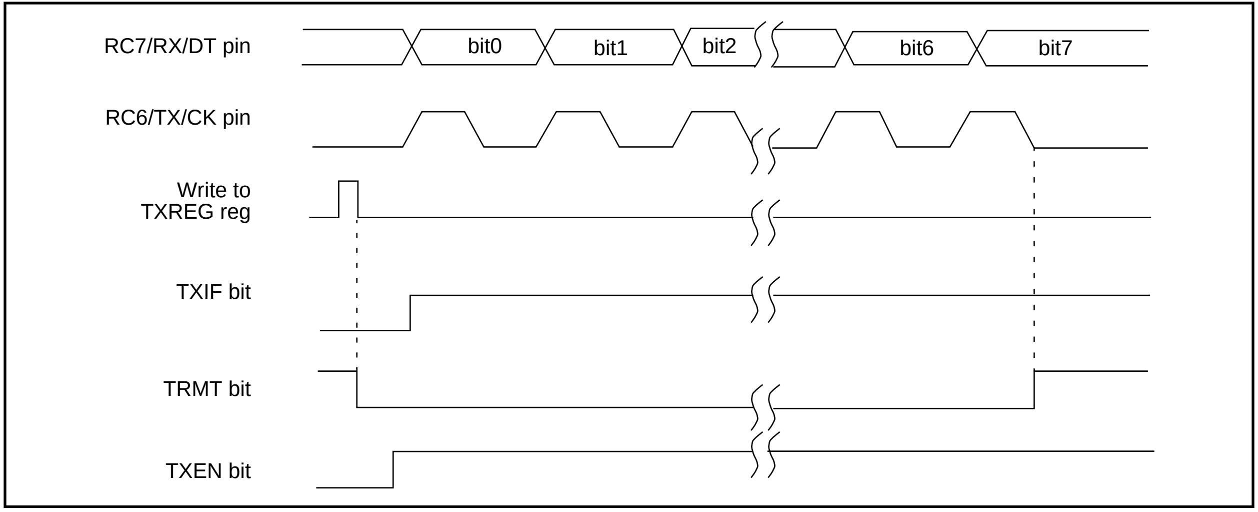
Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Master Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A/76, always maintain these bits clear.

### FIGURE 12-12: SYNCHRONOUS TRANSMISSION



Note: Sync master mode; SPBRG = '0'. Continuous transmission of two 8-bit words

### FIGURE 12-13: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



### TABLE 13-3: SUMMARY OF A/D REGISTERS, PIC16C73/73A/74/74A/76/77

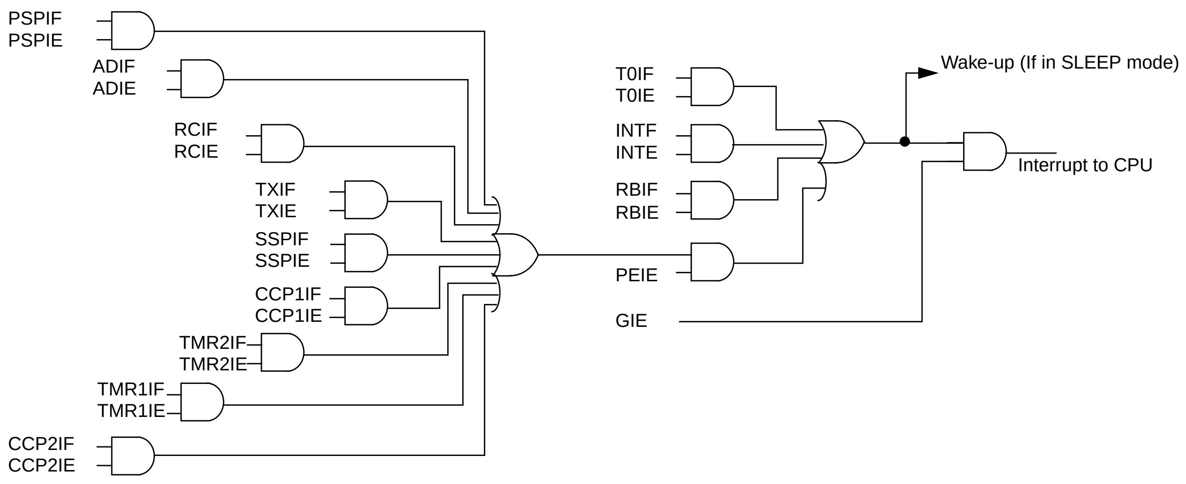
| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Bh,8Bh, 10Bh,18Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 0Dh | PIR2 | — | — | — | — | — | — | — | CCP2IF | ---- ---0 | ---- ---0 |
| 8Dh | PIE2 | — | — | — | — | — | — | — | CCP2IE | ---- ---0 | ---- ---0 |
| 1Eh | ADRES | A/D Result Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 1Fh | ADCON0 | ADCS1 | ADCS0 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | — | ADON | 0000 00-0 | 0000 00-0 |
| 9Fh | ADCON1 | — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 | ---- -000 | ---- -000 |
| 05h | PORTA | — | — | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | --0x 0000 | --0u 0000 |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | --11 1111 | --11 1111 |
| 09h | PORTE | — | — | — | — | — | RE2 | RE1 | RE0 | ---- -xxx | ---- -uuu |
| 89h | TRISE | IBF | OBF | IBOV | PSPMODE | — | PORTE Data Direction Bits | | | 0000 -111 | 0000 -111 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC6C73/73A/76, always maintain these bits clear.

NOTES:

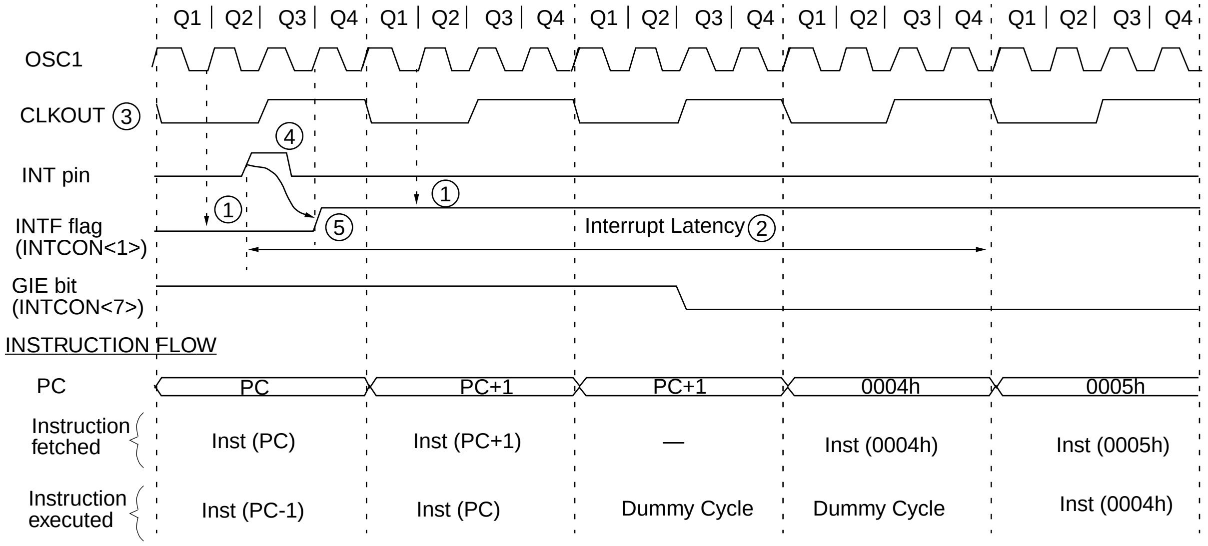
### FIGURE 14-16: INTERRUPT LOGIC



The following table shows which devices have which interrupts.

| Device | T0IF | INTF | RBIF | PSPIF | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | CCP2IF |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC16C72 | Yes | Yes | Yes | - | Yes | - | - | Yes | Yes | Yes | Yes | - |
| PIC16C73 | Yes | Yes | Yes | - | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PIC16C73A | Yes | Yes | Yes | - | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PIC16C74 | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PIC16C74A | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PIC16C76 | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PIC16C77 | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

### FIGURE 14-17: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).
2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time.
Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

## BTFSS Bit Test f, Skip if Set

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 127
0 ≤ b < 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| `01` | `11bb` | `bfff` | `ffff` |

Description: If bit 'b' in register 'f' is '0' then the next instruction is executed.
If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | No-Operation |

If Skip: (2nd Cycle)

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| No-Operation | No-Operation | No-Operation | No-Operation |

Example

```
HERE    BTFSC  FLAG,1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address `HERE`
After Instruction
if FLAG<1> = 0,
PC = address `FALSE`
if FLAG<1> = 1,
PC = address `TRUE`

## CALL Call Subroutine

Syntax: [ *label* ] CALL k

Operands: 0 ≤ k ≤ 2047

Operation: (PC)+ 1→ TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| `10` | `0kkk` | `kkkk` | `kkkk` |

Description: Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. `CALL` is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

| | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|
| 1st Cycle | Decode | Read literal 'k', Push PC to Stack | Process data | Write to PC |
| 2nd Cycle | No-Operation | No-Operation | No-Operation | No-Operation |

Example

```
HERE    CALL   THERE
```

Before Instruction
PC = Address `HERE`
After Instruction
PC = Address `THERE`
TOS = Address `HERE+1`

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

## 17.0 ELECTRICAL CHARACTERISTICS FOR PIC16C72

**Absolute Maximum Ratings †**

| | |
|---|---|
| Ambient temperature under bias | -55 to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on any pin with respect to VSS (except VDD, $\overline{\text{MCLR}}$, and RA4) | -0.3V to (VDD + 0.3V) |
| Voltage on VDD with respect to VSS | -0.3 to +7.5V |
| Voltage on $\overline{\text{MCLR}}$ with respect to VSS (Note 2) | 0 to +14V |
| Voltage on RA4 with respect to Vss | 0 to +14V |
| Total power dissipation (Note 1) | 1.0W |
| Maximum current out of VSS pin | 300 mA |
| Maximum current into VDD pin | 250 mA |
| Input clamp current, IIK (VI < 0 or VI > VDD) | ±20 mA |
| Output clamp current, IOK (VO < 0 or VO > VDD) | ±20 mA |
| Maximum output current sunk by any I/O pin | 25 mA |
| Maximum output current sourced by any I/O pin | 25 mA |
| Maximum current sunk by PORTA and PORTB (combined) | 200 mA |
| Maximum current sourced by PORTA and PORTB (combined) | 200 mA |
| Maximum current sunk by PORTC | 200 mA |
| Maximum current sourced by PORTC | 200 mA |

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

**Note 2:** Voltage spikes below VSS at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

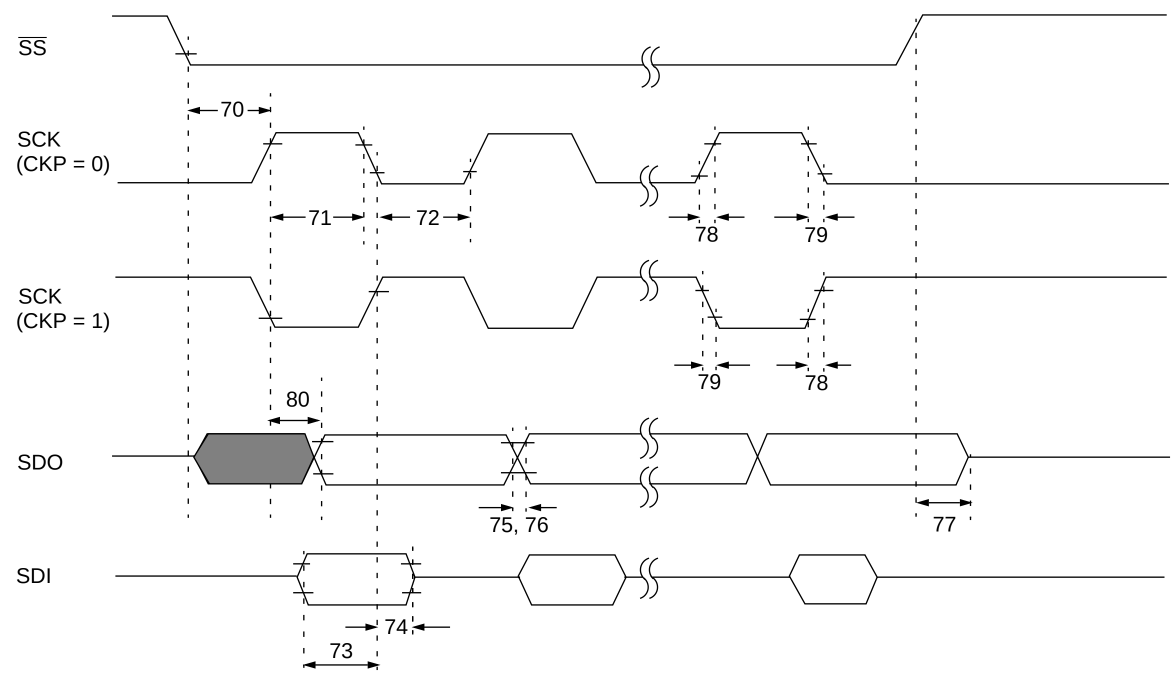
### TABLE 17-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

| OSC | PIC16C72-04 | PIC16C72-10 | PIC16C72-20 | PIC16LC72-04 | JW Devices |
|---|---|---|---|---|---|
| RC | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 16 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 3.8 mA max. at 3.0V<br>IPD: 5.0 µA max. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 16 µA max. at 4V<br>Freq: 4 MHz max. |
| XT | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 16 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 3.8 mA max. at 3.0V<br>IPD: 5.0 µA max. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 16 µA max. at 4V<br>Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V<br>IDD: 13.5 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 10 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 10 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 20 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 20 MHz max. | Not recommended for use in HS mode | VDD: 4.5V to 5.5V<br>IDD: 20 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 20 MHz max. |
| LP | VDD: 4.0V to 6.0V<br>IDD: 52.5 µA typ. at 32 kHz, 4.0V<br>IPD: 0.9 µA typ. at 4.0V<br>Freq: 200 kHz max. | Not recommended for use in LP mode | Not recommended for use in LP mode | VDD: 2.5V to 6.0V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 5.0 µA max. at 3.0V<br>Freq: 200 kHz max. | VDD: 2.5V to 6.0V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 5.0 µA max. at 3.0V<br>Freq: 200 kHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications.
It is recommended that the user select the device type that ensures the specifications required.

| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 17-8: SPI MODE TIMING



Note: Refer to Figure 17-1 for load conditions

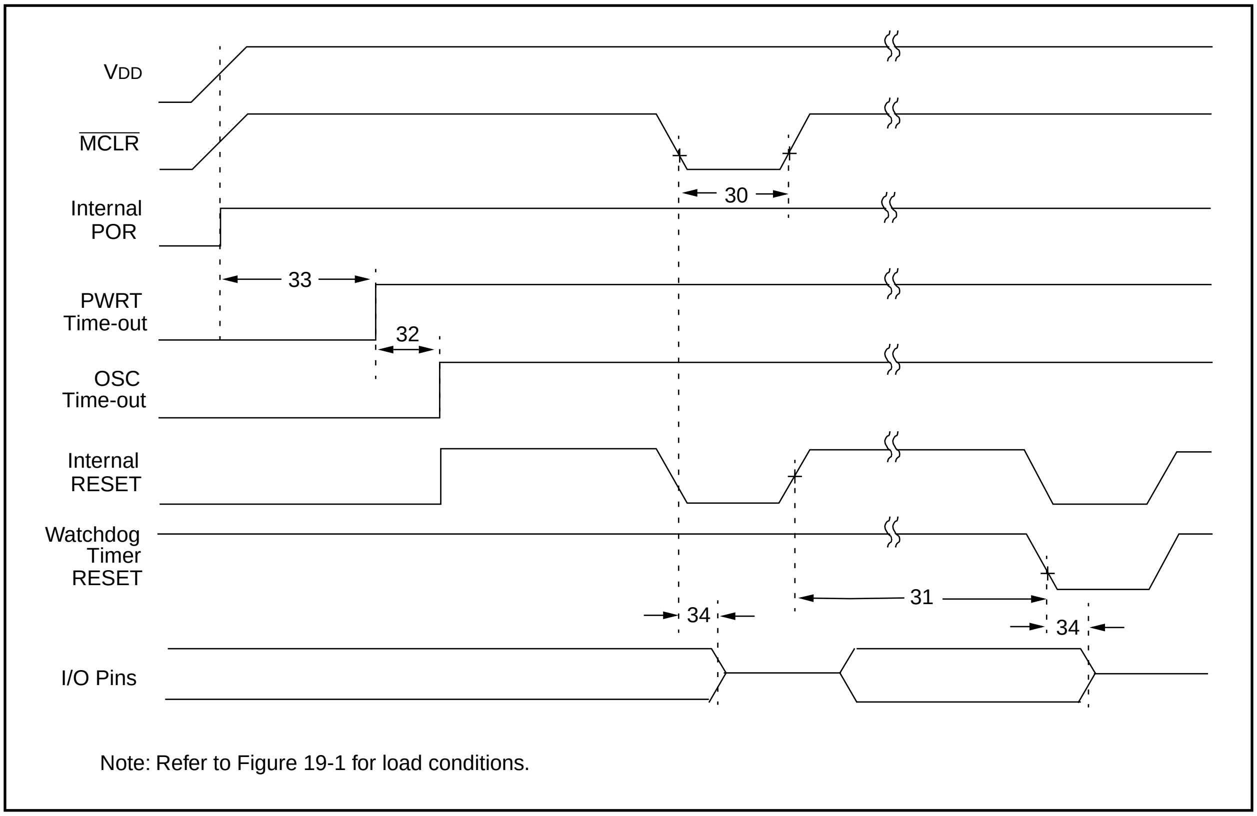
### TABLE 17-7: SPI MODE REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70 | TssL2scH,<br>TssL2scL | $\overline{SS}$↓ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71 | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72 | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73 | TdiV2scH,<br>TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74 | TscH2diL,<br>TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75 | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76 | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77 | TssH2doZ | $\overline{SS}$↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78 | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79 | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80 | TscH2doV,<br>TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

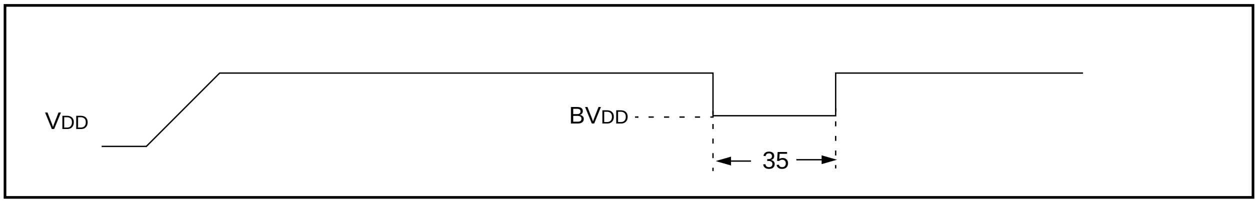
| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 19-1 for load conditions.

### FIGURE 19-5: BROWN-OUT RESET TIMING



### TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

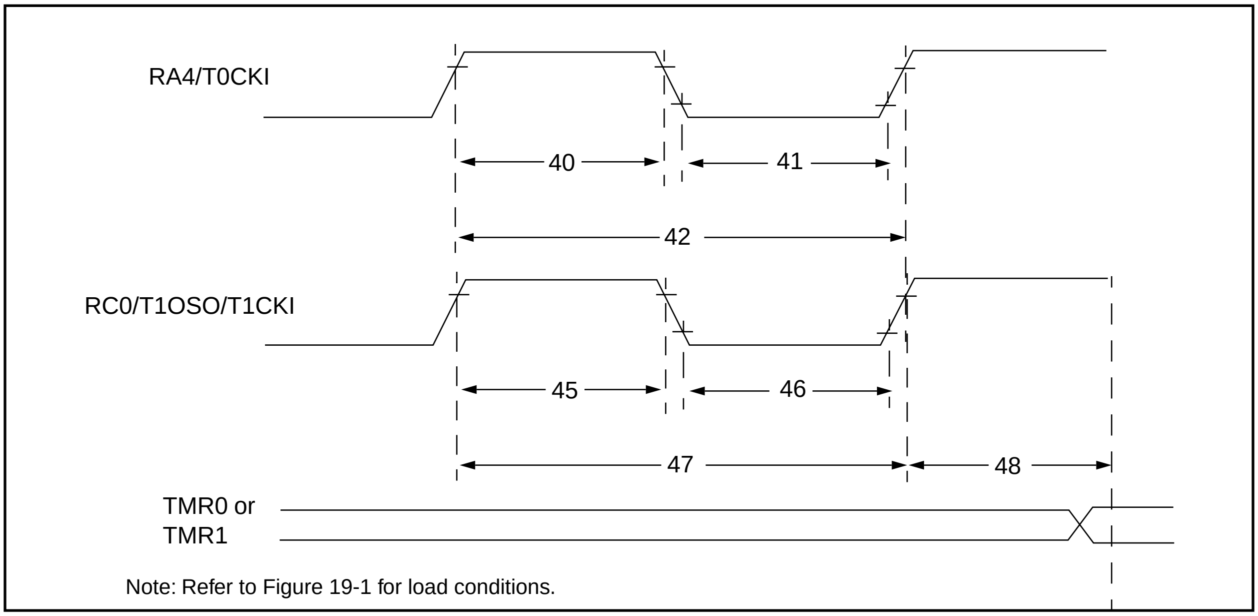
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2 | — | — | µs | VDD = 5V, -40˚C to +125˚C |
| 31* | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40˚C to +125˚C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024TOSC | — | — | TOSC = OSC1 period |
| 33* | Tpwrt | Power up Timer Period | 28 | 72 | 132 | ms | VDD = 5V, -40˚C to +125˚C |
| 34 | TIOZ | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset | — | — | 2.1 | µs | |
| 35 | TBOR | Brown-out Reset pulse width | 100 | — | — | µs | VDD ≤ BVDD (D005) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 19-6: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 19-1 for load conditions.

### TABLE 19-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

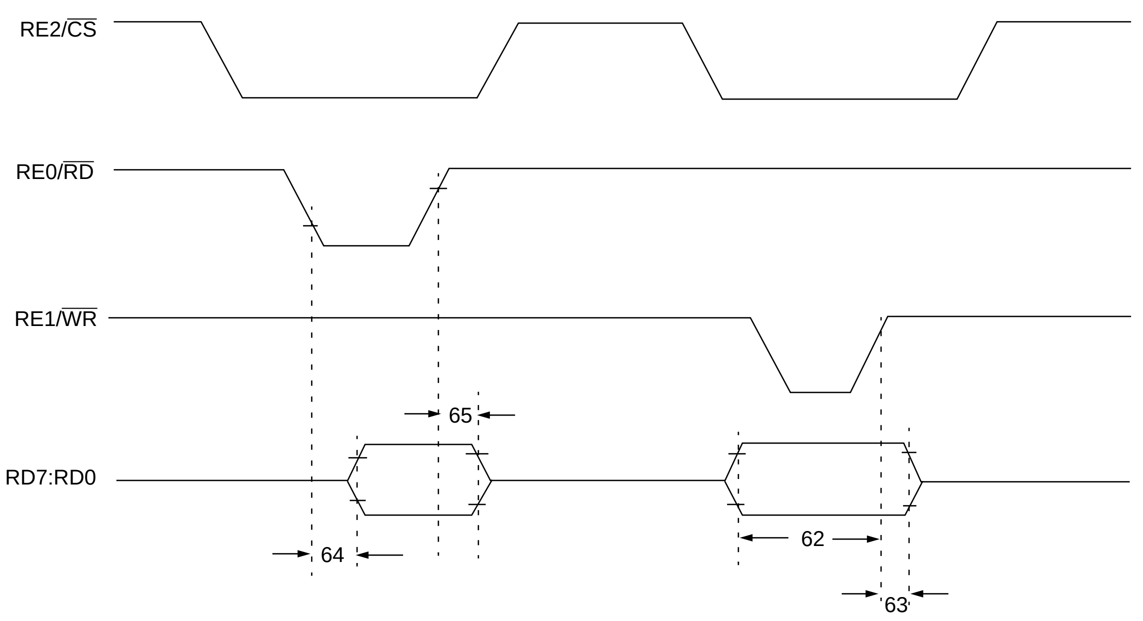
| Param No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 40* | Tt0H | T0CKI High Pulse Width | | No Prescaler | 0.5TCY + 20 | — | — | ns | Must also meet parameter 42 |
| | | | | With Prescaler | 10 | — | — | ns | |
| 41* | Tt0L | T0CKI Low Pulse Width | | No Prescaler | 0.5TCY + 20 | — | — | ns | Must also meet parameter 42 |
| | | | | With Prescaler | 10 | — | — | ns | |
| 42* | Tt0P | T0CKI Period | | No Prescaler | TCY + 40 | — | — | ns | |
| | | | | With Prescaler | Greater of:<br>20 or $\frac{T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (2, 4, ..., 256) |
| 45* | Tt1H | T1CKI High Time | Synchronous, Prescaler = 1 | | 0.5TCY + 20 | — | — | ns | Must also meet parameter 47 |
| | | | Synchronous, Prescaler = 2,4,8 | PIC16**C**7X | 15 | — | — | ns | |
| | | | | PIC16**LC**7X | 25 | — | — | ns | |
| | | | Asynchronous | PIC16**C**7X | 30 | — | — | ns | |
| | | | | PIC16**LC**7X | 50 | — | — | ns | |
| 46* | Tt1L | T1CKI Low Time | Synchronous, Prescaler = 1 | | 0.5TCY + 20 | — | — | ns | Must also meet parameter 47 |
| | | | Synchronous, Prescaler = 2,4,8 | PIC16**C**7X | 15 | — | — | ns | |
| | | | | PIC16**LC**7X | 25 | — | — | ns | |
| | | | Asynchronous | PIC16**C**7X | 30 | — | — | ns | |
| | | | | PIC16**LC**7X | 50 | — | — | ns | |
| 47* | Tt1P | T1CKI input period | Synchronous | PIC16**C**7X | Greater of:<br>30 OR $\frac{T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1, 2, 4, 8) |
| | | | | PIC16**LC**7X | Greater of:<br>50 OR $\frac{T_{CY} + 40}{N}$ | | | | N = prescale value (1, 2, 4, 8) |
| | | | Asynchronous | PIC16**C**7X | 60 | — | — | ns | |
| | | | | PIC16**LC**7X | 100 | — | — | ns | |
| | Ft1 | Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN) | | | DC | — | 200 | kHz | |
| 48 | TCKEZtmr1 | Delay from external clock edge to timer increment | | | 2Tosc | — | 7Tosc | — | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 19-8: PARALLEL SLAVE PORT TIMING (PIC16C74A)



Note: Refer to Figure 19-1 for load conditions

### TABLE 19-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C74A)

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 62 | TdtV2wrH | Data in valid before $\overline{\text{WR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ (setup time) | | 20<br>25 | —<br>— | —<br>— | ns<br>ns | <br>Extended Range Only |
| 63* | TwrH2dtI | $\overline{\text{WR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ to data–in invalid (hold time) | PIC16**C**74A | 20 | — | — | ns | |
| | | | PIC16**LC**74A | 35 | — | — | ns | |
| 64 | TrdL2dtV | $\overline{\text{RD}}\downarrow$ and $\overline{\text{CS}}\downarrow$ to data–out valid | | —<br>— | —<br>— | 80<br>90 | ns<br>ns | <br>Extended Range Only |
| 65 | TrdH2dtI | $\overline{\text{RD}}\uparrow$ or $\overline{\text{CS}}\downarrow$ to data–out invalid | | 10 | — | 30 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

## 20.1 DC Characteristics: PIC16C76/77-04 (Commercial, Industrial, Extended)
PIC16C76/77-10 (Commercial, Industrial, Extended)
PIC16C76/77-20 (Commercial, Industrial, Extended)

| DC CHARACTERISTICS | **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40˚C ≤ TA ≤ +125˚C for extended,<br>-40˚C ≤ TA ≤ +85˚C for industrial and<br>0˚C ≤ TA ≤ +70˚C for commercial |
|---|---|

| Param No. | Characteristic | Sym | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| D001 | Supply Voltage | VDD | 4.0 | - | 6.0 | V | XT, RC and LP osc configuration |
| D001A | | | 4.5 | - | 5.5 | V | HS osc configuration |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | V | |
| D003 | VDD start voltage to ensure internal Power-on Reset signal | VPOR | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset signal | SVDD | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D005 | Brown-out Reset Voltage | BVDD | 3.7 | 4.0 | 4.3 | V | BODEN bit in configuration word enabled |
| | | | 3.7 | 4.0 | 4.4 | V | Extended Range Only |
| D010 | Supply Current (Note 2,5) | IDD | - | 2.7 | 5 | mA | XT, RC osc configuration<br>FOSC = 4 MHz, VDD = 5.5V (Note 4) |
| D013 | | | - | 10 | 20 | mA | HS osc configuration<br>FOSC = 20 MHz, VDD = 5.5V |
| D015* | Brown-out Reset Current (Note 6) | ΔIBOR | - | 350 | 425 | µA | BOR enabled VDD = 5.0V |
| D020 | Power-down Current (Note 3,5) | IPD | - | 10.5 | 42 | µA | VDD = 4.0V, WDT enabled, -40°C to +85°C |
| D021 | | | - | 1.5 | 16 | µA | VDD = 4.0V, WDT disabled, -0°C to +70°C |
| D021A | | | - | 1.5 | 19 | µA | VDD = 4.0V, WDT disabled, -40°C to +85°C |
| D021B | | | - | 2.5 | 19 | µA | VDD = 4.0V, WDT disabled, -40°C to +125°C |
| D023* | Brown-out Reset Current (Note 6) | ΔIBOR | - | 350 | 425 | µA | BOR enabled VDD = 5.0V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

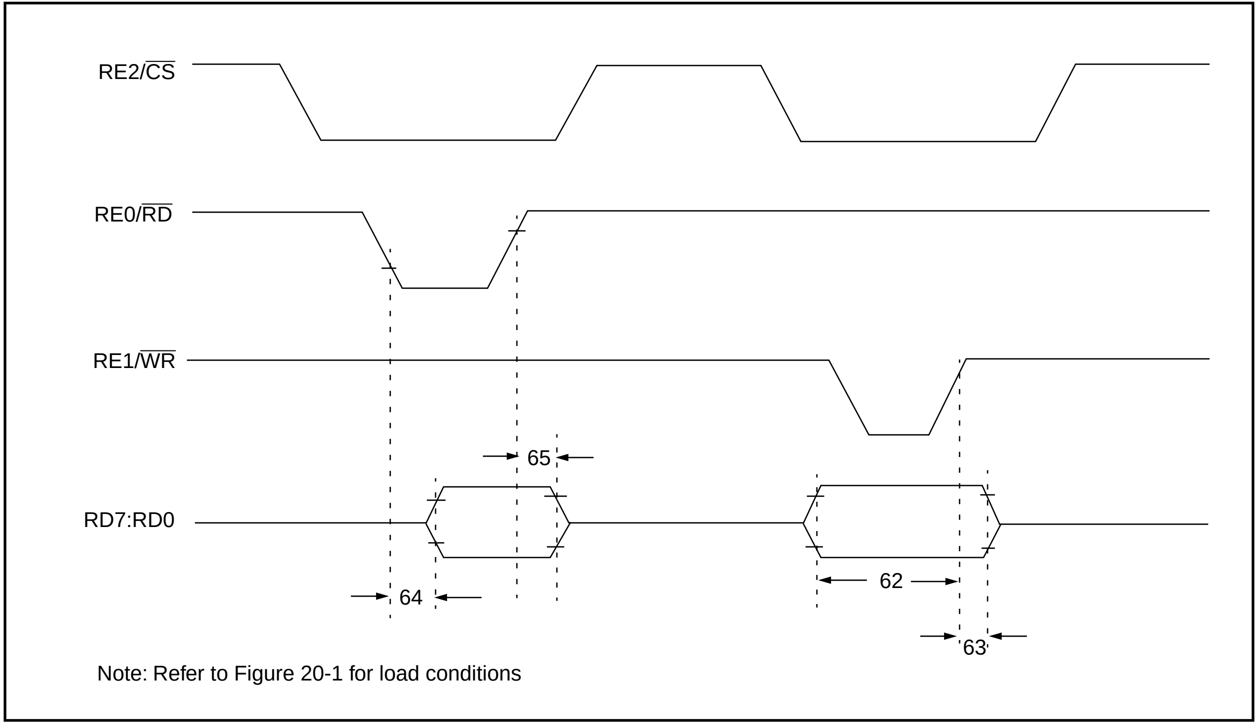
4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 20-8: PARALLEL SLAVE PORT TIMING (PIC16C77)



Note: Refer to Figure 20-1 for load conditions

### TABLE 20-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C77)

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 62 | TdtV2wrH | Data in valid before $\overline{\text{WR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ (setup time) | | 20 | — | — | ns | |
| | | | | 25 | — | — | ns | Extended Range Only |
| 63* | TwrH2dtI | $\overline{\text{WR}}\uparrow$ or $\overline{\text{CS}}\uparrow$ to data–in invalid (hold time) | PIC16**C**77 | 20 | — | — | ns | |
| | | | PIC16**LC**77 | 35 | — | — | ns | |
| 64 | TrdL2dtV | $\overline{\text{RD}}\downarrow$ and $\overline{\text{CS}}\downarrow$ to data–out valid | | — | — | 80 | ns | |
| | | | | — | — | 90 | ns | Extended Range Only |
| 65 | TrdH2dtI | $\overline{\text{RD}}\uparrow$ or $\overline{\text{CS}}\downarrow$ to data–out invalid | | 10 | — | 30 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

## E.5 PIC16C55X Family of Devices

| | | PIC16C554 | PIC16C556[1] | PIC16C558 |
|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 512 | 1K | 2K |
| | Data Memory (bytes) | 80 | 80 | 128 |
| **Peripherals** | Timer Module(s) | TMR0 | TMR0 | TMR0 |
| | Comparators(s) | — | — | — |
| | Internal Reference Voltage | — | — | — |
| **Features** | Interrupt Sources | 3 | 3 | 3 |
| | I/O Pins | 13 | 13 | 13 |
| | Voltage Range (Volts) | 2.5-6.0 | 2.5-6.0 | 2.5-6.0 |
| | Brown-out Reset | — | — | — |
| | Packages | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C5XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

## E.6 PIC16C62X and PIC16C64X Family of Devices

| | | PIC16C620 | PIC16C621 | PIC16C622 | PIC16C642 | PIC16C662 |
|---|---|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 512 | 1K | 2K | 4K | 4K |
| | Data Memory (bytes) | 80 | 80 | 128 | 176 | 176 |
| **Peripherals** | Timer Module(s) | TMR0 | TMR0 | TMR0 | TMR0 | TMR0 |
| | Comparators(s) | 2 | 2 | 2 | 2 | 2 |
| | Internal Reference Voltage | Yes | Yes | Yes | Yes | Yes |
| **Features** | Interrupt Sources | 4 | 4 | 4 | 4 | 5 |
| | I/O Pins | 13 | 13 | 13 | 22 | 33 |
| | Voltage Range (Volts) | 2.5-6.0 | 2.5-6.0 | 2.5-6.0 | 3.0-6.0 | 3.0-6.0 |
| | Brown-out Reset | Yes | Yes | Yes | Yes | Yes |
| | Packages | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 18-pin DIP,<br>SOIC;<br>20-pin SSOP | 28-pin PDIP,<br>SOIC,<br>Windowed CDIP | 40-pin PDIP,<br>Windowed CDIP;<br>44-pin PLCC,<br>MQFP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X and PIC16C64X Family devices use serial programming with clock pin RB6 and data pin RB7.