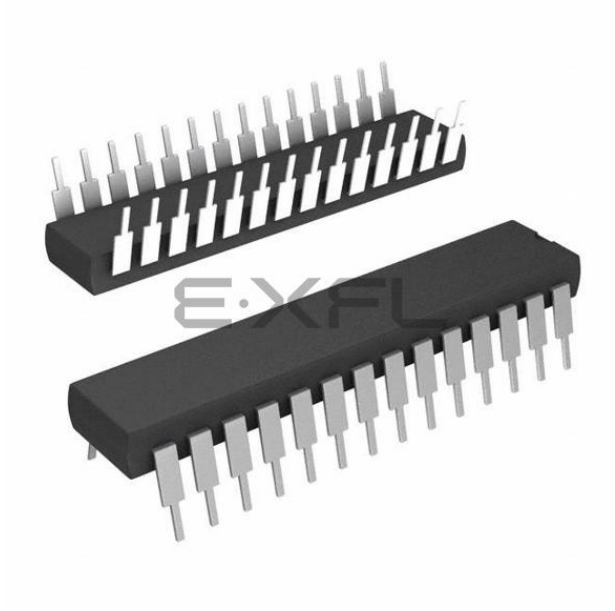

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 192 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 6V |
| Data Converters | A/D 5x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c73a-20e-sp |

**FIGURE 4-13: PIR1 REGISTER PIC16C73/73A/74/74A/76/77 (ADDRESS 0Ch)**

| R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **PSPIF(1):** Parallel Slave Port Read/Write Interrupt Flag bit
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

bit 6: **ADIF**: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

bit 5: **RCIF**: USART Receive Interrupt Flag bit
1 = The USART receive buffer is full (cleared by reading RCREG)
0 = The USART receive buffer is empty

bit 4: **TXIF**: USART Transmit Interrupt Flag bit
1 = The USART transmit buffer is empty (cleared by writing to TXREG)
0 = The USART transmit buffer is full

bit 3: **SSPIF**: Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2: **CCP1IF**: CCP1 Interrupt Flag bit
Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode
Unused in this mode

bit 1: **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF**: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Note 1: PIC16C73/73A/76 devices do not have a Parallel Slave Port implemented, this bit location is reserved on these devices, always maintain this bit clear.

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**NOTES:**

## 5.7 Parallel Slave Port

| Applicable Devices | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

PORTD operates as an 8-bit wide Parallel Slave Port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through $\overline{RD}$ control input pin RE0/$\overline{RD}$/AN5 and $\overline{WR}$ control input pin RE1/$\overline{WR}$/AN6.

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/$\overline{RD}$/AN5 to be the $\overline{RD}$ input, RE1/$\overline{WR}$/AN6 to be the $\overline{WR}$ input and RE2/$\overline{CS}$/AN7 to be the $\overline{CS}$ (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set) and the A/D port configuration bits PCFG2:PCFG0 (ADCON1<2:0>) must be set, which will configure pins RE2:RE0 as digital I/O.

There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored, since the microprocessor is controlling the direction of data flow.

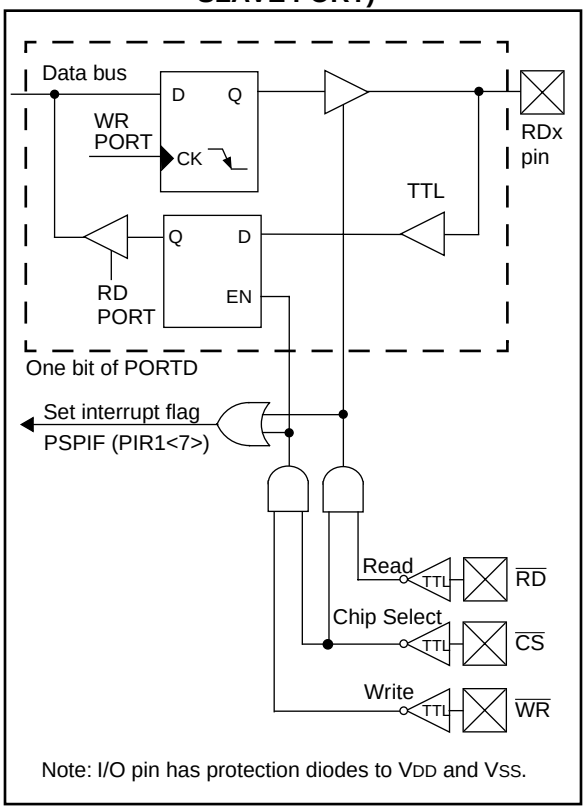
A write to the PSP occurs when both the $\overline{CS}$ and $\overline{WR}$ lines are first detected low. When either the $\overline{CS}$ or $\overline{WR}$ lines become high (level triggered), then the Input Buffer Full status flag bit IBF (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete (Figure 5-12). The interrupt flag bit PSPIF (PIR1<7>) is also set on the same Q4 clock cycle. IBF can only be cleared by reading the PORTD input latch. The input Buffer Overflow status flag bit IBOV (TRISE<5>) is set if a second write to the Parallel Slave Port is attempted when the previous byte has not been read out of the buffer.

A read from the PSP occurs when both the $\overline{CS}$ and $\overline{RD}$ lines are first detected low. The Output Buffer Full status flag bit OBF (TRISE<6>) is cleared immediately (Figure 5-13) indicating that the PORTD latch is waiting to be read by the external bus. When either the $\overline{CS}$ or $\overline{RD}$ pin becomes high (level triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware.

When not in Parallel Slave Port mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in firmware.

An interrupt is generated and latched into flag bit PSPIF when a read or write operation is completed. PSPIF must be cleared by the user in firmware and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

**FIGURE 5-11: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)**




Note: I/O pin has protection diodes to $V_{DD}$ and $V_{SS}$.

**NOTES:**

## 11.2 SPI Mode for PIC16C72/73/73A/74/74A

This section contains register definitions and operational characteristics of the SPI module for the PIC16C72, PIC16C73, PIC16C73A, PIC16C74, PIC16C74A.

**FIGURE 11-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)**

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **D/$\overline{A}$**: Data/Address bit ($I^2C$ mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit ($I^2C$ mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
0 = Stop bit was not detected last

bit 3: **S**: Start bit ($I^2C$ mode only. This bit is cleared when the SSP module is disabled, SSPEN is cleared)
1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
0 = Start bit was not detected last

bit 2: **R/$\overline{W}$**: Read/Write bit information ($I^2C$ mode only)
This bit holds the R/W bit information following the last address match. This bit is valid from the address match to the next start bit, stop bit, or $\overline{ACK}$ bit.
1 = Read
0 = Write

bit 1: **UA**: Update Address (10-bit $I^2C$ mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and $I^2C$ modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit ($I^2C$ mode only)
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

### TABLE 12-3: BAUD RATES FOR SYNCHRONOUS MODE

| BAUD RATE (K) | FOSC = 20 MHz KBAUD | % ERROR | SPBRG value (decimal) | 16 MHz KBAUD | % ERROR | SPBRG value (decimal) | 10 MHz KBAUD | % ERROR | SPBRG value (decimal) | 7.15909 MHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1.2 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 2.4 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 9.6 | NA | - | - | NA | - | - | 9.766 | +1.73 | 255 | 9.622 | +0.23 | 185 |
| 19.2 | 19.53 | +1.73 | 255 | 19.23 | +0.16 | 207 | 19.23 | +0.16 | 129 | 19.24 | +0.23 | 92 |
| 76.8 | 76.92 | +0.16 | 64 | 76.92 | +0.16 | 51 | 75.76 | -1.36 | 32 | 77.82 | +1.32 | 22 |
| 96 | 96.15 | +0.16 | 51 | 95.24 | -0.79 | 41 | 96.15 | +0.16 | 25 | 94.20 | -1.88 | 18 |
| 300 | 294.1 | -1.96 | 16 | 307.69 | +2.56 | 12 | 312.5 | +4.17 | 7 | 298.3 | -0.57 | 5 |
| 500 | 500 | 0 | 9 | 500 | 0 | 7 | 500 | 0 | 4 | NA | - | - |
| HIGH | 5000 | - | 0 | 4000 | - | 0 | 2500 | - | 0 | 1789.8 | - | 0 |
| LOW | 19.53 | - | 255 | 15.625 | - | 255 | 9.766 | - | 255 | 6.991 | - | 255 |

| BAUD RATE (K) | FOSC = 5.0688 MHz KBAUD | % ERROR | SPBRG value (decimal) | 4 MHz KBAUD | % ERROR | SPBRG value (decimal) | 3.579545 MHz KBAUD | % ERROR | SPBRG value (decimal) | 1 MHz KBAUD | % ERROR | SPBRG value (decimal) | 32.768 kHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | 0.303 | +1.14 | 26 |
| 1.2 | NA | - | - | NA | - | - | NA | - | - | 1.202 | +0.16 | 207 | 1.170 | -2.48 | 6 |
| 2.4 | NA | - | - | NA | - | - | NA | - | - | 2.404 | +0.16 | 103 | NA | - | - |
| 9.6 | 9.6 | 0 | 131 | 9.615 | +0.16 | 103 | 9.622 | +0.23 | 92 | 9.615 | +0.16 | 25 | NA | - | - |
| 19.2 | 19.2 | 0 | 65 | 19.231 | +0.16 | 51 | 19.04 | -0.83 | 46 | 19.24 | +0.16 | 12 | NA | - | - |
| 76.8 | 79.2 | +3.13 | 15 | 76.923 | +0.16 | 12 | 74.57 | -2.90 | 11 | 83.34 | +8.51 | 2 | NA | - | - |
| 96 | 97.48 | +1.54 | 12 | 1000 | +4.17 | 9 | 99.43 | +3.57 | 8 | NA | - | - | NA | - | - |
| 300 | 316.8 | +5.60 | 3 | NA | - | - | 298.3 | -0.57 | 2 | NA | - | - | NA | - | - |
| 500 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| HIGH | 1267 | - | 0 | 100 | - | 0 | 894.9 | - | 0 | 250 | - | 0 | 8.192 | - | 0 |
| LOW | 4.950 | - | 255 | 3.906 | - | 255 | 3.496 | - | 255 | 0.9766 | - | 255 | 0.032 | - | 255 |

### TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

| BAUD RATE (K) | FOSC = 20 MHz KBAUD | % ERROR | SPBRG value (decimal) | 16 MHz KBAUD | % ERROR | SPBRG value (decimal) | 10 MHz KBAUD | % ERROR | SPBRG value (decimal) | 7.15909 MHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1.2 | 1.221 | +1.73 | 255 | 1.202 | +0.16 | 207 | 1.202 | +0.16 | 129 | 1.203 | +0.23 | 92 |
| 2.4 | 2.404 | +0.16 | 129 | 2.404 | +0.16 | 103 | 2.404 | +0.16 | 64 | 2.380 | -0.83 | 46 |
| 9.6 | 9.469 | -1.36 | 32 | 9.615 | +0.16 | 25 | 9.766 | +1.73 | 15 | 9.322 | -2.90 | 11 |
| 19.2 | 19.53 | +1.73 | 15 | 19.23 | +0.16 | 12 | 19.53 | +1.73 | 7 | 18.64 | -2.90 | 5 |
| 76.8 | 78.13 | +1.73 | 3 | 83.33 | +8.51 | 2 | 78.13 | +1.73 | 1 | NA | - | - |
| 96 | 104.2 | +8.51 | 2 | NA | - | - | NA | - | - | NA | - | - |
| 300 | 312.5 | +4.17 | 0 | NA | - | - | NA | - | - | NA | - | - |
| 500 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| HIGH | 312.5 | - | 0 | 250 | - | 0 | 156.3 | - | 0 | 111.9 | - | 0 |
| LOW | 1.221 | - | 255 | 0.977 | - | 255 | 0.6104 | - | 255 | 0.437 | - | 255 |

| BAUD RATE (K) | FOSC = 5.0688 MHz KBAUD | % ERROR | SPBRG value (decimal) | 4 MHz KBAUD | % ERROR | SPBRG value (decimal) | 3.579545 MHz KBAUD | % ERROR | SPBRG value (decimal) | 1 MHz KBAUD | % ERROR | SPBRG value (decimal) | 32.768 kHz KBAUD | % ERROR | SPBRG value (decimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.3 | 0.31 | +3.13 | 255 | 0.3005 | -0.17 | 207 | 0.301 | +0.23 | 185 | 0.300 | +0.16 | 51 | 0.256 | -14.67 | 1 |
| 1.2 | 1.2 | 0 | 65 | 1.202 | +1.67 | 51 | 1.190 | -0.83 | 46 | 1.202 | +0.16 | 12 | NA | - | - |
| 2.4 | 2.4 | 0 | 32 | 2.404 | +1.67 | 25 | 2.432 | +1.32 | 22 | 2.232 | -6.99 | 6 | NA | - | - |
| 9.6 | 9.9 | +3.13 | 7 | NA | - | - | 9.322 | -2.90 | 5 | NA | - | - | NA | - | - |
| 19.2 | 19.8 | +3.13 | 3 | NA | - | - | 18.64 | -2.90 | 2 | NA | - | - | NA | - | - |
| 76.8 | 79.2 | +3.13 | 0 | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 96 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 300 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 500 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| HIGH | 79.2 | - | 0 | 62.500 | - | 0 | 55.93 | - | 0 | 15.63 | - | 0 | 0.512 | - | 0 |
| LOW | 0.3094 | - | 255 | 3.906 | - | 255 | 0.2185 | - | 255 | 0.0610 | - | 255 | 0.0020 | - | 255 |

### 12.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 12-10. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at FOSC.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double buffered register, i.e. it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG register is still full then overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited, so it is essential to clear error bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a stop bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG, will load bits RX9D and FERR with new values, therefore it is essential for the user to read the RCSTA register before reading RCREG register in order not to lose the old FERR and RX9D information.

**FIGURE 12-10: USART RECEIVE BLOCK DIAGRAM**

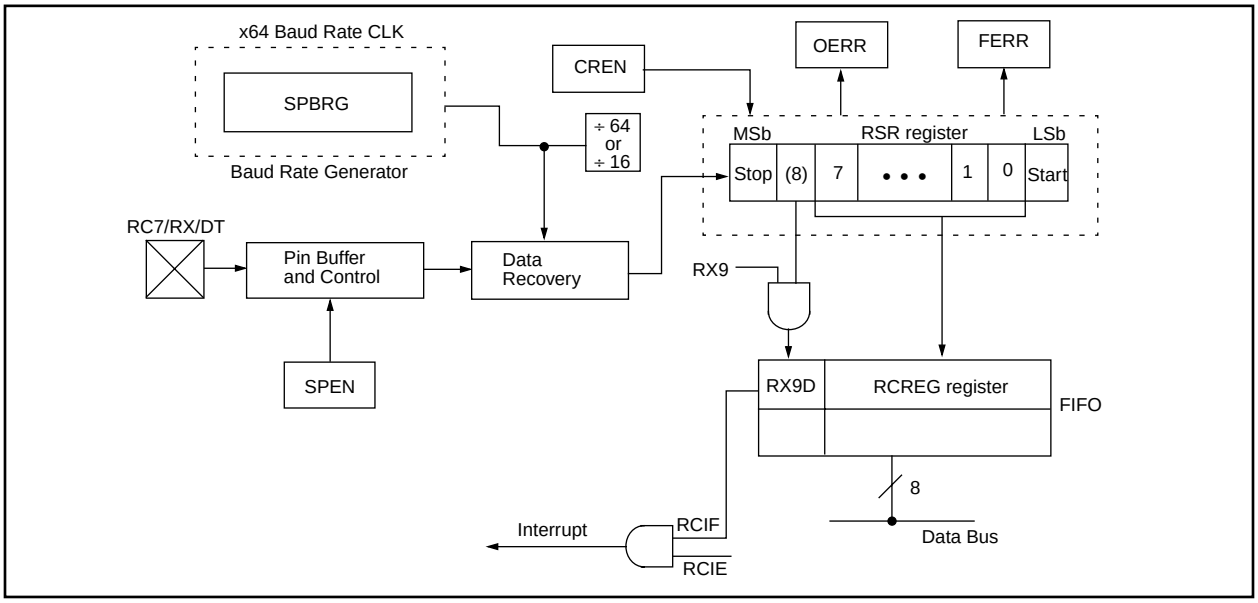
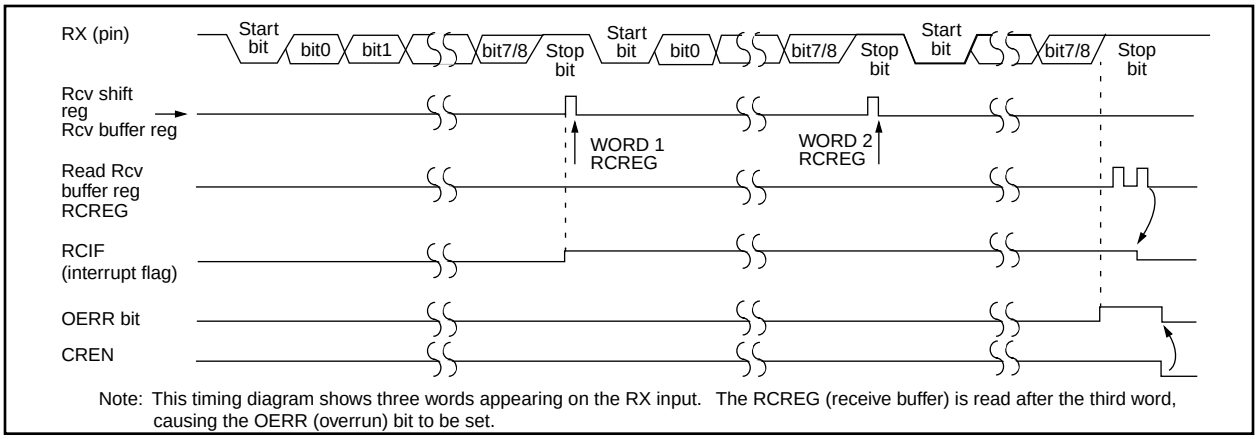



**FIGURE 12-11: ASYNCHRONOUS RECEPTION**




Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

**CLRF** **Clear f**

Syntax: [*label*] CLRF f

Operands: $0 \le f \le 127$

Operation: 00h → (f)
1 → Z

Status Affected: Z

Encoding:

| 00 | 0001 | 1fff | ffff |
|---|---|---|---|

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write register 'f' |

Example
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

**CLRW** **Clear W**

Syntax: [ *label* ] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

| 00 | 0001 | 0xxx | xxxx |
|---|---|---|---|

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | No-Operation | Process data | Write to W |

Example
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

**CLRWDT** **Clear Watchdog Timer**

Syntax: [ *label* ] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| 00 | 0000 | 0110 | 0100 |
|---|---|---|---|

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | No-Operation | Process data | Clear WDT Counter |

Example
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

**GOTO** **Unconditional Branch**

Syntax: [ *label* ] GOTO k

Operands: $0 \le k \le 2047$

Operation: $k \rightarrow PC<10:0>$
$PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 10 | 1kkk | kkkk | kkkk |

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

| | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|
| 1st Cycle | Decode | Read literal 'k' | Process data | Write to PC |
| 2nd Cycle | No-Operation | No-Operation | No-Operation | No-Operation |

Example

```
GOTO THERE
```

After Instruction
PC = Address THERE

**INCF** **Increment f**

Syntax: [ *label* ] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (destination)

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 00 | 1010 | dfff | ffff |

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to destination |

Example

```
INCF    CNT, 1
```

Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

**RLF** **Rotate Left f through Carry**

Syntax: [ *label* ] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

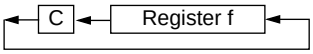
Operation: See description below

Status Affected: C

Encoding:

| 00 | 1101 | dfff | ffff |
|---|---|---|---|

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.




Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to destination |

Example

```
RLF     REG1,0
```

Before Instruction
```
REG1  =  1110 0110
C     =  0
```
After Instruction
```
REG1  =  1110 0110
W     =  1100 1100
C     =  1
```

**RRF** **Rotate Right f through Carry**

Syntax: [ *label* ] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

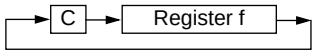
Operation: See description below

Status Affected: C

Encoding:

| 00 | 1100 | dfff | ffff |
|---|---|---|---|

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.




Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to destination |

Example

```
RRF     REG1,0
```

Before Instruction
```
REG1  =  1110 0110
C     =  0
```
After Instruction
```
REG1  =  1110 0110
W     =  0111 0011
C     =  0
```

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### 17.3 DC Characteristics: PIC16C72-04 (Commercial, Industrial, Extended)
### PIC16C72-10 (Commercial, Industrial, Extended)
### PIC16C72-20 (Commercial, Industrial, Extended)
### PIC16LC72-04 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C for extended,<br>-40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial<br>Operating voltage VDD range as described in DC spec Section 17.1 and Section 17.2. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ †** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | | | | |
| D030 | with TTL buffer | | VSS | - | 0.15VDD | V | For entire VDD range |
| D030A | | | VSS | - | 0.8V | V | 4.5 ≤ VDD ≤ 5.5V |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.2VDD | V | |
| D032 | $\overline{MCLR}$, OSC1 (in RC mode) | | VSS | - | 0.2VDD | V | |
| D033 | OSC1 (in XT, HS and LP) | | VSS | - | 0.3VDD | V | Note1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | | 2.0 | - | VDD | V | 4.5 ≤ VDD ≤ 5.5V |
| D040A | | | 0.25VDD + 0.8V | - | VDD | V | For entire VDD range |
| D041 | with Schmitt Trigger buffer | | 0.8VDD | - | VDD | V | For entire VDD range |
| D042 | $\overline{MCLR}$ | | 0.8VDD | - | VDD | V | |
| D042A | OSC1 (XT, HS and LP) | | 0.7VDD | - | VDD | V | Note1 |
| D043 | OSC1 (in RC mode) | | 0.9VDD | - | VDD | V | |
| D070 | PORTB weak pull-up current | IPURB | 50 | 250 | †400 | µA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current** (Notes 2, 3) | | | | | | |
| D060 | I/O ports | IIL | - | - | ±1 | µA | Vss ≤ VPIN ≤ VDD, Pin at hi-impedance |
| D061 | $\overline{MCLR}$, RA4/T0CKI | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD |
| D063 | OSC1 | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports | VOL | - | - | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C |
| D080A | | | - | - | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C |
| D083 | OSC2/CLKOUT (RC osc config) | | - | - | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C |
| D083A | | | - | - | 0.6 | V | IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

**TABLE 17-10: A/D CONVERTER CHARACTERISTICS:**
**PIC16C72-04 (Commercial, Industrial, Extended)**
**PIC16C72-10 (Commercial, Industrial, Extended)**
**PIC16C72-20 (Commercial, Industrial, Extended)**
**PIC16LC72-04 (Commercial, Industrial)**

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | | — | — | 8-bits | bit | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A02 | EABS | Total Absolute error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A03 | EIL | Integral linearity error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A04 | EDL | Differential linearity error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A05 | EFS | Full scale error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A06 | EOFF | Offset error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A10 | — | Monotonicity | | — | guaranteed | — | — | VSS ≤ VAIN ≤ VREF |
| A20 | VREF | Reference voltage | | 3.0V | — | VDD + 0.3 | V | |
| A25 | VAIN | Analog input voltage | | VSS - 0.3 | — | VREF + 0.3 | V | |
| A30 | ZAIN | Recommended impedance of analog voltage source | | — | — | 10.0 | kΩ | |
| A40 | IAD | A/D conversion current (VDD) | PIC16**C**72 | — | 180 | — | μA | Average current consumption when A/D is on. (Note 1) |
| | | | PIC16**LC**72 | — | 90 | — | μA | |
| A50 | IREF | VREF input current (Note 2) | | 10 | — | 1000 | μA | During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 13.1. |
| | | | | — | — | 10 | μA | During A/D Conversion cycle |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

## 18.0 ELECTRICAL CHARACTERISTICS FOR PIC16C73/74

**Absolute Maximum Ratings †**

Ambient temperature under bias ..... -55 to +125˚C

Storage temperature ..... -65˚C to +150˚C

Voltage on any pin with respect to VSS (except VDD, $\overline{MCLR}$. and RA4) ..... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS ..... -0.3 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS (Note 2) ..... 0 to +14V

Voltage on RA4 with respect to Vss ..... 0 to +14V

Total power dissipation (Note 1) ..... 1.0W

Maximum current out of VSS pin ..... 300 mA

Maximum current into VDD pin ..... 250 mA

Input clamp current, IIK (VI < 0 or VI > VDD) ..... ±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3) ..... 200 mA

Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3) ..... 200 mA

Maximum current sunk by PORTC and PORTD (combined) (Note 3) ..... 200 mA

Maximum current sourced by PORTC and PORTD (combined) (Note 3) ..... 200 mA

**Note 1:** Power dissipation is calculated as follows: Pdis = VDD x {IDD - ∑ IOH} + ∑ {(VDD - VOH) x IOH} + ∑(Vol x IOL)

**Note 2:** Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

**Note 3:** PORTD and PORTE are not implemented on the PIC16C73.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 18-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

| OSC | PIC16C73-04<br>PIC16C74-04 | PIC16C73-10<br>PIC16C74-10 | PIC16C73-20<br>PIC16C74-20 | PIC16LC73-04<br>PIC16LC74-04 | JW Devices |
|---|---|---|---|---|---|
| RC | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 3.0V to 6.0V<br>IDD: 3.8 mA max. at 3.0V<br>IPD: 13.5 µA max. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. |
| XT | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 3.0V to 6.0V<br>IDD: 3.8 mA max. at 3.0V<br>IPD: 13.5 µA max. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V<br>IDD: 13.5 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 15 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 10 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 20 MHz max. | Not recommended for use in HS mode | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 20 MHz max. |
| LP | VDD: 4.0V to 6.0V<br>IDD: 52.5 µA typ. at 32 kHz, 4.0V<br>IPD: 0.9 µA typ. at 4.0V<br>Freq: 200 kHz max. | Not recommended for use in LP mode | Not recommended for use in LP mode | VDD: 3.0V to 6.0V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 13.5 µA max. at 3.0V<br>Freq: 200 kHz max. | VDD: 3.0V to 6.0V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 13.5 µA max. at 3.0V<br>Freq: 200 kHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications.
It is recommended that the user select the device type that ensures the specifications required.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### 18.3 DC Characteristics: PIC16C73/74-04 (Commercial, Industrial)
### PIC16C73/74-10 (Commercial, Industrial)
### PIC16C73/74-20 (Commercial, Industrial)
### PIC16LC73/74-04 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial<br>Operating voltage VDD range as described in DC spec Section 18.1 and Section 18.2. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ †** | **Max** | **Units** | **Conditions** |
| | **Input Low Voltage** | | | | | | |
| | I/O ports | VIL | | | | | |
| D030 | with TTL buffer | | VSS | - | 0.15VDD | V | For entire VDD range |
| D030A | | | VSS | - | 0.8V | V | 4.5V ≤ VDD ≤ 5.5V |
| D031 | with Schmitt Trigger buffer | | VSS | - | 0.2VDD | V | |
| D032 | $\overline{MCLR}$, OSC1 (in RC mode) | | VSS | - | 0.2VDD | V | |
| D033 | OSC1 (in XT, HS and LP) | | VSS | - | 0.3VDD | V | Note1 |
| | **Input High Voltage** | | | | | | |
| | I/O ports | VIH | | - | | | |
| D040 | with TTL buffer | | 2.0 | - | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D040A | | | 0.25VDD + 0.8V | - | VDD | V | For entire VDD range |
| D041 | with Schmitt Trigger buffer | | 0.8VDD | - | VDD | V | For entire VDD range |
| D042 | $\overline{MCLR}$ | | 0.8VDD | - | VDD | V | |
| D042A | OSC1 (XT, HS and LP) | | 0.7VDD | - | VDD | V | Note1 |
| D043 | OSC1 (in RC mode) | | 0.9VDD | - | VDD | V | |
| D070 | PORTB weak pull-up current | IPURB | 50 | 250 | 400 | µA | VDD = 5V, VPIN = VSS |
| | **Input Leakage Current** (Notes 2, 3) | | | | | | |
| D060 | I/O ports | IIL | - | - | ±1 | µA | Vss ≤ VPIN ≤ VDD, Pin at hi-impedance |
| D061 | $\overline{MCLR}$, RA4/T0CKI | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD |
| D063 | OSC1 | | - | - | ±5 | µA | Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration |
| | **Output Low Voltage** | | | | | | |
| D080 | I/O ports | VOL | - | - | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C |
| D083 | OSC2/CLKOUT (RC osc config) | | - | - | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C |
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports (Note 3) | VOH | VDD - 0.7 | - | - | V | IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C |
| D092 | OSC2/CLKOUT (RC osc config) | | VDD - 0.7 | - | - | V | IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C |
| D150* | **Open-Drain High Voltage** | VOD | - | - | 14 | V | RA4 pin |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### 18.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST ($I^2C$ specifications only)
4. Ts ($I^2C$ specifications only)

| | | | |
|---|---|---|---|
| **T** | | | |
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

| | | | |
|---|---|---|---|
| **pp** | | | |
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | $\overline{RD}$ |
| cs | $\overline{CS}$ | rw | $\overline{RD}$ or $\overline{WR}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{SS}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O port | t1 | T1CKI |
| mc | $\overline{MCLR}$ | wr | $\overline{WR}$ |

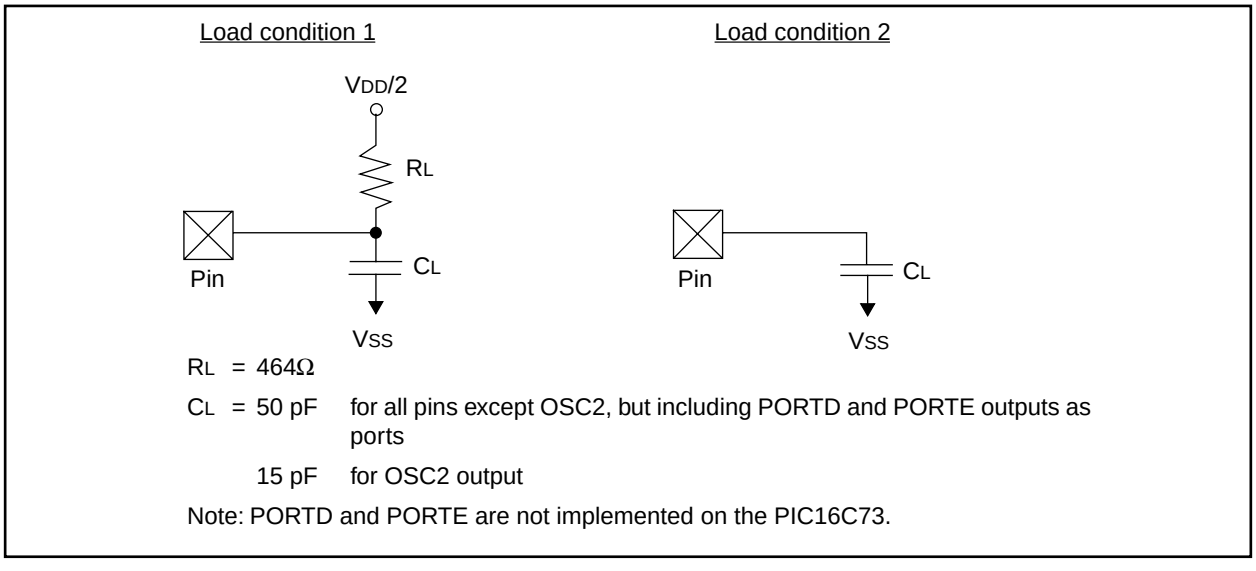
Uppercase letters and their meanings:

| | | | |
|---|---|---|---|
| **S** | | | |
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (Hi-impedance) | V | Valid |
| L | Low | Z | Hi-impedance |
| **$I^2C$ only** | | | |
| AA | output access | High | High |
| BUF | Bus free | Low | Low |

TCC:ST ($I^2C$ specifications only)

| | | | |
|---|---|---|---|
| **CC** | | | |
| HD | Hold | SU | Setup |
| **ST** | | | |
| DAT | DATA input hold | STO | STOP condition |
| STA | START condition | | |

**FIGURE 18-1: LOAD CONDITIONS**




$R_L$ = 464Ω

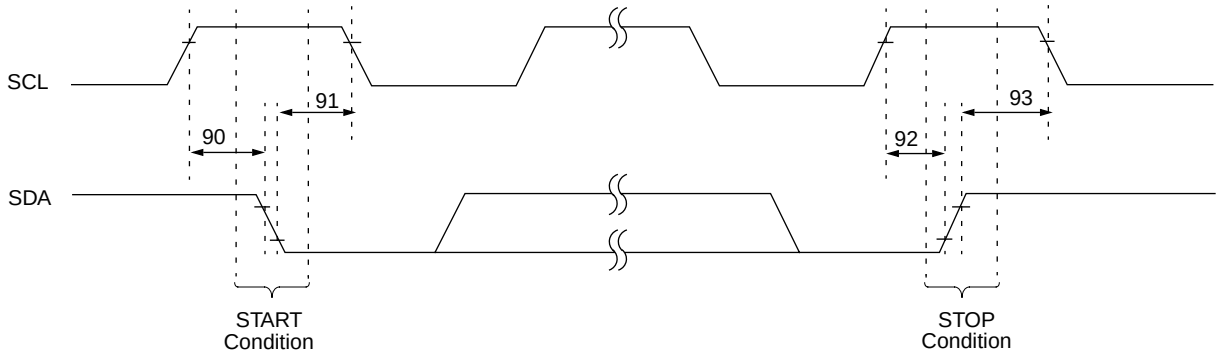
$C_L$ = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports

15 pF for OSC2 output

Note: PORTD and PORTE are not implemented on the PIC16C73.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

**FIGURE 18-9: $I^2C$ BUS START/STOP BITS TIMING**




Note: Refer to Figure 18-1 for load conditions

**TABLE 18-9: $I^2C$ BUS START/STOP BITS REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 90 | TSU:STA | START condition Setup time | 100 kHz mode | 4700 | — | — | ns | Only relevant for repeated START condition |
| | | | 400 kHz mode | 600 | — | — | | |
| 91 | THD:STA | START condition Hold time | 100 kHz mode | 4000 | — | — | ns | After this period the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | — | | |
| 92 | TSU:STO | STOP condition Setup time | 100 kHz mode | 4700 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |
| 93 | THD:STO | STOP condition Hold time | 100 kHz mode | 4000 | — | — | ns | |
| | | | 400 kHz mode | 600 | — | — | | |

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

**DC CHARACTERISTICS**

**Standard Operating Conditions (unless otherwise stated)**
Operating temperature -40˚C ≤ TA ≤ +125˚C for extended,
-40˚C ≤ TA ≤ +85˚C for industrial and
0˚C ≤ TA ≤ +70˚C for commercial
Operating voltage VDD range as described in DC spec Section 19.1 and Section 19.2.

| Param No. | Characteristic | Sym | Min | Typ † | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | **Output High Voltage** | | | | | | |
| D090 | I/O ports (Note 3) | VOH | VDD - 0.7 | - | - | V | IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C |
| D090A | | | VDD - 0.7 | - | - | V | IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C |
| D092 | OSC2/CLKOUT (RC osc config) | | VDD - 0.7 | - | - | V | IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C |
| D092A | | | VDD - 0.7 | - | - | V | IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C |
| D150* | **Open-Drain High Voltage** | VOD | - | - | 14 | V | RA4 pin |
| | **Capacitive Loading Specs on Output Pins** | | | | | | |
| D100 | OSC2 pin | COSC2 | - | - | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins and OSC2 (in RC | CIO | - | - | 50 | pF | |
| D102 | mode) SCL, SDA in $I^2C$ mode | CB | - | - | 400 | pF | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

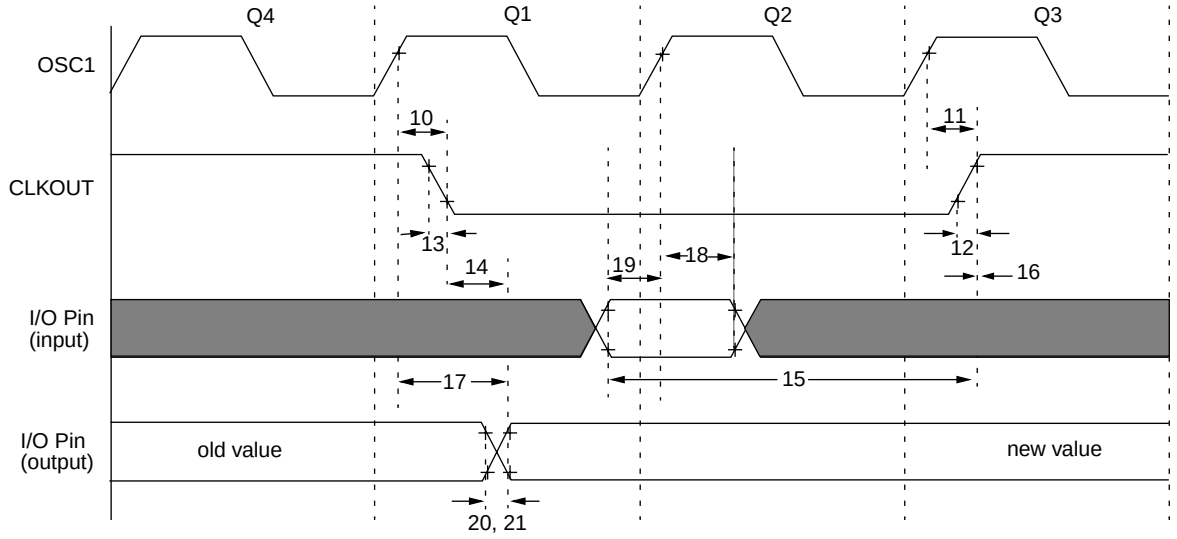
Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

**FIGURE 20-3: CLKOUT AND I/O TIMING**




Note: Refer to Figure 20-1 for load conditions.

**TABLE 20-3: CLKOUT AND I/O TIMING REQUIREMENTS**

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10* | TosH2ckL | OSC1↑ to CLKOUT↓ | | — | 75 | 200 | ns | Note 1 |
| 11* | TosH2ckH | OSC1↑ to CLKOUT↑ | | — | 75 | 200 | ns | Note 1 |
| 12* | TckR | CLKOUT rise time | | — | 35 | 100 | ns | Note 1 |
| 13* | TckF | CLKOUT fall time | | — | 35 | 100 | ns | Note 1 |
| 14* | TckL2ioV | CLKOUT ↓ to Port out valid | | — | — | 0.5TCY + 20 | ns | Note 1 |
| 15* | TioV2ckH | Port in valid before CLKOUT ↑ | | TOSC + 200 | — | — | ns | Note 1 |
| 16* | TckH2ioI | Port in hold after CLKOUT ↑ | | 0 | — | — | ns | Note 1 |
| 17* | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid | | — | 50 | 150 | ns | |
| 18* | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | PIC16**C**76/77 | 100 | — | — | ns | |
| | | | PIC16**LC**76/77 | 200 | — | — | ns | |
| 19* | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | | 0 | — | — | ns | |
| 20* | TioR | Port output rise time | PIC16**C**76/77 | — | 10 | 40 | ns | |
| | | | PIC16**LC**76/77 | — | — | 80 | ns | |
| 21* | TioF | Port output fall time | PIC16**C**76/77 | — | 10 | 40 | ns | |
| | | | PIC16**LC**76/77 | — | — | 80 | ns | |
| 22††* | Tinp | INT pin high or low time | | TCY | — | — | ns | |
| 23††* | Trbp | RB7:RB4 change INT high or low time | | TCY | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

**FIGURE 21-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)**

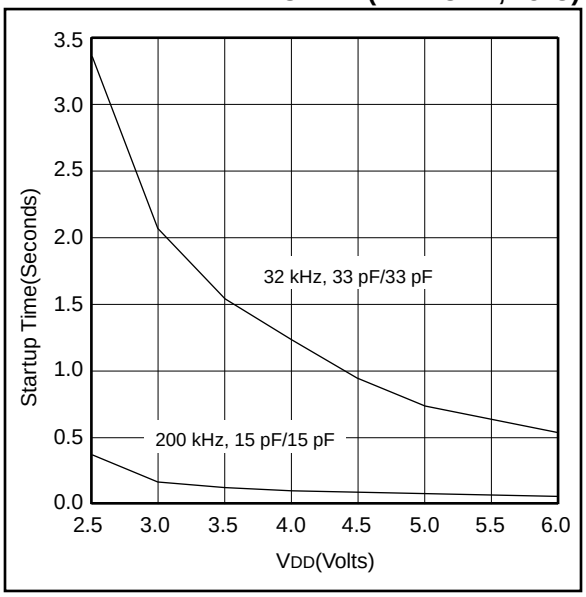



**FIGURE 21-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)**

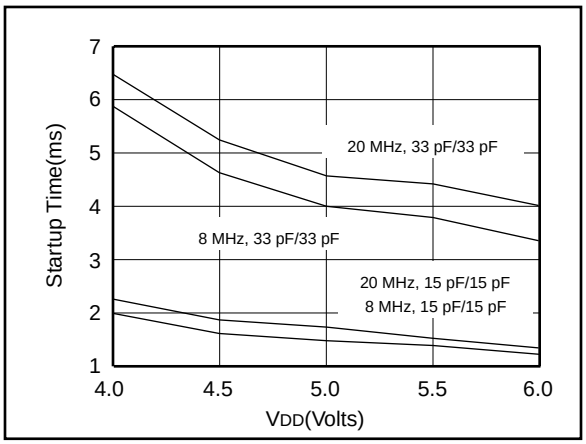



**FIGURE 21-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)**

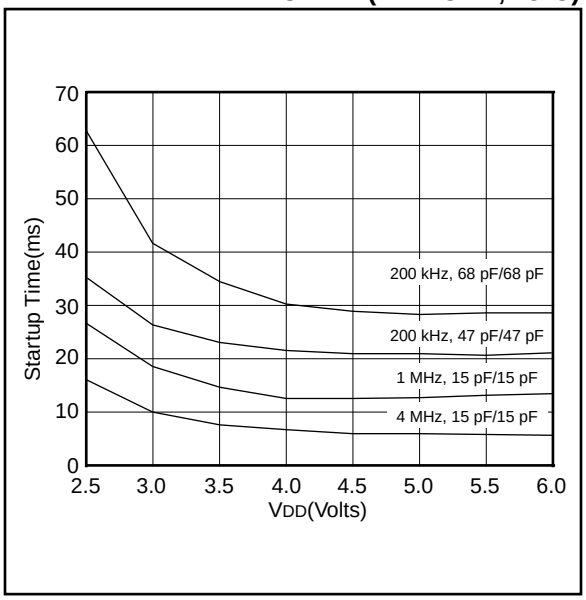



**TABLE 21-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS**

| Osc Type | Crystal Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz | 33 pF | 33 pF |
| | 200 kHz | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
| | 8 MHz | 15-33 pF | 15-33 pF |
| | 20 MHz | 15-33 pF | 15-33 pF |
| | | | |
| **Crystals Used** | | | |
| 32 kHz | Epson C-001R32.768K-A | | ± 20 PPM |
| 200 kHz | STD XTL 200.000KHz | | ± 20 PPM |
| 1 MHz | ECS ECS-10-13-1 | | ± 50 PPM |
| 4 MHz | ECS ECS-40-20-1 | | ± 50 PPM |
| 8 MHz | EPSON CA-301 8.000M-C | | ± 30 PPM |
| 20 MHz | EPSON CA-301 20.000M-C | | ± 30 PPM |

Data based on matrix samples. See first page of this section for details.

## D



## E



## F



## G



## I