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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c73at-04-so

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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. The special function registers can be classified into two sets (core and peripheral). Those registers associated with the "core" functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (3)
Bank 0											
00h ⁽¹⁾	INDF	Addressing	this location	uses conten	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect data	a memory ad	dress pointe	er					XXXX XXXX	uuuu uuuu
05h	PORTA	—	—	PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read		0x 0000	0u 0000
06h	PORTB	PORTB Dat	a Latch whe	n written: PC	ORTB pins wh	nen read				xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Dat	ta Latch whe	n written: PC	ORTC pins w	nen read				xxxx xxxx	uuuu uuuu
08h	_	Unimpleme	nted							—	—
09h	_	Unimpleme	nted							_	_
0Ah ^(1,2)	PCLATH	_	- — Write Buffer for the upper 5 bits of the Program Counter							0 0000	0 0000
0Bh (1)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
0Dh	_	Unimpleme	Inimplemented							—	_
0Eh	TMR1L	Holding reg	Holding register for the Least Significant Byte of the 16-bit TMR1 register							xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the N	Aost Signific	ant Byte of th	ne 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	is Serial Port	Receive Bu	ffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	Register (LS	SB)					xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	Register (M	SB)					XXXX XXXX	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	_	Unimpleme	nted							_	_
19h	_	Unimpleme	nted							_	_
1Ah	-	Unimpleme	nted							—	_
1Bh	_	Unimpleme	nted							_	_
1Ch	_	Unimpleme	nted							_	_
1Dh	_	Unimpleme	nted							_	_
1Eh	ADRES	A/D Result	Register							xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	0000 00-0

TABLE 4-1: PIC16C72 SPECIAL FUNCTION REGISTER SUMMARY

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C72, always maintain these bits clear.

									, en,		
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 2								•	•		
100h ⁽⁴⁾	INDF	Addressing	this location	uses conter	nts of FSR to a	ddress data ı	memory (not	a physical re	egister)	0000 0000	0000 0000
101h	TMR0	Timer0 mod	dule's registe	r						xxxx xxxx	uuuu uuuu
102h ⁽⁴⁾	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000
103h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
104h ⁽⁴⁾	FSR	Indirect dat	a memory ac	dress pointe	er	1			1	xxxx xxxx	uuuu uuuu
105h	_	Unimpleme	nted							_	_
106h	PORTB	PORTB Da	ta Latch whe	n written: PC	ORTB pins whe	en read				xxxx xxxx	uuuu uuuu
107h	—	Unimpleme	nted							—	—
108h	—	Unimpleme		—	—						
109h	—	Unimpleme	nted		—	—					
10Ah ^(1,4)	PCLATH	—	— — Write Buffer for the upper 5 bits of the Program Counter								0 0000
10Bh (4)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
10Ch- 10Fh	_	Unimpleme	nted	•	_	_					
Bank 3											
180h ⁽⁴⁾	INDF	Addressing	this location	uses conter	nts of FSR to a	ddress data ı	memory (not	a physical re	egister)	0000 0000	0000 0000
181h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h ⁽⁴⁾	PCL	Program Co	ounter's (PC)	Least Sigr	nificant Byte			•	•	0000 0000	0000 0000
183h ⁽⁴⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	с	0001 1xxx	000q quuu
184h ⁽⁴⁾	FSR	Indirect dat	a memory ac	dress pointe	er			1		xxxx xxxx	uuuu uuuu
185h	_	Unimpleme	nted							_	_
186h	TRISB	PORTB Da	ta Direction F	Register						1111 1111	1111 1111
187h	_	Unimpleme	nted							_	_
188h	_	Unimpleme	nted							_	_
189h	—	Unimpleme	nted							—	—
18Ah ^(1,4)	PCLATH	_	_	_	Write Buffer f	or the upper	5 bits of the	Program Cou	Inter	0 0000	0 0000
18Bh ⁽⁴⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
18Ch- 18Fh	_	Unimpleme	nted							_	_

TABLE 4-3: PIC16C76/77 SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

 $\label{eq:logarder} \begin{array}{ll} \mbox{Legend:} & x = \mbox{unknown}, \mbox{u} = \mbox{unknown}, \mbox{q} = \mbox{value depends on condition, $-$ = unimplemented read as '0'.} \\ & \mbox{Shaded locations are unimplemented, read as '0'.} \end{array}$

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the PIC16C76, always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD and PORTE are not physically implemented on the PIC16C76, read as '0'.

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

ORG 0x5	00	
BSF	pclath,3	;Select page 1 (800h-FFFh)
BCF	pclath,4	;Only on >4K devices
CALL	SUB1_P1	;Call subroutine in
	:	;page 1 (800h-FFFh)
	:	
	:	
ORG 0x9	00	
SUB1_P1	:	;called subroutine
	:	;page 1 (800h-FFFh)
	:	
RETURN		<pre>;return to Call subroutine ;in page 0 (000h-7FFh)</pre>

4.5 <u>Indirect Addressing, INDF and FSR</u> <u>Registers</u>

Ap	pli	cabl	e D	evi	ces	
72	73	73A	74	74A	76	77

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-18.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

	movlw movwf	0x20 FSR	;initialize pointer ;to RAM
NEXT	clrf	INDF	;clear INDF register
	incf	FSR,F	;inc pointer
	btfss	FSR,4	;all done?
	goto	NEXT	;no clear next
CONTINUE			
	:		;yes continue

FIGURE 4-18: DIRECT/INDIRECT ADDRESSING



8.1 <u>Timer1 Operation in Timer Mode</u>

Applicable Devices

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is FOSC/4. The synchronize control bit T1SYNC (T1CON<2>) has no effect since the internal clock is always in sync.

8.2 <u>Timer1 Operation in Synchronized</u> Counter Mode Applicable Devices 72 73 73A 74 74A 76 77

Counter mode is selected by setting bit TMR1CS. In this mode the timer increments on every rising edge of clock input on pin RC1/T1OSI/CCP2 when bit T1OSCEN is set or pin RC0/T1OSO/T1CKI when bit T1OSCEN is cleared.

If T1SYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple-counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if the external clock is present, since the synchronization circuit is shut off. The prescaler however will continue to increment.

8.2.1 EXTERNAL CLOCK INPUT TIMING FOR SYNCHRONIZED COUNTER MODE

When an external clock input is used for Timer1 in synchronized counter mode, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of TMR1 after synchronization.

When the prescaler is 1:1, the external clock input is the same as the prescaler output. The synchronization of T1CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T1CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the appropriate electrical specifications, parameters 45, 46, and 47.

When a prescaler other than 1:1 is used, the external clock input is divided by the asynchronous ripplecounter type prescaler so that the prescaler output is symmetrical. In order for the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T1CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T1CKI high and low time is that they do not violate the minimum pulse width requirements of 10 ns). Refer to the appropriate electrical specifica-tions, parameters 40, 42, 45, 46, and 47.



FIGURE 8-2: TIMER1 BLOCK DIAGRAM

TABLE 10-5:	REGISTERS	ASSOCIATED	WITH PWM	AND TIMER2
-------------	-----------	------------	----------	------------

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ^(1,2)	ADIF	RCIF ⁽²⁾	TXIF ⁽²⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh ⁽²⁾	PIR2	—	_	_	—	—	—	_	CCP2IF	0	0
8Ch	PIE1	PSPIE ^(1,2)	ADIE	RCIE ⁽²⁾	TXIE ⁽²⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh ⁽²⁾	PIE2	—			—	—	—		CCP2IE	0	0
87h	TRISC	PORTC Da	ata Directio		1111 1111	1111 1111					
11h	TMR2	Timer2 mod	dule's regist		0000 0000	0000 0000					
92h	PR2	Timer2 mod	dule's period	l register						1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Co	mpare/PWI	V register1 ((LSB)					xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWI	V register1 ((MSB)					xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
1Bh ⁽²⁾	CCPR2L	Capture/Co	mpare/PWI	V register2 ((LSB)					xxxx xxxx	uuuu uuuu
1Ch ⁽²⁾	CCPR2H	Capture/Co	mpare/PWI	V register2 ((MSB)					xxxx xxxx	uuuu uuuu
1Dh ⁽²⁾	CCP2CON	—	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A/76, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port, USART or CCP2 module, these bits are unimplemented, read as '0'.

To enable the serial port, SSP enable bit SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear enable bit SSPEN, re-initialize SSPCON register, and then set enable bit SSPEN. This configures the SDI, SDO, SCK, and SS pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- <u>SS</u> must have TRISA<5> set (if implemented)

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and SS could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-4 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- Master sends data Slave sends data
- · Master sends dummy data Slave sends data

FIGURE 11-4: SPI MASTER/SLAVE CONNECTION

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor" mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched interrupt flag bit SSPIF (PIR1<3>) is set.

The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-5 and Figure 11-6 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or TCY)
- Fosc/16 (or 4 TCY)
- Fosc/64 (or 16 TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.



12.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. If bit BRGH (TXSTA<2>) is clear (i.e., at the low baud rates), the sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 12-3). If bit BRGH is set (i.e., at the high baud rates), the sampling is done on the 3 clock edges preceding the second rising edge after the first falling edge of a x4 clock (Figure 12-4 and Figure 12-5).

FIGURE 12-3: RX PIN SAMPLING SCHEME. BRGH = 0 (PIC16C73/73A/74/74A)



FIGURE 12-4: RX PIN SAMPLING SCHEME, BRGH = 1 (PIC16C73/73A/74/74A)







12.3 USART Synchronous Master Mode

Applicable Devices 72 73 73A 74 74A 76 77

In Synchronous Master mode, the data is transmitted in a half-duplex manner i.e. transmission and reception do not occur at the same time. When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

12.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 12-7. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG is empty and interrupt bit, TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 12-12). The transmission can also be started by first loading the TXREG register and then setting bit TXEN (Figure 12-13). This is advantageous when slow baud rates are selected, since the BRG is kept in reset when bits TXEN, CREN, and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing enable bit TXEN, during a transmission, will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to hi-impedance. If either bit CREN or bit SREN is set, during a transmission, the transmission is aborted and the DT pin reverts to a hi-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic however is not reset although it is disconnected from the pins. In order to reset the transmitter, the user has to clear bit TXEN. If bit SREN is set (to interrupt an on-going transmission and receive a single word), then after the single word is received, bit SREN will be cleared and the serial port will revert back to transmitting since bit TXEN is still set. The DT line will immediately switch from hi-impedance receive mode to transmit and start driving. To avoid this, bit TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 12.1).
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
- 3. If interrupts are desired, then set enable bit TXIE.
- 4. If 9-bit transmission is desired, then set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.

13.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

Applicable Devices

The analog-to-digital (A/D) converter module has five inputs for the PIC16C72/73/73A/76, and eight for the PIC16C74/74A/77.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 13-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 13-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

R/W-0	R/W-0 R/\	<u>W-0 R/W-</u>	0 R/W-0	R/W-0	U-0	R/W-0							
ADCS1	ADCS0 CH	IS2 CHS	1 CHS0	GO/DONE	—	ADON	R = Readable bit						
bit7						bit0	W = Writable bit						
							U = Unimplemented bit, read as '0'						
							- n = Value at POR reset						
bit 7-6:	ADCS1:ADCS	50: A/D Con	version Cloc	< Select bits									
	00 = Fosc/2												
	01 = Fosc/8												
	10 = FOSC/32 11 = FPC (clock derived from an internal PC oscillator)												
	$\perp \perp = FRC$ (CIO	ck derived fr	om an intern	al RC oscillato	r)								
bit 5-3:	CHS2:CHS0:	Analog Cha	nnel Select b	oits									
	000 = channe	ΙΟ, (RAU/AP 1 1 (RΔ1/ΔΝ	10) 11)										
	010 = channe	1 2, (RA2/AM	12)										
	011 = channe	I 3, (RA3/AN	J3)										
	100 = channe	I 4, (RA5/AN	14) (1)										
	101 = channe	15, (RE0/AN	15) ⁽¹⁾										
	110 = channe	10, (RE1/AN 17, (RE2/AN	10)(1)										
bit 2:	GO/DONE: A/	D Conversio	on Status bit										
	If ADON = 1												
	1 = A/D conve	rsion in pro	gress (setting	this bit starts	the A/D co	onversion)							
	0 = A/D conve	rsion not in p	rogress (Thi	s bit is automat	ically clear	red by hardwa	are when the A/D conversion						
	is complete)												
bit 1:	Unimplement	ted: Read as	s '0'										
bit 0:	ADON: A/D O	n bit											
	1 = A/D conve	rter module	is operating										
	u = A/D conve	rter module	is snutoff an	a consumes n	o operating	g current							
Note 1:	A/D channels	5, 6, and 7	are impleme	nted on the PIC	C16C74/74	4A/77 only.							
			· ·										

FIGURE 13-1: ADCON0 REGISTER (ADDRESS 1Fh)

13.1 A/D Acquisition Requirements

Applicable Devices 72 73 73 74 74 76 77

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 13-4. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), Figure 13-4. The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 10 k Ω . After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 13-1 may be used. This equation calculates the acquisition time to within 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

EQUATION 13-1: A/D MINIMUM CHARGING TIME

 $VHOLD = (VREF - (VREF/512)) \bullet (1 - e^{(-TCAP/CHOLD(RIC + RSS + RS))})$

Given: VHOLD = (VREF/512), for 1/2 LSb resolution

The above equation reduces to:

 $TCAP = -(51.2 \text{ pF})(1 \text{ k}\Omega + \text{Rss} + \text{Rs}) \ln(1/511)$

Example 13-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

CHOLD = 51.2 pF

Rs = 10 kΩ

1/2 LSb error

FIGURE 13-4: ANALOG INPUT MODEL

 $VDD = 5V \rightarrow Rss = 7 \text{ k}\Omega$

Temp (application system max.) = 50°C

VHOLD = 0 @ t = 0

- Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.
- Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **Note 3:** The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.
- Note 4: After a conversion has completed, a 2.0TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 13-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

- TACQ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient
- TACQ = $5 \mu s + TCAP + [(Temp 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$
- TCAP = -CHOLD (Ric + Rss + Rs) ln(1/511)-51.2 pF (1 k Ω + 7 k Ω + 10 k Ω) ln(0.0020) -51.2 pF (18 k Ω) ln(0.0020) -0.921 µs (-6.2364) 5.747 µs
- TACQ = 5 μs + 5.747 μs + [(50°C 25°C)(0.05 μs/°C)] 10.747 μs + 1.25 μs 11.997 μs



13.2 <u>Selecting the A/D Conversion Clock</u> Applicable Devices

72 73 73A 74 74A 76 77

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5TAD per 8-bit conversion. The source of the A/D conversion clock is software selectable. The four possible options for TAD are:

- 2Tosc
- 8Tosc
- 32Tosc
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 $\mu s.$

Table 13-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

13.3 Configuring Analog Port Pins Applicable Devices 72/73/73A/74/74A/76/77

The ADCON1, TRISA, and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

- Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.
- **Note 2:** Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

AD Clock S	ource (TAD)	Device Frequency								
Operation	ADCS1:ADCS0	20 MHz	5 MHz	1.25 MHz	333.33 kHz					
2Tosc	00	100 ns ⁽²⁾	400 ns ⁽²⁾	1.6 μs	6 µs					
8Tosc	01	400 ns ⁽²⁾	1.6 μs	6.4 μs	24 μs ⁽³⁾					
32Tosc	10	1.6 μs	6.4 μs	25.6 μs ⁽³⁾	96 μs ⁽³⁾					
RC ⁽⁵⁾	11	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ⁽¹⁾					

TABLE 13-1: TAD vs. DEVICE OPERATING FREQUENCIES

Legend: Shaded cells are outside of recommended range.

- 2: These values violate the minimum required TAD time.
- 3: For faster conversion times, the selection of another clock source is recommended.
- 4: When device frequency is greater than 1 MHz, the RC A/D conversion clock source is recommended for sleep operation only.
- 5: For extended voltage devices (LC), please refer to Electrical Specifications section.

Note 1: The RC source has a typical TAD time of 4 μ s.

17.1 DC Characteristics: PIC16C72-04 (Commercial, Industrial, Extended) PIC16C72-10 (Commercial, Industrial, Extended) PIC16C72-20 (Commercial, Industrial, Extended)

			Standard Operating Conditions (unless otherwise stated)							
DC CHA	RACTERISTICS		Operat	ing tem	peratu	re -4۔ 1-	10° C \leq IA \leq +125 °C for extended, 10° C \leq TA \leq +85 °C for industrial and			
						0°	$C \leq TA \leq +70^{\circ}C$ for commercial			
Param No.	Characteristic	Sym	Min	Тур†	Мах	Units	Conditions			
D001 D001A	Supply Voltage	Vdd	4.0 4.5	-	6.0 5.5	> >	XT, RC and LP osc configuration HS osc configuration			
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V				
D003	VDD start voltage to ensure internal Power- on Reset Signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details			
D004*	VDD rise rate to ensure internal Power-on Reset Signal	Svdd	0.05	-	-	V/ms	See section on Power-on Reset for details			
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN bit in configuration word enabled			
			3.7	4.0	4.4	V	Extended Only			
D010	Supply Current (Note 2,5)	IDD	-	2.7	5.0	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4)			
D013			-	10	20	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V			
D015	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled VDD = 5.0V			
D020	Power-down Current	IPD	-	10.5	42	μΑ	VDD = 4.0V, WDT enabled, -40° C to $+85^{\circ}$ C			
D021	(Note 3,5)		-	1.5	16	μA	$VDD = 4.0V$, WDT disabled, $-0^{\circ}C$ to $+70^{\circ}C$			
D021A				1.5	19	μΑ μΑ	$VDD = 4.0V$, VDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$			
D023	Brown-out Reset Current (Note 6)	Δ IBOR	-	350	425	μA	BOR enabled VDD = 5.0V			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD \overline{MCLR} = VDD; WDT enabled/disabled as specified.

The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VbD and Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

 Applicable Devices
 72
 73
 73A
 74
 74A
 76
 77

FIGURE 18-7: PARALLEL SLAVE PORT TIMING (PIC16C74)



TABLE 18-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C74)

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
62	TdtV2wrH	Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time)		20	_	_	ns	
63*	TwrH2dtl	\overline{WR}^{\uparrow} or \overline{CS}^{\uparrow} to data–in invalid (hold time)	PIC16 C 74	20	—	—	ns	
			PIC16 LC 74	35	—	—	ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data–out valid	-	—	80	ns		
65	TrdH2dtl	\overline{RD} or \overline{CS} to data–out invalid		10	_	30	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 19-5: BROWN-OUT RESET TIMING



TABLE 19-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER,
AND BROWN-OUT RESET REQUIREMENTS

Parameter	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
No.							
30	TmcL	MCLR Pulse Width (low)	2	_	_	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	_	1024Tosc	_	-	Tosc = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tıoz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	_	—	2.1	μs	
35	TBOR	Brown-out Reset pulse width	100	—	_	μs	$VDD \le BVDD (D005)$

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 19-13: A/D CONVERTER CHARACTERISTICS:

PIC16C73A/74A-04 (Commercial, Industrial, Extended) PIC16C73A/74A-10 (Commercial, Industrial, Extended) PIC16C73A/74A-20 (Commercial, Industrial, Extended) PIC16LC73A/74A-04 (Commercial, Industrial)

Param No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
A01	Nr	Resolution	Resolution		—	8-bits	bit	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A02	Eabs	Total Absolute error		_	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$
A03	EIL	Integral linearity error		_	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$
A04	Edl	Differential linearity error		—	—	<±1	LSb	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A05	Efs	Full scale error		—	—	<±1	LSb	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A06	Eoff	Offset error		_	_	<±1	LSb	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A10	_	Monotonicity			guaranteed	—	—	$VSS \leq VAIN \leq VREF$
A20	Vref	Reference voltage		3.0V	—	VDD + 0.3	V	
A25	VAIN	Analog input voltage		Vss - 0.3	—	Vref + 0.3	V	
A30	Zain	Recommended impedar analog voltage source	ice of	_	—	10.0	kΩ	
A40	IAD	A/D conversion current	PIC16 C 73A/74A	—	180	_	μA	Average current consump-
		(VDD)	PIC16 LC 73A/74A	_	90	_	μA	tion when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)		10	—	1000	μΑ	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 13.1.
					_	10	μΑ	cycle

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

20.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2	ppS	3. TCC:ST	(I ² C specifications only)				
2. TppS		4. Ts	(I ² C specifications only)				
Т							
F	Frequency	Т	Time				
Lower	case letters (pp) and their meanings:						
рр							
сс	CCP1	osc	OSC1				
ck	CLKOUT	rd	RD				
CS	CS	rw	RD or WR				
di	SDI	sc	SCK				
do	SDO	SS	SS				
dt	Data in	tO	TOCKI				
io	I/O port	t1	T1CKI				
mc	MCLR	wr	WR				
Upper	case letters and their meanings:						
S							
F	Fall	P	Period				
H	High	R	Rise				
	Invalid (Hi-impedance)	V	Valid				
L	Low	Z	Hi-impedance				
I ² C only							
AA	output access	High	High				
BUF	Bus free	Low	Low				
Tcc:st	(I ² C specifications only)	_					
CC							
HD	Hold	SU	Setup				
ST							
DAT	DATA input hold	STO	STOP condition				
STA	START condition						
FIGURE	20-1: LOAD CONDITIONS						
			Logd condition 2				
	Load condition 1		Load condition 2				
VDD/2 RL							
	Pin	P					
	VSS Vee						
	PL - 4640						
	CL = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports						
	15 pF for OSC2 output						
Note: PORTD and PORTE are not implemented on the PIC16C76.							

TABLE 20-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input	Тсү	_	_	ns	
71*	TscH	SCK input high time (slave mode)	Tcy + 20	_	_	ns	
72*	TscL	SCK input low time (slave mode)	Tcy + 20	_	_	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75*	TdoR	SDO data output rise time	_	10	25	ns	
76*	TdoF	SDO data output fall time	_	10	25	ns	
77*	TssH2doZ	SS↑ to SDO output hi-impedance	10	_	50	ns	
78*	TscR	SCK output rise time (master mode)	_	10	25	ns	
79*	TscF	SCK output fall time (master mode)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	_	—	50	ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	Тсү	—	—	ns	
82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	—	—	50	ns	
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK edge	1.5Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

E.3 PIC16C15X Family of Devices

		PIC16C154	PIC16CR154	PIC16C156	PIC16CR156	PIC16C158	PIC16CR158
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x12 words)	512		1K		2К	—
Memory	ROM Program Memory (x12 words)	—	512	_	1K		2К
	RAM Data Memory (bytes)	25	25	25	25	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	12	12	12
	Voltage Range (Volts)	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5
Features	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC; 20-pin SSOP					

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

E.4 PIC16C5X Family of Devices

		PIC16C52	PIC16C54	PIC16C54A	PIC16CR54A	PIC16C55	PIC16C56
Clock	Maximum Frequency of Operation (MHz)	4	20	20	20	20	20
	EPROM Program Memory (x12 words)	384	512	512	—	512	1K
Memory	ROM Program Memory (x12 words)	—	—	—	512	—	—
	RAM Data Memory (bytes)	25	25	25	25	24	25
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	12	20	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.0-6.25	2.5-6.25	2.5-6.25
Features	Number of Instructions	33	33	33	33	33	33
reatures	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP

		PIC16C57	PIC16CR57B	PIC16C58A	PIC16CR58A
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20
	EPROM Program Memory (x12 words)	2К	_	2K	_
Memory	ROM Program Memory (x12 words)	_	2K	_	2K
	RAM Data Memory (bytes)	72	72	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	I/O Pins	20	20	12	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.5-6.25
Features	Number of Instructions	33	33	33	33
	Packages	28-pin DIP, SOIC, SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

E.8 PIC16C8X Family of Devices

		PIC16F83	PIC16CR83	PIC16F84	PIC16CR84
Clock	Maximum Frequency of Operation (MHz)	10	10	10	10
	Flash Program Memory	512	—	1K	_
	EEPROM Program Memory	—	—	—	—
Memory	ROM Program Memory	—	512	—	1K
	Data Memory (bytes)	36	36	68	68
	Data EEPROM (bytes)	64	64	64	64
Peripher- als	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	Interrupt Sources	4	4	4	4
	I/O Pins	13	13	13	13
Features	Voltage Range (Volts)	2.0-6.0	2.0-6.0	2.0-6.0	2.0-6.0
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C8X Family devices use serial programming with clock pin RB6 and data pin RB7.

E.9 PIC16C9XX Family Of Devices

		PIC16C923	PIC16C924
Clock	Maximum Frequency of Operation (MHz)	8	8
Momony	EPROM Program Memory	4K	4K
Clock M Memory D Peripherals ((A L Features I F	Data Memory (bytes)	176	176
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Module(s)	1	1
	Serial Port(s) (SPI/I ² C, USART)	SPI/I ² C	SPI/I ² C
	Parallel Slave Port	—	—
	A/D Converter (8-bit) Channels	—	5
	LCD Module	4 Com, 32 Seg	4 Com, 32 Seg
	Interrupt Sources	8	9
	I/O Pins	25	25
	Input Pins	27	27
	Voltage Range (Volts)	3.0-6.0	3.0-6.0
Features	In-Circuit Serial Programming	Yes	Yes
	Brown-out Reset	—	—
	Packages	64-pin SDIP ⁽¹⁾ , TQFP; 68-pin PLCC, Die	64-pin SDIP ⁽¹⁾ , TQFP; 68-pin PLCC, Die

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C9XX Family devices use serial programming with clock pin RB6 and data pin RB7.

NOTES: