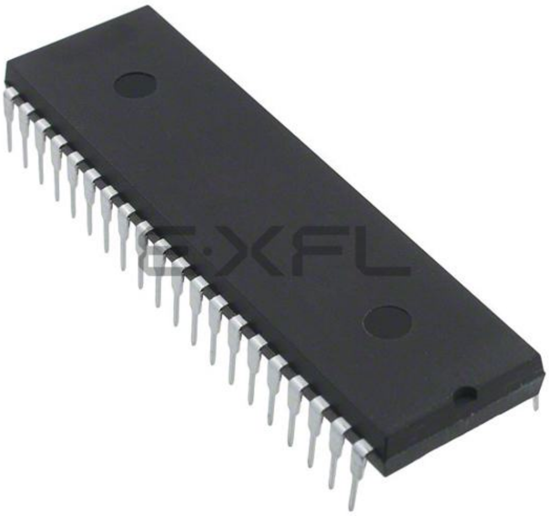
# Microchip Technology - PIC16C74A-20I/P Datasheet



| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 192 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 6V |
| Data Converters | A/D 8x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c74a-20i-p |

### TABLE 1-1: PIC16C7XX FAMILY OF DEVCES

| | | PIC16C710 | PIC16C71 | PIC16C711 | PIC16C715 | PIC16C72 | PIC16CR72[1] |
|---|---|---|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 512 | 1K | 1K | 2K | 2K | — |
| | ROM Program Memory (14K words) | — | — | — | — | — | 2K |
| | Data Memory (bytes) | 36 | 36 | 68 | 128 | 128 | 128 |
| **Peripherals** | Timer Module(s) | TMR0 | TMR0 | TMR0 | TMR0 | TMR0,<br>TMR1,<br>TMR2 | TMR0,<br>TMR1,<br>TMR2 |
| | Capture/Compare/ PWM Module(s) | — | — | — | — | 1 | 1 |
| | Serial Port(s) (SPI/I$^2$C, USART) | — | — | — | — | SPI/I$^2$C | SPI/I$^2$C |
| | Parallel Slave Port | — | — | — | — | — | — |
| **Features** | A/D Converter (8-bit) Channels | 4 | 4 | 4 | 4 | 5 | 5 |
| | Interrupt Sources | 4 | 4 | 4 | 4 | 8 | 8 |
| | I/O Pins | 13 | 13 | 13 | 13 | 22 | 22 |
| | Voltage Range (Volts) | 3.0-6.0 | 3.0-6.0 | 3.0-6.0 | 3.0-5.5 | 2.5-6.0 | 3.0-5.5 |
| | In-Circuit Serial Programming | Yes | Yes | Yes | Yes | Yes | Yes |
| | Brown-out Reset | Yes | — | Yes | Yes | Yes | Yes |
| | Packages | 18-pin DIP, SOIC;<br>20-pin SSOP | 18-pin DIP, SOIC | 18-pin DIP, SOIC;<br>20-pin SSOP | 18-pin DIP, SOIC;<br>20-pin SSOP | 28-pin SDIP, SOIC, SSOP | 28-pin SDIP, SOIC, SSOP |

| | | PIC16C73A | PIC16C74A | PIC16C76 | PIC16C77 |
|---|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 4K | 4K | 8K | 8K |
| | Data Memory (bytes) | 192 | 192 | 368 | 368 |
| **Peripherals** | Timer Module(s) | TMR0,<br>TMR1,<br>TMR2 | TMR0,<br>TMR1,<br>TMR2 | TMR0,<br>TMR1,<br>TMR2 | TMR0,<br>TMR1,<br>TMR2 |
| | Capture/Compare/PWM Module(s) | 2 | 2 | 2 | 2 |
| | Serial Port(s) (SPI/I$^2$C, USART) | SPI/I$^2$C, USART | SPI/I$^2$C, USART | SPI/I$^2$C, USART | SPI/I$^2$C, USART |
| | Parallel Slave Port | — | Yes | — | Yes |
| | A/D Converter (8-bit) Channels | 5 | 8 | 5 | 8 |
| **Features** | Interrupt Sources | 11 | 12 | 11 | 12 |
| | I/O Pins | 22 | 33 | 22 | 33 |
| | Voltage Range (Volts) | 2.5-6.0 | 2.5-6.0 | 2.5-6.0 | 2.5-6.0 |
| | In-Circuit Serial Programming | Yes | Yes | Yes | Yes |
| | Brown-out Reset | Yes | Yes | Yes | Yes |
| | Packages | 28-pin SDIP, SOIC | 40-pin DIP;<br>44-pin PLCC, MQFP, TQFP | 28-pin SDIP, SOIC | 40-pin DIP;<br>44-pin PLCC, MQFP, TQFP |

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C7XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

### TABLE 4-3: PIC16C76/77 SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets (2) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 1** | | | | | | | | | | | |
| 80h(4) | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | `0000 0000` | `0000 0000` |
| 81h | OPTION | $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | `1111 1111` | `1111 1111` |
| 82h(4) | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | `0000 0000` | `0000 0000` |
| 83h(4) | STATUS | IRP | RP1 | RP0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | `0001 1xxx` | `000q quuu` |
| 84h(4) | FSR | Indirect data memory address pointer | | | | | | | | `xxxx xxxx` | `uuuu uuuu` |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | `--11 1111` | `--11 1111` |
| 86h | TRISB | PORTB Data Direction Register | | | | | | | | `1111 1111` | `1111 1111` |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | `1111 1111` | `1111 1111` |
| 88h(5) | TRISD | PORTD Data Direction Register | | | | | | | | `1111 1111` | `1111 1111` |
| 89h(5) | TRISE | IBF | OBF | IBOV | PSPMODE | — | PORTE Data Direction Bits | | | `0000 -111` | `0000 -111` |
| 8Ah(1,4) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | `---0 0000` | `---0 0000` |
| 8Bh(4) | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | `0000 000x` | `0000 000u` |
| 8Ch | PIE1 | PSPIE(3) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | `0000 0000` | `0000 0000` |
| 8Dh | PIE2 | — | — | — | — | — | — | — | CCP2IE | `---- ---0` | `---- ---0` |
| 8Eh | PCON | — | — | — | — | — | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | `---- --qq` | `---- --uu` |
| 8Fh | — | Unimplemented | | | | | | | | — | — |
| 90h | — | Unimplemented | | | | | | | | — | — |
| 91h | — | Unimplemented | | | | | | | | — | — |
| 92h | PR2 | Timer2 Period Register | | | | | | | | `1111 1111` | `1111 1111` |
| 93h | SSPADD | Synchronous Serial Port ($I^2C$ mode) Address Register | | | | | | | | `0000 0000` | `0000 0000` |
| 94h | SSPSTAT | SMP | CKE | D/$\overline{\text{A}}$ | P | S | R/$\overline{\text{W}}$ | UA | BF | `0000 0000` | `0000 0000` |
| 95h | — | Unimplemented | | | | | | | | — | — |
| 96h | — | Unimplemented | | | | | | | | — | — |
| 97h | — | Unimplemented | | | | | | | | — | — |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | `0000 -010` | `0000 -010` |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | `0000 0000` | `0000 0000` |
| 9Ah | — | Unimplemented | | | | | | | | — | — |
| 9Bh | — | Unimplemented | | | | | | | | — | — |
| 9Ch | — | Unimplemented | | | | | | | | — | — |
| 9Dh | — | Unimplemented | | | | | | | | — | — |
| 9Eh | — | Unimplemented | | | | | | | | — | — |
| 9Fh | ADCON1 | — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 | `---- -000` | `---- -000` |

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
2: Other (non power-up) resets include external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.
3: Bits PSPIE and PSPIF are reserved on the PIC16C76, always maintain these bits clear.
4: These registers can be addressed from any bank.
5: PORTD and PORTE are not physically implemented on the PIC16C76, read as '0'.

### 4.2.2.2 OPTION REGISTER

| Applicable Devices | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

**FIGURE 4-8: OPTION REGISTER (ADDRESS 81h, 181h)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |

bit7 bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

| Bit Value | TMR0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

### 7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

| **Note:** | To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled. |
|---|---|

### EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

Lines 2 and 3 do NOT have to be included if the final desired prescale value is other than 1:1. If 1:1 is final desired value, then a temporary prescale value is set in lines 2 and 3 and the final prescale value will be set in lines 10 and 11.

```
1)  BSF    STATUS, RP0   ;Bank 1
2)  MOVLW  b'xx0x0xxx'   ;Select clock source and prescale value of
3)  MOVWF  OPTION_REG    ;other than 1:1
4)  BCF    STATUS, RP0   ;Bank 0
5)  CLRF   TMR0          ;Clear TMR0 and prescaler
6)  BSF    STATUS, RP1   ;Bank 1
7)  MOVLW  b'xxxx1xxx'   ;Select WDT, do not change prescale value
8)  MOVWF  OPTION_REG    ;
9)  CLRWDT               ;Clears WDT and prescaler
10) MOVLW  b'xxxx1xxx'   ;Select new prescale value and WDT
11) MOVWF  OPTION_REG    ;
12) BCF    STATUS, RP0   ;Bank 0
```

To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 7-2.

### EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT               ;Clear WDT and prescaler
BSF     STATUS, RP0 ;Bank 1
MOVLW   b'xxxx0xxx' ;Select TMR0, new prescale value and
MOVWF   OPTION_REG  ;clock source
BCF     STATUS, RP0 ;Bank 0
```

### TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h,101h | TMR0 | Timer0 module’s register | | | | | | | | `xxxx xxxx` | `uuuu uuuu` |
| 0Bh,8Bh,<br>10Bh,18Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | `0000 000x` | `0000 000u` |
| 81h,181h | OPTION | $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | `1111 1111` | `1111 1111` |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | `--11 1111` | `--11 1111` |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

### TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

| BAUD RATE (K) | FOSC = 20 MHz | | | 16 MHz | | | 10 MHz | | | 7.16 MHz | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) |
| 9.6 | 9.615 | +0.16 | 129 | 9.615 | +0.16 | 103 | 9.615 | +0.16 | 64 | 9.520 | -0.83 | 46 |
| 19.2 | 19.230 | +0.16 | 64 | 19.230 | +0.16 | 51 | 18.939 | -1.36 | 32 | 19.454 | +1.32 | 22 |
| 38.4 | 37.878 | -1.36 | 32 | 38.461 | +0.16 | 25 | 39.062 | +1.7 | 15 | 37.286 | -2.90 | 11 |
| 57.6 | 56.818 | -1.36 | 21 | 58.823 | +2.12 | 16 | 56.818 | -1.36 | 10 | 55.930 | -2.90 | 7 |
| 115.2 | 113.636 | -1.36 | 10 | 111.111 | -3.55 | 8 | 125 | +8.51 | 4 | 111.860 | -2.90 | 3 |
| 250 | 250 | 0 | 4 | 250 | 0 | 3 | NA | - | - | NA | - | - |
| 625 | 625 | 0 | 1 | NA | - | - | 625 | 0 | 0 | NA | - | - |
| 1250 | 1250 | 0 | 0 | NA | - | - | NA | - | - | NA | - | - |

| BAUD RATE (K) | FOSC = 5.068 MHz | | | 4 MHz | | | 3.579 MHz | | | 1 MHz | | | 32.768 kHz | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) |
| 9.6 | 9.6 | 0 | 32 | NA | - | - | 9.727 | +1.32 | 22 | 8.928 | -6.99 | 6 | NA | - | - |
| 19.2 | 18.645 | -2.94 | 16 | 1.202 | +0.17 | 207 | 18.643 | -2.90 | 11 | 20.833 | +8.51 | 2 | NA | - | - |
| 38.4 | 39.6 | +3.12 | 7 | 2.403 | +0.13 | 103 | 37.286 | -2.90 | 5 | 31.25 | -18.61 | 1 | NA | - | - |
| 57.6 | 52.8 | -8.33 | 5 | 9.615 | +0.16 | 25 | 55.930 | -2.90 | 3 | 62.5 | +8.51 | 0 | NA | - | - |
| 115.2 | 105.6 | -8.33 | 2 | 19.231 | +0.16 | 12 | 111.860 | -2.90 | 1 | NA | - | - | NA | - | - |
| 250 | NA | - | - | NA | - | - | 223.721 | -10.51 | 0 | NA | - | - | NA | - | - |
| 625 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1250 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |

**Note:** For the PIC16C73/73A/74/74A, the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information, or use the PIC16C76/77.

## 14.4 Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST), and Brown-out Reset (BOR)

| Applicable Devices | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

### 14.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the startup conditions.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*."

### 14.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

### 14.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

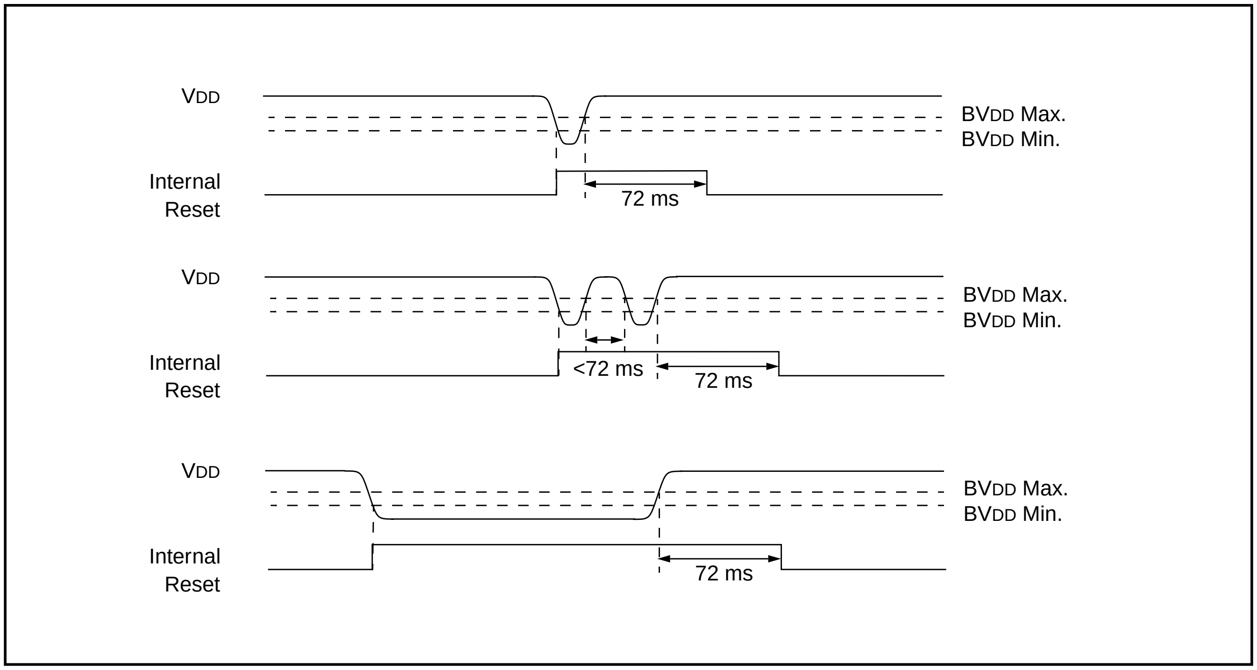
The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

### 14.4.4 BROWN-OUT RESET (BOR)

| Applicable Devices | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (3.8V - 4.2V range) for greater than parameter #35, the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 14-9 shows typical brown-out situations.

**FIGURE 14-9: BROWN-OUT SITUATIONS**



### 14.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 14-10, Figure 14-11, and Figure 14-12 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 14-11). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 14-7 shows the reset conditions for some special function registers, while Table 14-8 shows the reset conditions for all the registers.

### 14.4.6 POWER CONTROL/STATUS REGISTER (PCON)

| **Applicable Devices** | | | | | | |
|---|---|---|---|---|---|---|
| 72 | 73 | 73A | 74 | 74A | 76 | 77 |

The Power Control/Status Register, PCON has up to two bits, depending upon the device. Bit0 is not implemented on the PIC16C73 or PIC16C74.

Bit0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. Bit $\overline{\text{BOR}}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{\text{BOR}}$ cleared, indicating a BOR occurred. The $\overline{\text{BOR}}$ bit is a "Don’t Care" bit and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

**TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS, PIC16C73/74**

| **Oscillator Configuration** | **Power-up** | | **Wake-up from SLEEP** |
|---|---|---|---|
| | **PWRTE = 1** | **PWRTE = 0** | |
| XT, HS, LP | 72 ms + 1024TOSC | 1024TOSC | 1024 TOSC |
| RC | 72 ms | — | — |

**TABLE 14-4: TIME-OUT IN VARIOUS SITUATIONS, PIC16C72/73A/74A/76/77**

| **Oscillator Configuration** | **Power-up** | | **Brown-out** | **Wake-up from SLEEP** |
|---|---|---|---|---|
| | **$\overline{\text{PWRTE}}$ = 0** | **$\overline{\text{PWRTE}}$ = 1** | | |
| XT, HS, LP | 72 ms + 1024TOSC | 1024TOSC | 72 ms + 1024TOSC | 1024TOSC |
| RC | 72 ms | — | 72 ms | — |

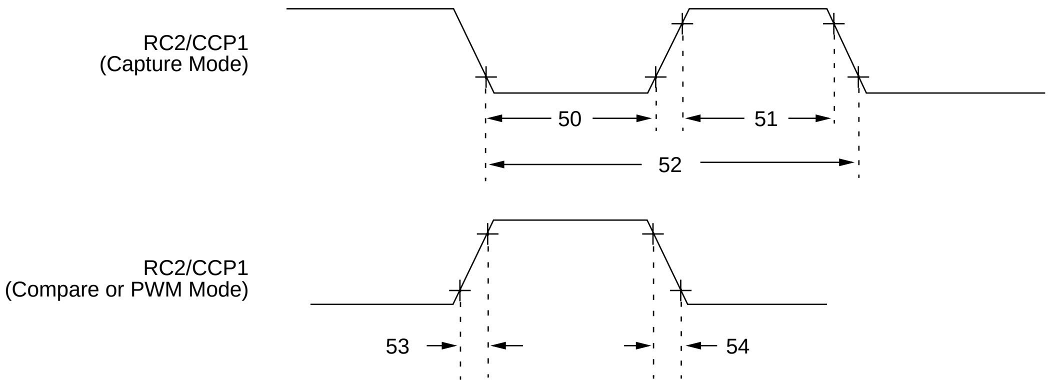
**TABLE 14-5: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C73/74**

| **$\overline{\text{POR}}$** | **$\overline{\text{TO}}$** | **$\overline{\text{PD}}$** | |
|---|---|---|---|
| 0 | 1 | 1 | Power-on Reset |
| 0 | 0 | x | Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$ |
| 0 | x | 0 | Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$ |
| 1 | 0 | 1 | WDT Reset |
| 1 | 0 | 0 | WDT Wake-up |
| 1 | u | u | $\overline{\text{MCLR}}$ Reset during normal operation |
| 1 | 1 | 0 | $\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP |

Legend: u = unchanged, x = unknown

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 17-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 17-1 for load conditions.

### TABLE 17-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

| Param No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 input low time | No Prescaler | | 0.5$T_{CY}$ + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**72 | 10 | — | — | ns | |
| | | | | PIC16**LC**72 | 20 | — | — | ns | |
| 51* | TccH | CCP1 input high time | No Prescaler | | 0.5$T_{CY}$ + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**72 | 10 | — | — | ns | |
| | | | | PIC16**LC**72 | 20 | — | — | ns | |
| 52* | TccP | CCP1 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4 or 16) |
| 53* | TccR | CCP1 output rise time | | PIC16**C**72 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**72 | — | 25 | 45 | ns | |
| 54* | TccF | CCP1 output fall time | | PIC16**C**72 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**72 | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### TABLE 17-10: A/D CONVERTER CHARACTERISTICS: PIC16C72-04 (Commercial, Industrial, Extended) PIC16C72-10 (Commercial, Industrial, Extended) PIC16C72-20 (Commercial, Industrial, Extended) PIC16LC72-04 (Commercial, Industrial)

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | — | — | 8-bits | bit | VREF = VDD = 5.12V,<br>VSS ≤ VAIN ≤ VREF |
| A02 | EABS | Total Absolute error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V,<br>VSS ≤ VAIN ≤ VREF |
| A03 | EIL | Integral linearity error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V,<br>VSS ≤ VAIN ≤ VREF |
| A04 | EDL | Differential linearity error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V,<br>VSS ≤ VAIN ≤ VREF |
| A05 | EFS | Full scale error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V,<br>VSS ≤ VAIN ≤ VREF |
| A06 | EOFF | Offset error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V,<br>VSS ≤ VAIN ≤ VREF |
| A10 | — | Monotonicity | — | guaranteed | — | — | VSS ≤ VAIN ≤ VREF |
| A20 | VREF | Reference voltage | 3.0V | — | VDD + 0.3 | V | |
| A25 | VAIN | Analog input voltage | VSS - 0.3 | — | VREF + 0.3 | V | |
| A30 | ZAIN | Recommended impedance of analog voltage source | — | — | 10.0 | kΩ | |
| A40 | IAD | A/D conversion current (VDD) PIC16**C**72 | — | 180 | — | µA | Average current consumption when A/D is on. (Note 1) |
| | | PIC16**LC**72 | — | 90 | — | µA | |
| A50 | IREF | VREF input current (Note 2) | 10 | — | 1000 | µA | During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 13.1. |
| | | | — | — | 10 | µA | During A/D Conversion cycle |

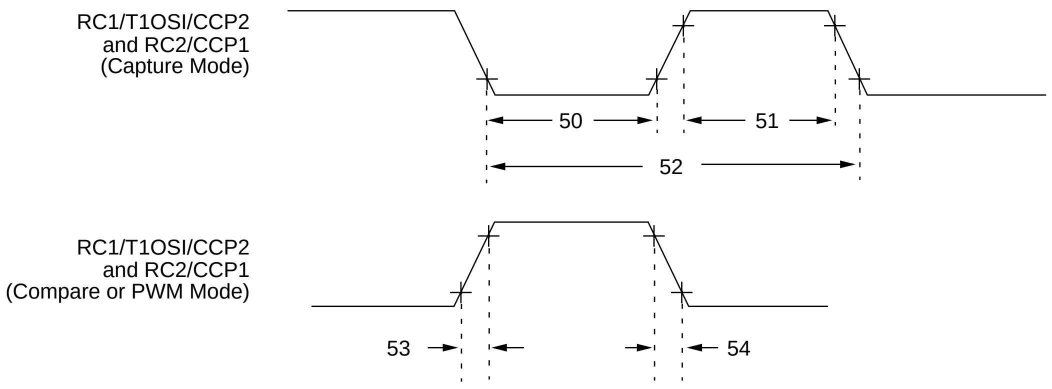
* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

### FIGURE 18-6: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 18-1 for load conditions.

### TABLE 18-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

| Parameter No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 and CCP2 input low time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**73/74 | 10 | — | — | ns | |
| | | | | PIC16**LC**73/74 | 20 | — | — | ns | |
| 51* | TccH | CCP1 and CCP2 input high time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**73/74 | 10 | — | — | ns | |
| | | | | PIC16**LC**73/74 | 20 | — | — | ns | |
| 52* | TccP | CCP1 and CCP2 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4 or 16) |
| 53* | TccR | CCP1 and CCP2 output fall time | | PIC16**C**73/74 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**73/74 | — | 25 | 45 | ns | |
| 54* | TccF | CCP1 and CCP2 output fall time | | PIC16**C**73/74 | — | 10 | 25 | ns | |
| | | | | PIC16**LC**73/74 | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

## 19.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I$^2$C specifications only)
4. Ts (I$^2$C specifications only)

| **T** | | | |
|---|---|---|---|
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

| **pp** | | | |
|---|---|---|---|
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | $\overline{RD}$ |
| cs | $\overline{CS}$ | rw | $\overline{RD}$ or $\overline{WR}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{SS}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O port | t1 | T1CKI |
| mc | $\overline{MCLR}$ | wr | $\overline{WR}$ |

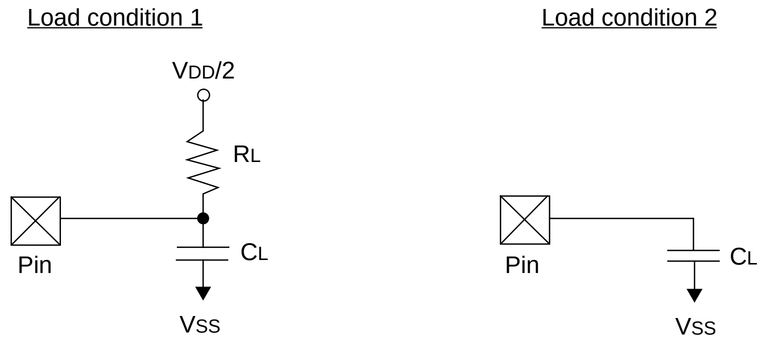
Uppercase letters and their meanings:

| **S** | | | |
|---|---|---|---|
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (Hi-impedance) | V | Valid |
| L | Low | Z | Hi-impedance |
| **I$^2$C only** | | | |
| AA | output access | High | High |
| BUF | Bus free | Low | Low |

TCC:ST (I$^2$C specifications only)

| **CC** | | | |
|---|---|---|---|
| HD | Hold | SU | Setup |
| **ST** | | | |
| DAT | DATA input hold | STO | STOP condition |
| STA | START condition | | |

**FIGURE 19-1: LOAD CONDITIONS**



RL = 464Ω

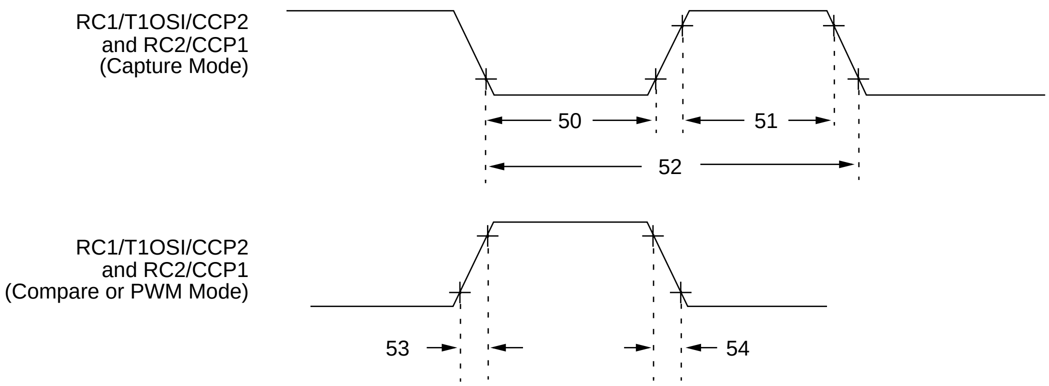
CL = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports

15 pF for OSC2 output

Note: PORTD and PORTE are not implemented on the PIC16C73A.

| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

### FIGURE 19-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 19-1 for load conditions.

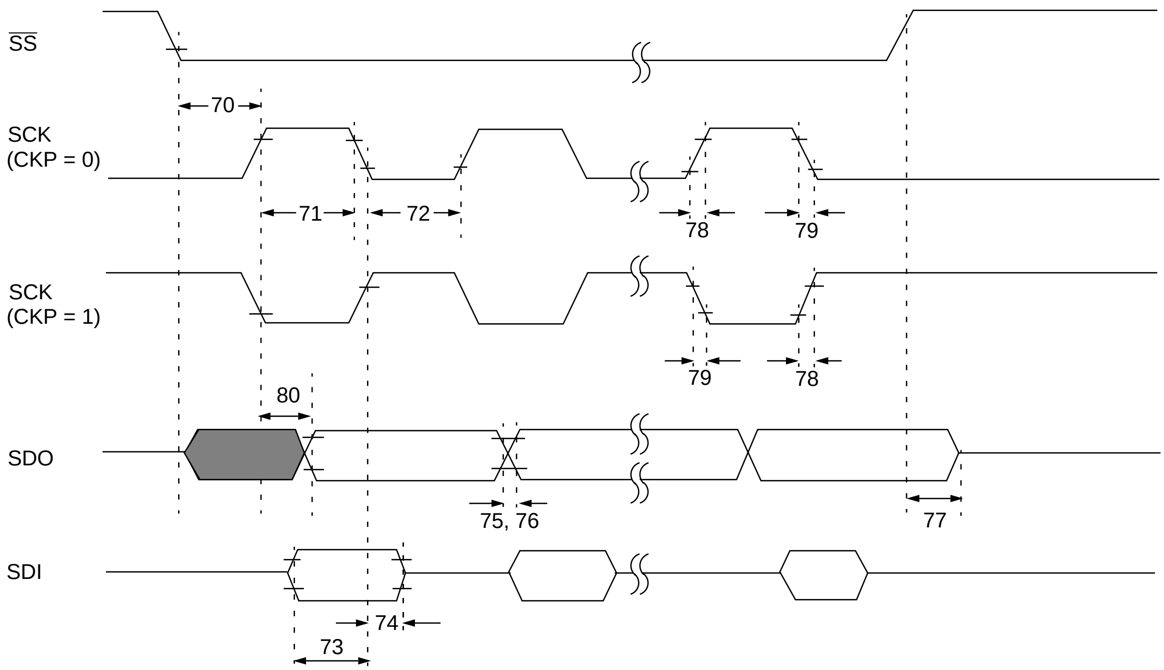
### TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

| Param No. | Sym | Characteristic | | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| 50* | TccL | CCP1 and CCP2 input low time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**73A/74A | 10 | — | — | ns | |
| | | | | PIC16**LC**73A/74A | 20 | — | — | ns | |
| 51* | TccH | CCP1 and CCP2 input high time | No Prescaler | | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | PIC16**C**73A/74A | 10 | — | — | ns | |
| | | | | PIC16**LC**73A/74A | 20 | — | — | ns | |
| 52* | TccP | CCP1 and CCP2 input period | | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4 or 16) |
| 53* | TccR | CCP1 and CCP2 output rise time | | PIC16**C**73A/74A | — | 10 | 25 | ns | |
| | | | | PIC16**LC**73A/74A | — | 25 | 45 | ns | |
| 54* | TccF | CCP1 and CCP2 output fall time | | PIC16**C**73A/74A | — | 10 | 25 | ns | |
| | | | | PIC16**LC**73A/74A | — | 25 | 45 | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated.
These parameters are for design guidance only and are not tested.

### FIGURE 19-9: SPI MODE TIMING



Note: Refer to Figure 19-1 for load conditions

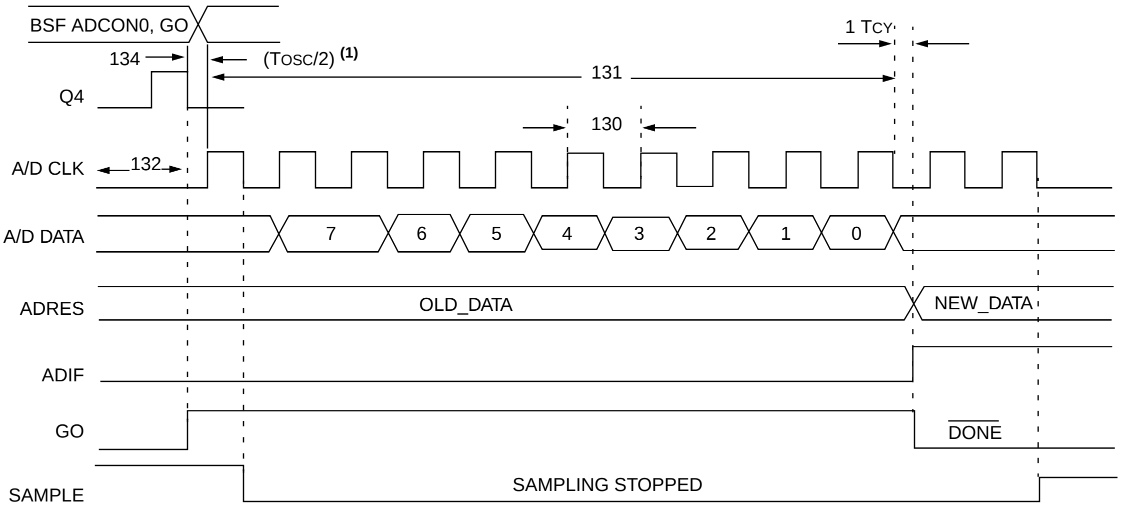
### TABLE 19-8: SPI MODE REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70 | TssL2scH,<br>TssL2scL | $\overline{SS}$↓ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71 | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72 | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73 | TdiV2scH,<br>TdiV2scL | Setup time of SDI data input to SCK edge | 100 | — | — | ns | |
| 74 | TscH2diL,<br>TscL2diL | Hold time of SDI data input to SCK edge | 100 | — | — | ns | |
| 75 | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76 | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77 | TssH2doZ | $\overline{SS}$↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78 | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79 | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80 | TscH2doV,<br>TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |

### FIGURE 19-14: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

## TABLE 19-14: A/D CONVERSION REQUIREMENTS

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 130 | TAD | A/D clock period | PIC16**C**73A/74A | 1.6 | — | — | µs | TOSC based, VREF ≥ 3.0V |
| | | | PIC16**LC**73A/74A | 2.0 | — | — | µs | TOSC based, VREF full range |
| | | | PIC16**C**73A/74A | 2.0 | 4.0 | 6.0 | µs | A/D RC Mode |
| | | | PIC16**LC**73A/74A | 3.0 | 6.0 | 9.0 | µs | A/D RC Mode |
| 131 | TCNV | Conversion time (not including S/H time) (Note 1) | | — | 9.5 | — | TAD | |
| 132 | TACQ | Acquisition time | | Note 2 | 20 | — | µs | |
| | | | | 5* | — | — | µs | The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD). |
| 134 | TGO | Q4 to A/D clock start | | — | TOSC/2 § | — | — | If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed. |
| 135 | TSWC | Switching from convert → sample time | | 1.5 § | — | — | TAD | |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

## 20.0 ELECTRICAL CHARACTERISTICS FOR PIC16C76/77

**Absolute Maximum Ratings †**

| | |
|---|---|
| Ambient temperature under bias | -55 to +125˚C |
| Storage temperature | -65˚C to +150˚C |
| Voltage on any pin with respect to $V_{SS}$ (except $V_{DD}$, $\overline{MCLR}$. and RA4) | -0.3V to ($V_{DD}$ + 0.3V) |
| Voltage on $V_{DD}$ with respect to $V_{SS}$ | -0.3 to +7.5V |
| Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ (Note 2) | 0 to +14V |
| Voltage on RA4 with respect to Vss | 0 to +14V |
| Total power dissipation (Note 1) | 1.0W |
| Maximum current out of $V_{SS}$ pin | 300 mA |
| Maximum current into $V_{DD}$ pin | 250 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{DD}$) | ±20 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) | ±20 mA |
| Maximum output current sunk by any I/O pin | 25 mA |
| Maximum output current sourced by any I/O pin | 25 mA |
| Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3) | 200 mA |
| Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3) | 200 mA |
| Maximum current sunk by PORTC and PORTD (combined) (Note 3) | 200 mA |
| Maximum current sourced by PORTC and PORTD (combined) (Note 3) | 200 mA |

**Note 1:** Power dissipation is calculated as follows: Pdis = $V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{Ol} \times I_{OL})$

**Note 2:** Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to $V_{SS}$.

**Note 3:** PORTD and PORTE are not implemented on the PIC16C76.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Applicable Devices** | 72 | 73 | 73A | 74 | 74A | 76 | 77 |

### TABLE 20-8: SPI MODE REQUIREMENTS

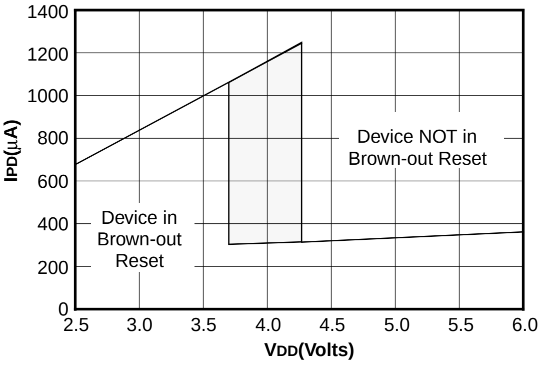
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70* | TssL2scH,<br>TssL2scL | $\overline{\text{SS}}$↓ to SCK↓ or SCK↑ input | TCY | — | — | ns | |
| 71* | TscH | SCK input high time (slave mode) | TCY + 20 | — | — | ns | |
| 72* | TscL | SCK input low time (slave mode) | TCY + 20 | — | — | ns | |
| 73* | TdiV2scH,<br>TdiV2scL | Setup time of SDI data input to SCK edge | 100 | — | — | ns | |
| 74* | TscH2diL,<br>TscL2diL | Hold time of SDI data input to SCK edge | 100 | — | — | ns | |
| 75* | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76* | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77* | TssH2doZ | $\overline{\text{SS}}$↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78* | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79* | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80* | TscH2doV,<br>TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |
| 81* | TdoV2scH,<br>TdoV2scL | SDO data output setup to SCK edge | TCY | — | — | ns | |
| 82* | TssL2doV | SDO data output valid after $\overline{\text{SS}}$↓ edge | — | — | 50 | ns | |
| 83* | TscH2ssH,<br>TscL2ssH | $\overline{\text{SS}}$ ↑ after SCK edge | 1.5TCY + 40 | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

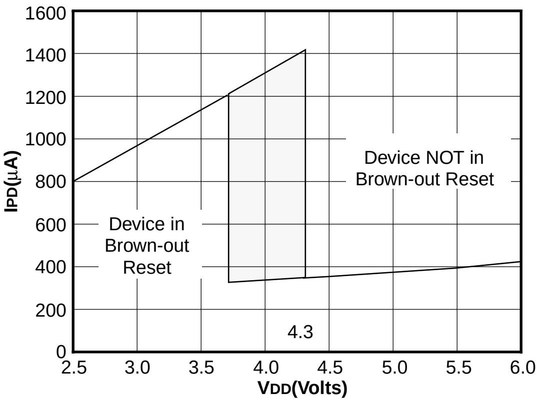
| Applicable Devices | 72 | 73 | 73A | 74 | 74A | 76 | 77 |
|---|---|---|---|---|---|---|---|

**FIGURE 21-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)**



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

**FIGURE 21-9: MAXIMUM IPD vs. VDD BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)**



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

**FIGURE 21-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)**

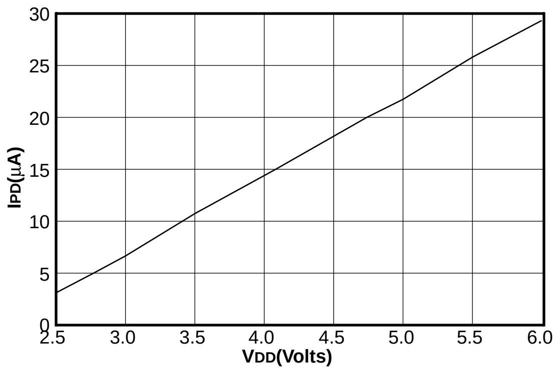
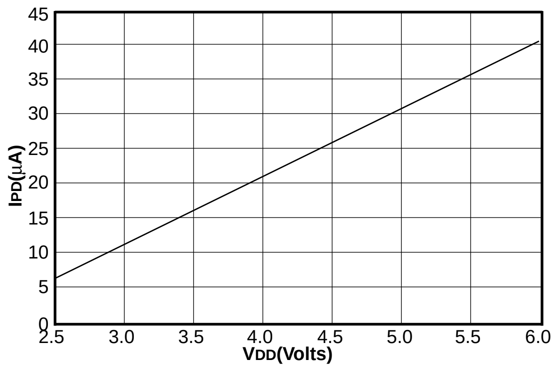
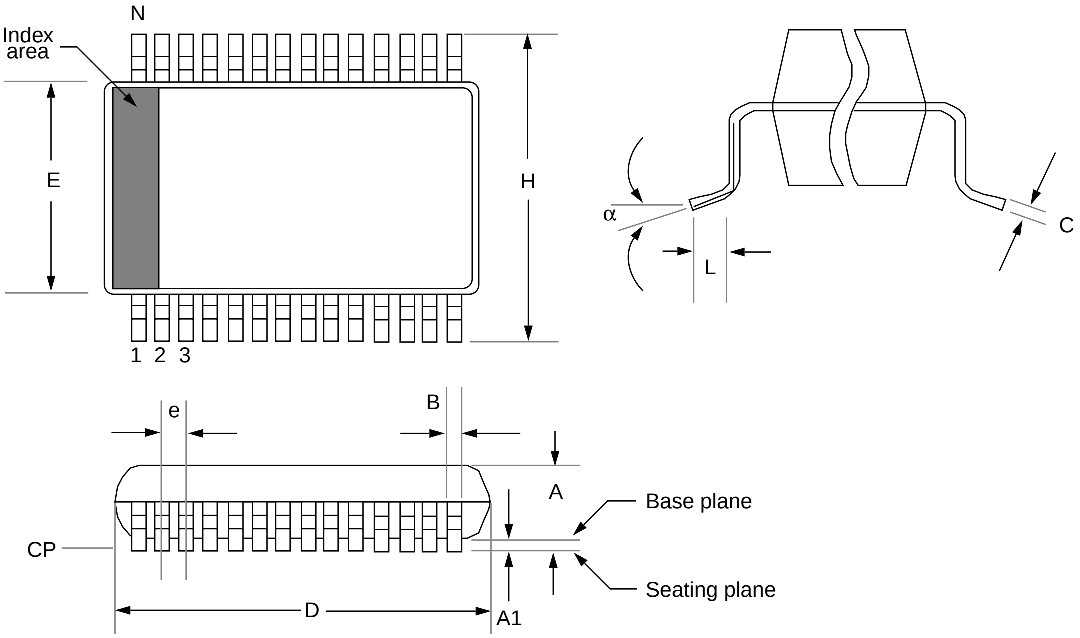


**FIGURE 21-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)**



Data based on matrix samples. See first page of this section for details.

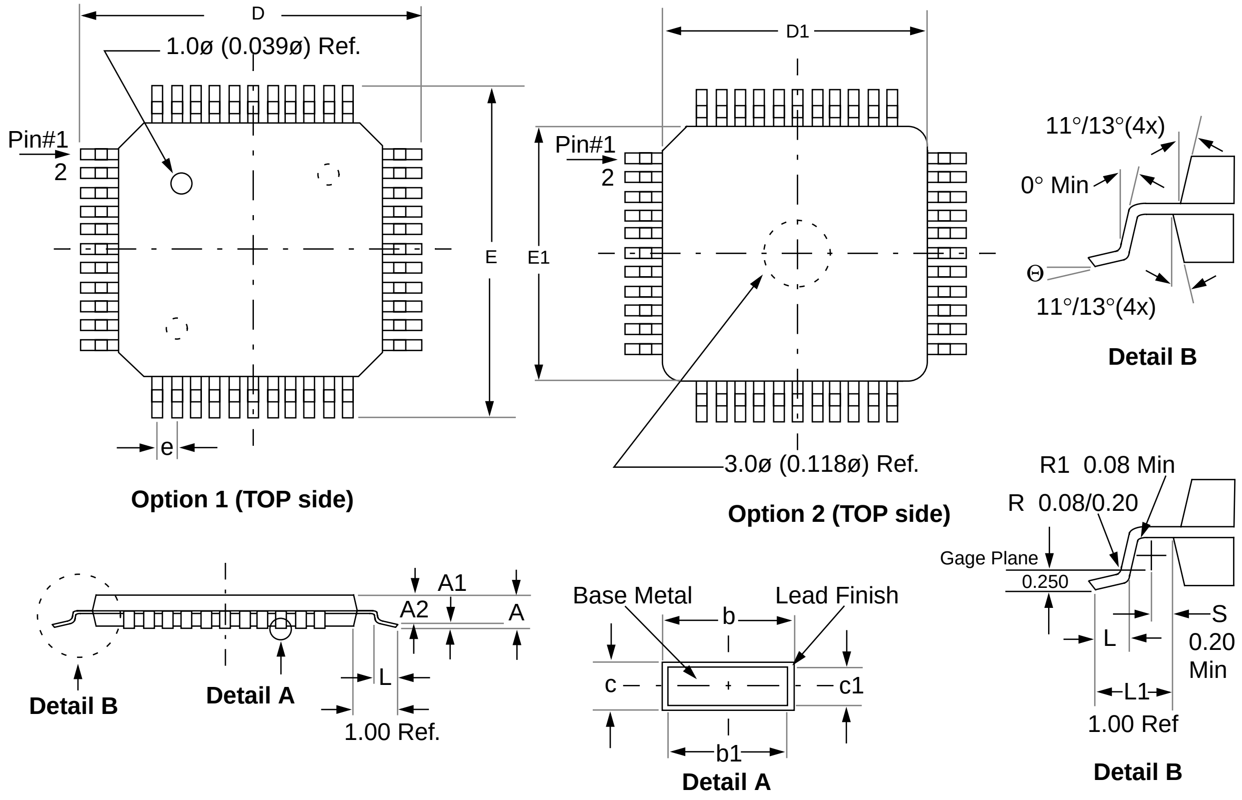
## 22.6 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)



**Package Group: Plastic SSOP**

| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | **Min** | **Max** | **Notes** | **Min** | **Max** | **Notes** |
| α | 0° | 8° | | 0° | 8° | |
| A | 1.730 | 1.990 | | 0.068 | 0.078 | |
| A1 | 0.050 | 0.210 | | 0.002 | 0.008 | |
| B | 0.250 | 0.380 | | 0.010 | 0.015 | |
| C | 0.130 | 0.220 | | 0.005 | 0.009 | |
| D | 10.070 | 10.330 | | 0.396 | 0.407 | |
| E | 5.200 | 5.380 | | 0.205 | 0.212 | |
| e | 0.650 | 0.650 | **Reference** | 0.026 | 0.026 | **Reference** |
| H | 7.650 | 7.900 | | 0.301 | 0.311 | |
| L | 0.550 | 0.950 | | 0.022 | 0.037 | |
| N | 28 | 28 | | 28 | 28 | |
| CP | - | 0.102 | | - | 0.004 | |

## 22.9 44-Lead Plastic Surface Mount (TQFP 10x10 mm Body 1.0/0.10 mm Lead Form) (TQ)



| Package Group: Plastic TQFP | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| A | 1.00 | 1.20 | | 0.039 | 0.047 | |
| A1 | 0.05 | 0.15 | | 0.002 | 0.006 | |
| A2 | 0.95 | 1.05 | | 0.037 | 0.041 | |
| D | 11.75 | 12.25 | | 0.463 | 0.482 | |
| D1 | 9.90 | 10.10 | | 0.390 | 0.398 | |
| E | 11.75 | 12.25 | | 0.463 | 0.482 | |
| E1 | 9.90 | 10.10 | | 0.390 | 0.398 | |
| L | 0.45 | 0.75 | | 0.018 | 0.030 | |
| e | 0.80 BSC | | | 0.031 BSC | | |
| b | 0.30 | 0.45 | | 0.012 | 0.018 | |
| b1 | 0.30 | 0.40 | | 0.012 | 0.016 | |
| c | 0.09 | 0.20 | | 0.004 | 0.008 | |
| c1 | 0.09 | 0.16 | | 0.004 | 0.006 | |
| N | 44 | 44 | | 44 | 44 | |
| Θ | 0° | 7° | | 0° | 7° | |

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010”) per side. D1 and E1 dimensions including mold mismatch.

2: Dimension “b” does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003”)max.

3: This outline conforms to JEDEC MS-026.