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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	$4V \sim 6V$
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c74a-20i-pq

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Pin Name	DIP Pin#	SSOP Pin#	SOIC Pin#	l/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	9	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	10	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/Vpp	1	1	1	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	2	2	I/O	TTL	RA0 can also be analog input0
RA1/AN1	3	3	3	I/O	TTL	RA1 can also be analog input1
RA2/AN2	4	4	4	I/O	TTL	RA2 can also be analog input2
RA3/AN3/VREF	5	5	5	I/O	TTL	RA3 can also be analog input3 or analog reference voltage
RA4/T0CKI	6	6	6	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
RA5/SS/AN4	7	7	7	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	21	I/O	TTL/ST ⁽¹⁾	RB0 can also be the external interrupt pin.
RB1	22	22	22	I/O	TTL	
RB2	23	23	23	I/O	TTL	
RB3	24	24	24	I/O	TTL	
RB4	25	25	25	I/O	TTL	Interrupt on change pin.
RB5	26	26	26	I/O	TTL	Interrupt on change pin.
RB6	27	27	27	I/O	TTL/ST ⁽²⁾	Interrupt on change pin. Serial programming clock.
RB7	28	28	28	I/O	TTL/ST ⁽²⁾	Interrupt on change pin. Serial programming data.
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11	11	I/O	ST	RC0 can also be the Timer1 oscillator output or Timer1 clock input.
RC1/T1OSI	12	12	12	I/O	ST	RC1 can also be the Timer1 oscillator input.
RC2/CCP1	13	13	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	14	14	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	15	15	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	16	16	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6	17	17	17	I/O	ST	
RC7	18	18	18	I/O	ST	
Vss	8, 19	8, 19	8, 19	Р		Ground reference for logic and I/O pins.
Vdd	20	20	20	Р		Positive supply for logic and I/O pins.
Legend: I = input	0 =	output	1	I/O = i	nput/output	P = power
	— =	Not used	1	TTI =	TTI input	ST = Schmitt Trigger input

TABLE 3-1:	PIC16C72	PINOUT	DESCRIPTION
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Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt. 2: This buffer is a Schmitt Trigger input when used in serial programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

PIC16C7X

NOTES:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 0)										
00h ⁽⁴⁾	INDF	Addressing	this location	egister)	0000 0000	0000 0000					
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽⁴⁾	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
03h ⁽⁴⁾	STATUS	IRP ⁽⁷⁾	RP1 ⁽⁷⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽⁴⁾	FSR	Indirect data	a memory ac	dress pointe	er	•				XXXX XXXX	uuuu uuuu
05h	PORTA	_	—	PORTA Dat	a Latch when	written: POR	TA pins wher	n read		0x 0000	0u 0000
06h	PORTB	PORTB Dat	ta Latch whe	n written: PC	ORTB pins whe	n read				XXXX XXXX	uuuu uuuu
07h	PORTC	PORTC Dat	ta Latch whe	n written: PC	ORTC pins whe	en read				XXXX XXXX	uuuu uuuu
08h ⁽⁵⁾	PORTD	PORTD Dat	ta Latch whe	n written: PC	ORTD pins whe	en read				XXXX XXXX	uuuu uuuu
09h (5)	PORTE	—	_	_	_	_	RE2	RE1	RE0	xxx	uuu
0Ah ^(1,4)	PCLATH	—	—	—	Write Buffer fo	or the upper	5 bits of the I	Program Cou	inter	0 0000	0 0000
0Bh ⁽⁴⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽³⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	-	-	—	—	CCP2IF	0	0
0Eh	TMR1L	Holding reg	ister for the L	_east Signific	cant Byte of the	e 16-bit TMR	1 register			XXXX XXXX	uuuu uuuu
0Fh	TMR1H	Holding reg	ister for the I	Most Signific	ant Byte of the	16-bit TMR1	register			XXXX XXXX	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	is Serial Port	Receive Bu	ffer/Transmit R	egister				XXXX XXXX	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	Register1 (I	_SB)					XXXX XXXX	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	Register1 (I	MSB)					XXXX XXXX	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Data Register									0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Co	Capture/Compare/PWM Register2 (LSB)								uuuu uuuu
1Ch	CCPR2H	Capture/Co	mpare/PWM	Register2 (I	MSB)					XXXX XXXX	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
1Eh	ADRES	A/D Result	Register							XXXX XXXX	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	0000 00-0

 TABLE 4-2:
 PIC16C73/73A/74/74A SPECIAL FUNCTION REGISTER SUMMARY

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

4: These registers can be addressed from either bank.

5: PORTD and PORTE are not physically implemented on the PIC16C73/73A, read as '0'.

6: Brown-out Reset is not implemented on the PIC16C73 or the PIC16C74, read as '0'.

7: The IRP and RP1 bits are reserved on the PIC16C73/73A/74/74A, always maintain these bits clear.

4.2.2.6 PIE2 REGISTER Applicable Devices 72 73 73 74 74 76 77

This register contains the individual enable bit for the CCP2 peripheral interrupt.

FIGURE 4-14: PIE2 REGISTER (ADDRESS 8Dh)



4.3 PCL and PCLATH Applicable Devices 72/73/73A/74/74A/76/77

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The upper bits (PC<12:8>) are not readable, but are indirectly writable through the PCLATH register. On any reset, the upper bits of the PC will be cleared. Figure 4-17 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 4-17: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 STACK

The PIC16CXX family has an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.
- Note 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

4.4 Program Memory Paging Applicable Devices 72|73|73A|74|74A|76|77

PIC16C7X devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<4:3> bits are not required for the return instructions (which POPs the address from the stack).

Note: PIC16C7X devices with 4K or less of program memory ignore paging bit PCLATH<4>. The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

TABLE 5-9:PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/RD/AN5	bit0	ST/TTL ⁽¹⁾	Input/output port pin or read control input in parallel slave port mode or analog input: RD 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/WR/AN6	bit1	ST/TTL ⁽¹⁾	Input/output port pin or write control input in parallel slave port mode or analog input: WR 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected)
RE2/CS/AN7	bit2	ST/TTL ⁽¹⁾	Input/output port pin or chip select control input in parallel slave port mode or analog input: \overline{CS} 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE	—	_	—	—	_	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Da	PORTE Data Direction Bits			0000 -111
9Fh	ADCON1	_	_	_	—	—	PCFG2	PCFG1	PCFG0	000	000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTE.

NOTES:

7.0 TIMER0 MODULE Applicable Devices 727373A7474A7677

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit TOCS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0

FIGURE 7-1: TIMER0 BLOCK DIAGRAM

Source Edge Select bit TOSE (OPTION<4>). Clearing bit TOSE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 <u>Timer0 Interrupt</u>

Applicable Devices

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for Timer0 interrupt timing.







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FIGURE 11-8: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)(PIC16C76/77)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	R = Readable bit		
bit7		W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset								
bit 7:	<pre>WCOL: Write Collision Detect bit 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software) 0 = No collision</pre>									
bit 6:	SSPOV: R	eceive Ove	erflow Indi	cator bit						
	In SPI mode 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master mode the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register. 0 = No overflow									
	In I^2C mode 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode. 0 = No overflow									
bit 5:	SSPEN: S	ynchronou	s Serial P	ort Enable	bit					
	In SPI mode 1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins 0 = Disables serial port and configures these pins as I/O port pins							pins		
	In I^2 <u>C mode</u> 1 = Enables the serial port and configures the SDA and SCL pins as serial port pins 0 = Disables serial port and configures these pins as I/O port pins In both modes, when enabled, these pins must be properly configured as input or output									
bit 4:	CKP : Clock Polarity Select bit In SPI mode 1 = Idle state for clock is a high level 0 = Idle state for clock is a low level In I^2C mode SCK release control 1 = Enable clock 0 = Holds clock low (clock stretch) (Used to ensure data setup time)									
bit 3-0:	$\begin{array}{l} \textbf{SSPM3:S3} \\ 0000 = SF \\ 0001 = SF \\ 0010 = SF \\ 0100 = SF \\ 0100 = SF \\ 0101 = SF \\ 0110 = I^2 \\ 0111 = I^2 \\ 1011 = I^2 \\ 1110 = I^2 \\ 1111 = I^2 \\ \end{array}$	SPM0: Syn PI master n PI master n PI master n PI master n PI slave mc CI slave mc CI slave mo CI slave mo CI slave mo CI slave mo CI slave mo CI slave mo	chronous node, cloc node, cloc node, cloc ode, clock ode, clock de, 7-bit a de, 10-bit controlled de, 7-bit a de, 10-bit	Serial Por k = Fosc/ ² k = Fosc/ ² k = Fosc/ ⁶ k = TMR2 = SCK pin = SCK pin ddress address t master m ddress wit address w	t Mode Se 4 16 64 0. <u>SS</u> pin c 1. <u>SS</u> pin c 1. <u>SS</u> pin c 1. th start an vith start a	elect bits ontrol enat ontrol disa e idle) d stop bit i nd stop bit	bled. bled. SS ca nterrupts er interrupts e	n be used as I/O pin nabled enabled		

TABLE 14-6:	STATUS BITS AND THEIR	SIGNIFICANCE,	PIC16C72/73A/74A/76/77
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POR	BOR	TO	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on POR
0	x	x	0	Illegal, PD is set on POR
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 14-7: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register PIC16C73/74	PCON Register PIC16C72/73A/74A/76/77
Power-on Reset	000h	0001 1xxx	0-	0x
MCLR Reset during normal operation	000h	000u uuuu	u-	uu
MCLR Reset during SLEEP	000h	0001 Ouuu	u-	uu
WDT Reset	000h	0000 luuu	u-	uu
WDT Wake-up	PC + 1	uuu0 Ouuu	u-	uu
Brown-out Reset	000h	0001 luuu	N/A	u0
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuul Ouuu	u-	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 14-8:	INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices				es		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt	
W	72	73	73A	74	74A	76	77	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	72	73	73A	74	74A	76	77	N/A	N/A	N/A
TMR0	72	73	73A	74	74A	76	77	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	72	73	73A	74	74A	76	77	0000h	0000h	PC + 1 (2)
STATUS	72	73	73A	74	74A	76	77	0001 1xxx	000q quuu (3)	uuuq quuu (3)
FSR	72	73	73A	74	74A	76	77	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	72	73	73A	74	74A	76	77	0x 0000	0u 0000	uu uuuu
PORTB	72	73	73A	74	74A	76	77	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	72	73	73A	74	74A	76	77	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	72	73	73A	74	74A	76	77	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	72	73	73A	74	74A	76	77	xxx	uuu	uuu
PCLATH	72	73	73A	74	74A	76	77	0 0000	0 0000	u uuuu

Legend: u = unchanged, x = unknown, -= unimplemented bit, read as '0', <math>q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 14-7 for reset value for specific condition.

15.0 INSTRUCTION SET SUMMARY

Each PIC16CXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 15-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 15-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 15-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with $x = 0$. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; $d = 0$: store result in W, d = 1: store result in file register f. Default is $d = 1$
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination either the W register or the specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
<>	Register bit field
∈	In the set of
italics	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Table 15-2 lists the instructions recognized by the MPASM assembler.

Figure 15-1 shows the general formats that the instructions can have.

Note: To maintain upward compatibility with future PIC16CXX products, <u>do not use</u> the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS



PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77





TABLE 17-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
50*	TccL	CCP1 input low time	No Prescaler		0.5Tcy + 20	_		ns	
			With Prescaler PIC16C72		10	—	—	ns	
				PIC16 LC 72	20	-	_	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5Tcy + 20			ns	
			With Prescaler	PIC16 C 72	10	-		ns	
				PIC16 LC 72	20	-		ns	
52*	TccP	CCP1 input period			<u>3Tcy + 40</u> N	_	_	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 output rise time		PIC16 C 72	—	10	25	ns	
				PIC16 LC 72	_	25	45	ns	
54*	TccF	CCP1 output fall time		PIC16 C 72	_	10	25	ns	
				PIC16 LC 72		25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 17-10: I²C BUS DATA TIMING



TABLE 17-9: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Мах	Units	Conditions
100	Тнідн	Clock high time	100 kHz mode	4.0	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
102	Tr	SDA and SCL rise	100 kHz mode	_	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	—	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup	100 kHz mode	4.7	—	μs	
		time	400 kHz mode	0.6	—	μs	
109	ΤΑΑ	Output valid from	100 kHz mode		3500	ns	Note 1
		CIOCK	400 kHz mode	_	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3		μs	start
	Cb	Bus capacitive loading		400	pF		

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz)S I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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TABLE 18-8: SPI MODE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input	Тсү		_	ns	
71	TscH	SCK input high time (slave mode)	Tcy + 20	_	_	ns	
72	TscL	SCK input low time (slave mode)	Tcy + 20	_	_	ns	
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	50	_	_	ns	
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	50	_	_	ns	
75	TdoR	SDO data output rise time		10	25	ns	
76	TdoF	SDO data output fall time	_	10	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance	10	_	50	ns	
78	TscR	SCK output rise time (master mode)	_	10	25	ns	
79	TscF	SCK output fall time (master mode)		10	25	ns	
80	TscH2doV, TscL2doV	H2doV, SDO data output valid after SCK L2doV edge		_	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 19-13: A/D CONVERTER CHARACTERISTICS:

PIC16C73A/74A-04 (Commercial, Industrial, Extended) PIC16C73A/74A-10 (Commercial, Industrial, Extended) PIC16C73A/74A-20 (Commercial, Industrial, Extended) PIC16LC73A/74A-04 (Commercial, Industrial)

Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions	
A01	Nr	Resolution			—	8-bits	bit	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A02	Eabs	Total Absolute error		_	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$
A03	EIL	Integral linearity error		_	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$
A04	Edl	Differential linearity error		—	—	<±1	LSb	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A05	Efs	Full scale error		—	—	<±1	LSb	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A06	Eoff	Offset error		_	_	<±1	LSb	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$
A10	_	Monotonicity			guaranteed	—	—	$VSS \leq VAIN \leq VREF$
A20	Vref	Reference voltage		3.0V	—	VDD + 0.3	V	
A25	VAIN	Analog input voltage		Vss - 0.3	—	Vref + 0.3	V	
A30	Zain	Recommended impedar analog voltage source	_	—	10.0	kΩ		
A40	IAD	A/D conversion current	PIC16 C 73A/74A	—	180	_	μA	Average current consump-
		(VDD)	PIC16 LC 73A/74A	_	90	— μΑ		tion when A/D is on. (Note 1)
A50	IREF	VREF input current (Note	10	—	1000	μΑ	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 13.1.	
					_	10	μΑ	cycle

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

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FIGURE 20-11: SPI SLAVE MODE TIMING (CKE = 0)

FIGURE 20-12: SPI SLAVE MODE TIMING (CKE = 1)



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FIGURE 20-15: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



TABLE 20-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16 C 76/77		_	80 100	ns	
121	Tckrf	Clock out rise time and fall time (Master Mode)	PIC16 C 76/77		_	45	ns	
122	Tdtrf	Data out rise time and fall time	PIC16 LC 76/77 PIC16 C 76/77		-	50 45	ns ns	
			PIC16 LC 76/77	—	-	50	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 20-16: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



TABLE 20-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK \downarrow (DT setup time)	15	_	_	ns	
126	TckL2dtl	Data hold after CK \downarrow (DT hold time)	15	—	—	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices72737374747677FIGURE 21-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)



FIGURE 21-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

APPENDIX C: WHAT'S NEW

Added the following devices:

- PIC16C76
- PIC16C77

Removed the PIC16C710, PIC16C71, PIC16C711 from this datasheet.

Added PIC16C76 and PIC16C77 devices. The PIC16C76/77 devices have 368 bytes of data memory distributed in 4 banks and 8K of program memory in 4 pages. These two devices have an enhanced SPI that supports both clock phase and polarity. The USART has been enhanced.

When upgrading to the PIC16C76/77 please note that the upper 16 bytes of data memory in banks 1,2, and 3 are mapped into bank 0. This may require relocation of data memory usage in the user application code.

Added Q-cycle definitions to the Instruction Set Summary section.

APPENDIX D: WHAT'S CHANGED

Minor changes, spelling and grammatical changes.

Added the following note to the USART section. This note applies to all devices except the PIC16C76 and PIC16C77.

For the PIC16C73/73A/74/74A the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information or use the PIC16C76/77.

Divided SPI section into SPI for the PIC16C76/77 and SPI for all other devices.

ON-LINE SUPPORT

Microchip provides two methods of on-line support. These are the Microchip BBS and the Microchip World Wide Web (WWW) site.

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When using the BBS via the Compuserve Network, in most cases, a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore you do not need CompuServe membership to join Microchip's BBS. There is no charge for connecting to the Microchip BBS. The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe service allow multiple users various baud rates depending on the local point of access.

The following connect procedure applies in most locations.

- 1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
- 2. Dial your local CompuServe access number.
- 3. Depress the **<Enter>** key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
- Type +, depress the <Enter> key and "Host Name:" will appear.
- 5. Type MCHIPBBS, depress the **<Enter>** key and you will be connected to the Microchip BBS.

In the United States, to find the CompuServe phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with "Host Name:", type NETWORK, depress the **<Enter>** key and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 723-1550 for your local CompuServe number.

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