



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c76-10i-so

PIC16C7X

NOTES:

PIC16C7X

TABLE 4-2: PIC16C73/73A/74/74A SPECIAL FUNCTION REGISTER SUMMARY (Cont'd)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 1											
80h ⁽⁴⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	RBP _U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽⁴⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h ⁽⁴⁾	STATUS	IRP ⁽⁷⁾	RP1 ⁽⁷⁾	RP0	T0	PD	Z	DC	C	0001 1xxx	000q quuu
84h ⁽⁴⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
88h ⁽⁵⁾	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h ⁽⁵⁾	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	0000 -111
8Ah ^(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
8Bh ⁽⁴⁾	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE ⁽³⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	---- --0
8Eh	PCON	—	—	—	—	—	—	POR	BOR ⁽⁶⁾	---- --qq	---- --uu
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
93h	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	0000 0000
94h	SSPSTAT	—	—	D/A	P	S	R/W	UA	BF	--00 0000	--00 0000
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

4: These registers can be addressed from either bank.

5: PORTD and PORTE are not physically implemented on the PIC16C73/73A, read as '0'.

6: Brown-out Reset is not implemented on the PIC16C73 or the PIC16C74, read as '0'.

7: The IRP and RP1 bits are reserved on the PIC16C73/73A/74/74A, always maintain these bits clear.

PIC16C7X

8.5 Resetting Timer1 using a CCP Trigger Output

Applicable Devices							
72	73	73A	74	74A	76	77	

The CCP2 module is not implemented on the PIC16C72 device.

If the CCP1 or CCP2 module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1.

Note: The special event triggers from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for Timer1.

8.6 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

Applicable Devices							
72	73	73A	74	74A	76	77	

TMR1H and TMR1L registers are not reset to 00h on a POR or any other reset except by the CCP1 and CCP2 special event triggers.

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other resets, the register is unaffected.

8.7 Timer1 Prescaler

Applicable Devices							
72	73	73A	74	74A	76	77	

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh,10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ^(1,2)	ADIF	RCIF ⁽²⁾	TXIF ⁽²⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE ^(1,2)	ADIE	RCIE ⁽²⁾	TXIE ⁽²⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNCR	TMR1CS	TMR1ON	- -00 0000	- -uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A/76, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port or a USART, these bits are unimplemented, read as '0'.

To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$ must have TRISA<5> set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. An example would be in master mode where you are only sending data (to a display driver), then both SDI and $\overline{SS}$ could be used as general purpose outputs by clearing their corresponding TRIS register bits.

Figure 11-10 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application firmware. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2) is to broadcast data by the firmware protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SCK output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a “line activity monitor” mode.

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

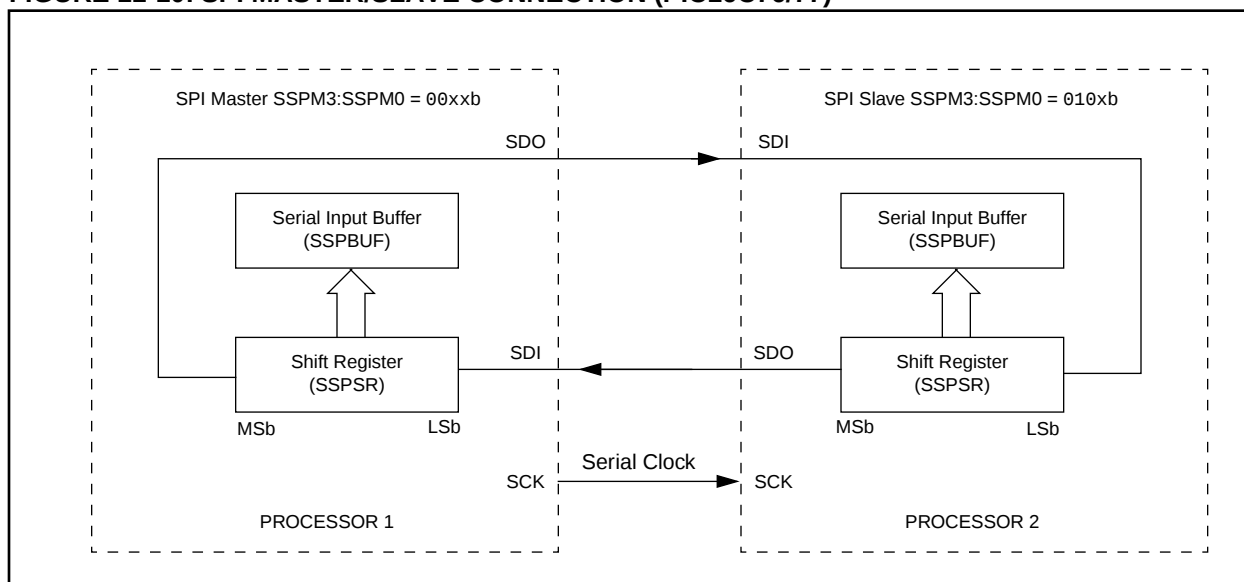
The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 11-11, Figure 11-12, and Figure 11-13 where the MSB is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- $F_{osc}/4$ (or T_{cy})
- $F_{osc}/16$ (or $4 \cdot T_{cy}$)
- $F_{osc}/64$ (or $16 \cdot T_{cy}$)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 5 MHz. When in slave mode the external clock must meet the minimum high and low times.

In sleep mode, the slave can transmit and receive data and wake the device from sleep.

FIGURE 11-10: SPI MASTER/SLAVE CONNECTION (PIC16C76/77)



12.1 USART Baud Rate Generator (BRG)

Applicable Devices							
72	73	73A	74	74A	76	77	

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz
Desired Baud Rate = 9600
BRGH = 0
SYNC = 0

EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

$$\begin{aligned}\text{Desired Baud rate} &= \text{Fosc} / (64 (X + 1)) \\ 9600 &= 16000000 / (64 (X + 1)) \\ X &= \lfloor 25.042 \rfloor = 25 \\ \text{Calculated Baud Rate} &= 16000000 / (64 (25 + 1)) \\ &= 9615 \\ \text{Error} &= \frac{(\text{Calculated Baud Rate} - \text{Desired Baud Rate})}{\text{Desired Baud Rate}} \\ &= (9615 - 9600) / 9600 \\ &= 0.16\%\end{aligned}$$

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the $\text{Fosc}/(16(X + 1))$ equation can reduce the baud rate error in some cases.

Note: For the PIC16C73/73A/74/74A, the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information, or use the PIC16C76/77.

Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = $\text{Fosc}/(64(X+1))$	Baud Rate = $\text{Fosc}/(16(X+1))$
1	(Synchronous) Baud Rate = $\text{Fosc}/(4(X+1))$	NA

X = value in SPBRG (0 to 255)

TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD RATE (K)	FOSC = 20 MHz			16 MHz			10 MHz			7.16 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64	9.520	-0.83	46
19.2	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32	19.454	+1.32	22
38.4	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15	37.286	-2.90	11
57.6	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10	55.930	-2.90	7
115.2	113.636	-1.36	10	111.111	-3.55	8	125	+8.51	4	111.860	-2.90	3
250	250	0	4	250	0	3	NA	-	-	NA	-	-
625	625	0	1	NA	-	-	625	0	0	NA	-	-
1250	1250	0	0	NA	-	-	NA	-	-	NA	-	-

BAUD RATE (K)	FOSC = 5.068 MHz			4 MHz			3.579 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.6	0	32	NA	-	-	9.727	+1.32	22	8.928	-6.99	6	NA	-	-
19.2	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11	20.833	+8.51	2	NA	-	-
38.4	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5	31.25	-18.61	1	NA	-	-
57.6	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3	62.5	+8.51	0	NA	-	-
115.2	105.6	-8.33	2	19.231	+0.16	12	111.860	-2.90	1	NA	-	-	NA	-	-
250	NA	-	-	NA	-	-	223.721	-10.51	0	NA	-	-	NA	-	-
625	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1250	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-

Note: For the PIC16C73/73A/74/74A, the asynchronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information, or use the PIC16C76/77.

FIGURE 14-13: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

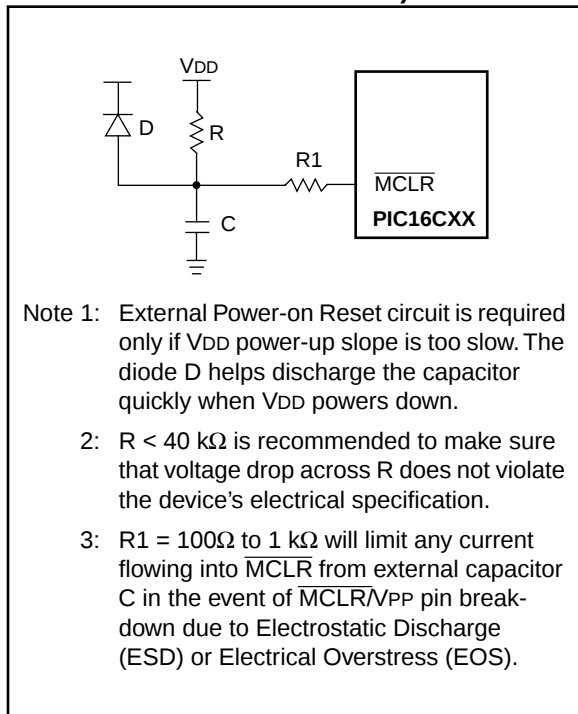


FIGURE 14-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

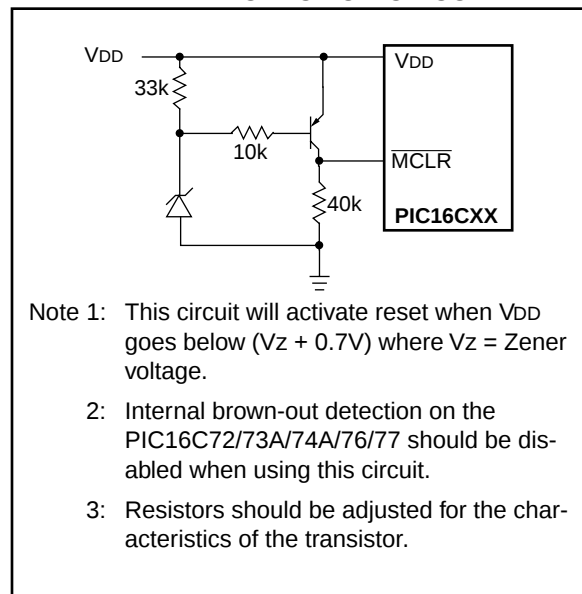
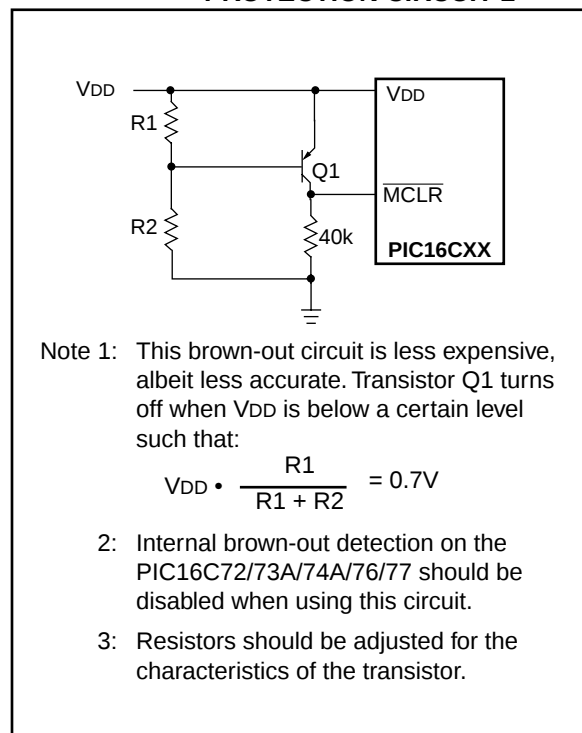


FIGURE 14-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



NOP		No Operation			
Syntax:	[<i>label</i>] NOP				
Operands:	None				
Operation:	No operation				
Status Affected:	None				
Encoding:	00	0000	0xx0	0000	
Description:	No operation.				
Words:	1				
Cycles:	1				
Q Cycle Activity:	Q1	Q2	Q3	Q4	
	Decode	No-Operation	No-Operation	No-Operation	
Example	NOP				

RETFIE		Return from Interrupt						
Syntax:	[<i>label</i>] RETFIE							
Operands:	None							
Operation:	TOS → PC, 1 → GIE							
Status Affected:	None							
Encoding:	<table><tr><td>00</td><td>0000</td><td>0000</td><td>1001</td></tr></table>				00	0000	0000	1001
00	0000	0000	1001					
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.							
Words:	1							
Cycles:	2							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
1st Cycle	Decode	No-Operation	Set the GIE bit	Pop from the Stack				
2nd Cycle	No-Operation	No-Operation	No-Operation	No-Operation				

Example

RETFIE

After Interrupt

PC = TOS

GIE = 1

OPTION	Load Option Register			
Syntax:	[<i>label</i>] OPTION			
Operands:	None			
Operation:	(W) → OPTION			
Status Affected:	None			
Encoding:	00	0000	0110	0010
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.			
Words:	1			
Cycles:	1			
Example				
To maintain upward compatibility with future PIC16CXX products, do not use this instruction.				

SUBWF Subtract W from f

Syntax: [label] SUBWF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{destination})$

Status Affected: C, DC, Z

Encoding:

00	0010	dfff	ffff
----	------	------	------

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to destination

Example 1: SUBWF REG1, 1

Before Instruction

REG1 = 3
W = 2
C = ?
Z = ?

After Instruction

REG1 = 1
W = 2
C = 1; result is positive
Z = 0

Example 2: Before Instruction

REG1 = 2
W = 2
C = ?
Z = ?

After Instruction

REG1 = 0
W = 2
C = 1; result is zero
Z = 1

Example 3: Before Instruction

REG1 = 1
W = 2
C = ?
Z = ?

After Instruction

REG1 = 0xFF
W = 2
C = 0; result is negative
Z = 0

SWAPF Swap Nibbles in f

Syntax: [label] SWAPF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (\text{destination}<7:4>)$,
 $(f<7:4>) \rightarrow (\text{destination}<3:0>)$

Status Affected: None

Encoding:

00	1110	dfff	ffff
----	------	------	------

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to destination

Example SWAPF REG, 0

Before Instruction

REG1 = 0xA5

After Instruction

REG1 = 0xA5
W = 0x5A

TRIS Load TRIS Register

Syntax: [label] TRIS f

Operands: $5 \leq f \leq 7$

Operation: $(W) \rightarrow \text{TRIS register } f$;

Status Affected: None

Encoding:

00	0000	0110	0fff
----	------	------	------

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77

FIGURE 17-3: CLKOUT AND I/O TIMING

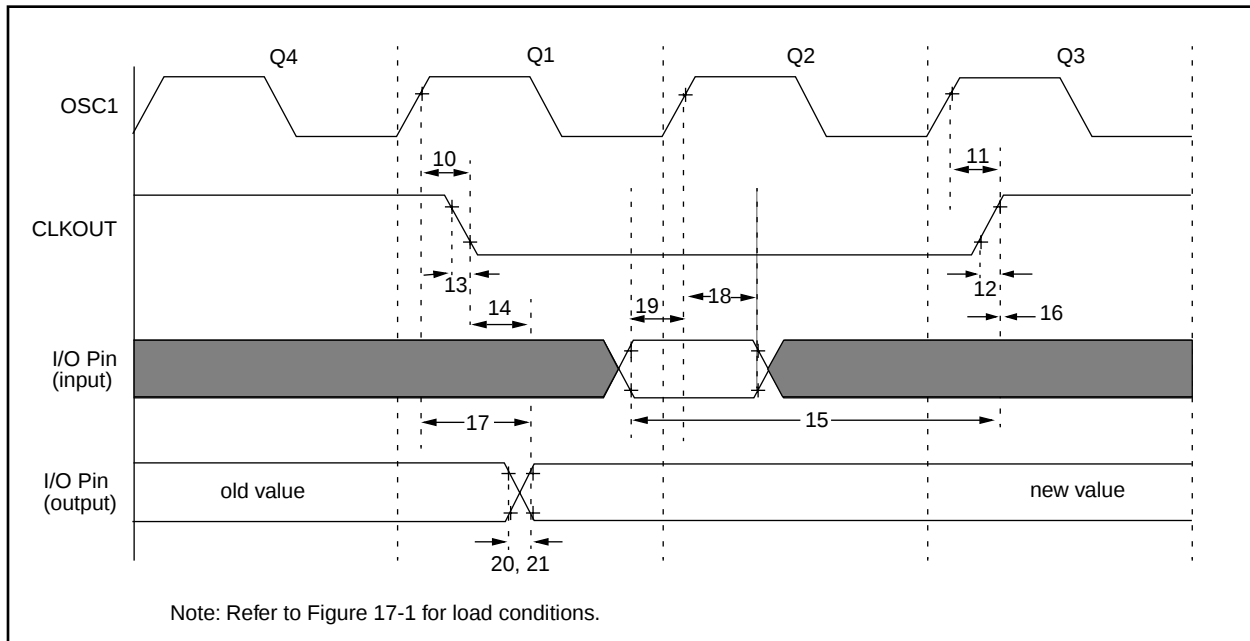


TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time	—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time	—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	Tosc + 200	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C72	100	—	ns	
			PIC16LC72	200	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	PIC16C72	—	10	ns	
			PIC16LC72	—	—	80	ns
21*	TioF	Port output fall time	PIC16C72	—	10	ns	
			PIC16LC72	—	—	80	ns
22††*	Tinp	INT pin high or low time	Tcy	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time	Tcy	—	—	ns	

* These parameters are characterized but not tested.

†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

20.1 DC Characteristics: **PIC16C76/77-04 (Commercial, Industrial, Extended)**
PIC16C76/77-10 (Commercial, Industrial, Extended)
PIC16C76/77-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial							
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	- -	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7 3.7	4.0 4.0	4.3 4.4	V V	BODEN bit in configuration word enabled Extended Range Only
D010 D013	Supply Current (Note 2,5)	IDD	- -	2.7 10	5 20	mA mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4) HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled VDD = 5.0V
D020 D021 D021A D021B	Power-down Current (Note 3,5)	IPD	- - - -	10.5 1.5 1.5 2.5	42 16 19 19	μA μA μA μA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

FIGURE 20-8: PARALLEL SLAVE PORT TIMING (PIC16C77)

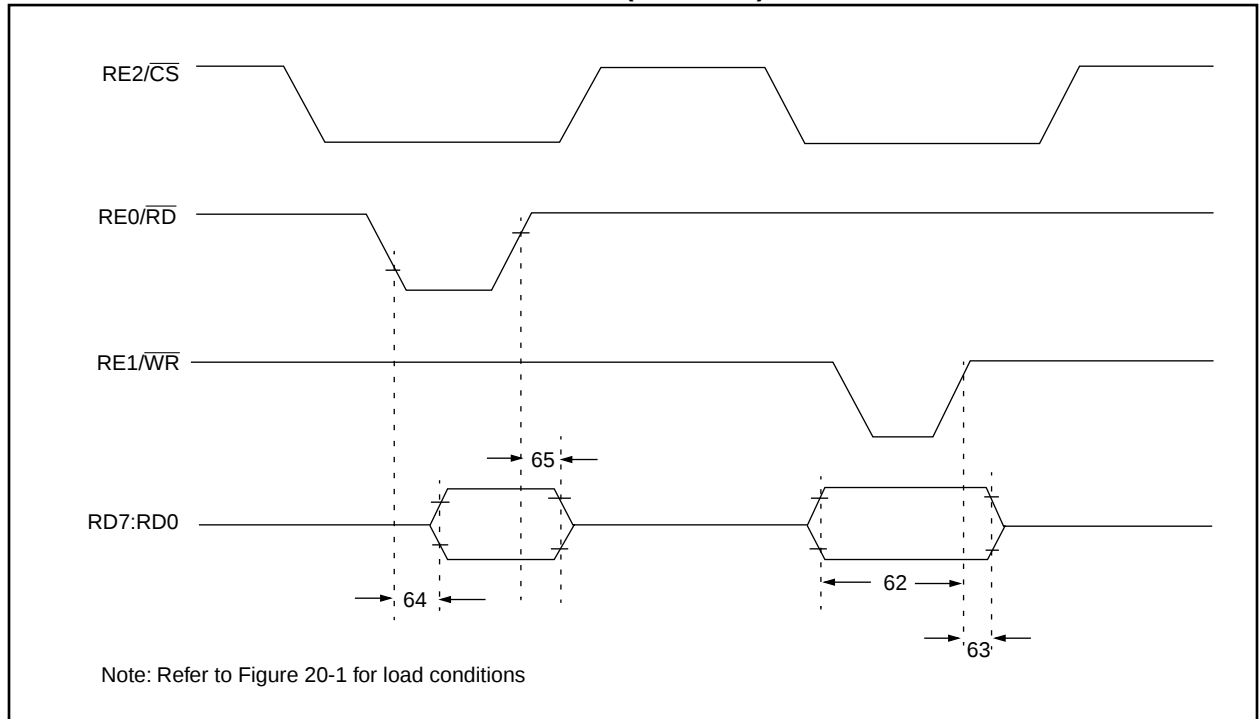


TABLE 20-7: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C77)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time)	20 25	— —	— —	ns ns	Extended Range Only
63*	TwrH2dtI	$\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data-in invalid (hold time)	PIC16C77 20	— —	— —	ns	
			PIC16LC77 35	—	—	ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data-out valid	— —	— —	80 90	ns ns	Extended Range Only
65	TrdH2dtI	$\overline{RD}\uparrow$ or $\overline{CS}\downarrow$ to data-out invalid	10	—	30	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

21.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified V_{DD} range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean +3 σ) and (mean -3 σ) respectively where σ is standard deviation.

FIGURE 21-1: TYPICAL I_{PD} vs. V_{DD} (WDT DISABLED, RC MODE)

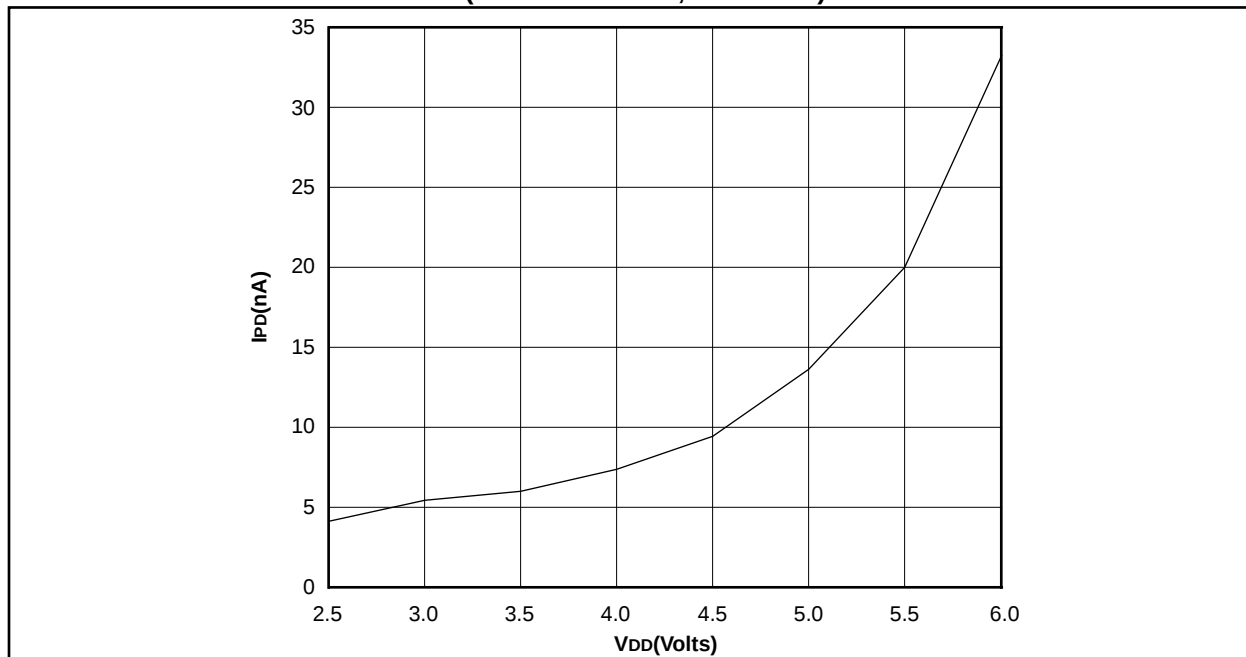
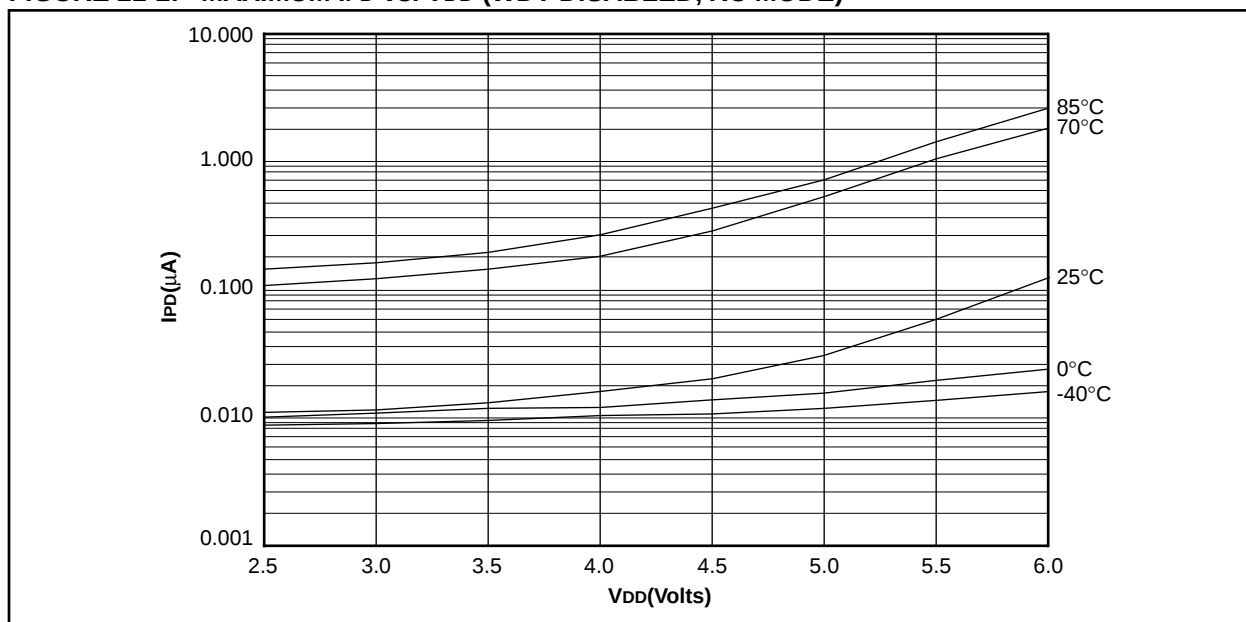


FIGURE 21-2: MAXIMUM I_{PD} vs. V_{DD} (WDT DISABLED, RC MODE)



Applicable Devices	72	73	73A	74	74A	76	77
--------------------	----	----	-----	----	-----	----	----

FIGURE 21-14: TYPICAL I_{DD} vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

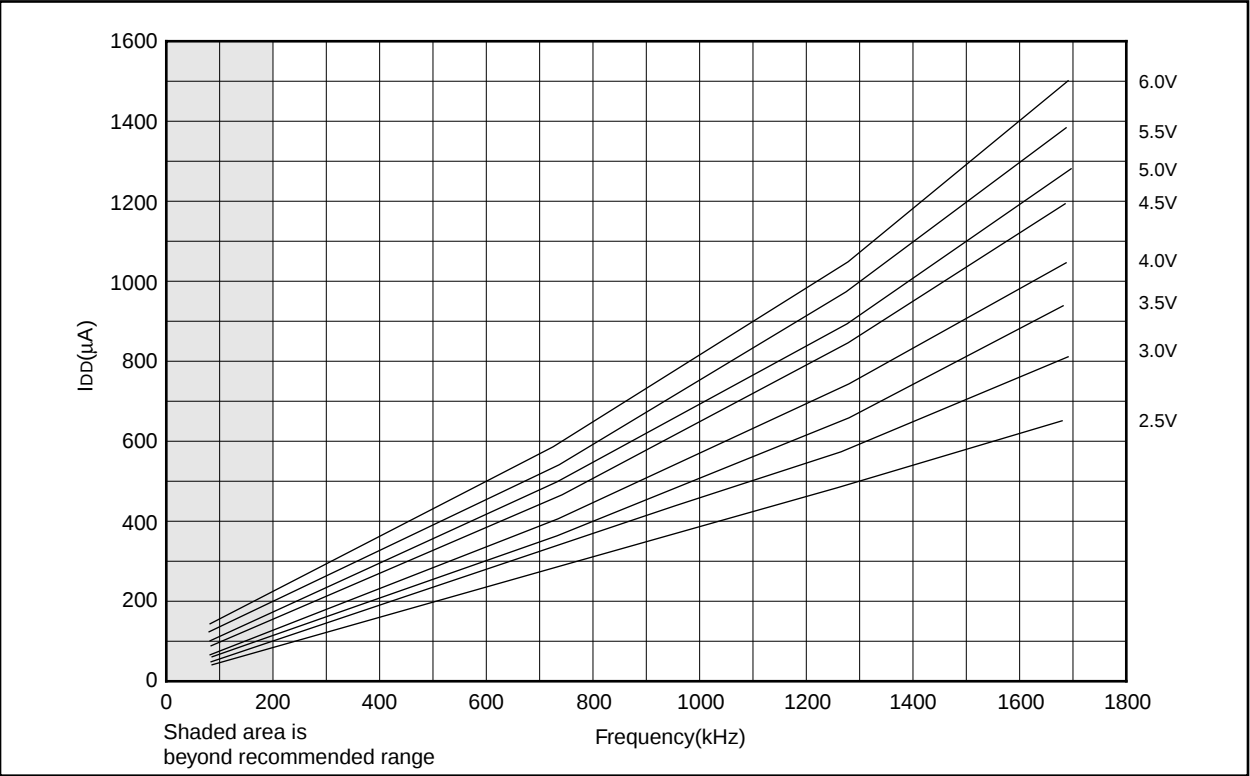
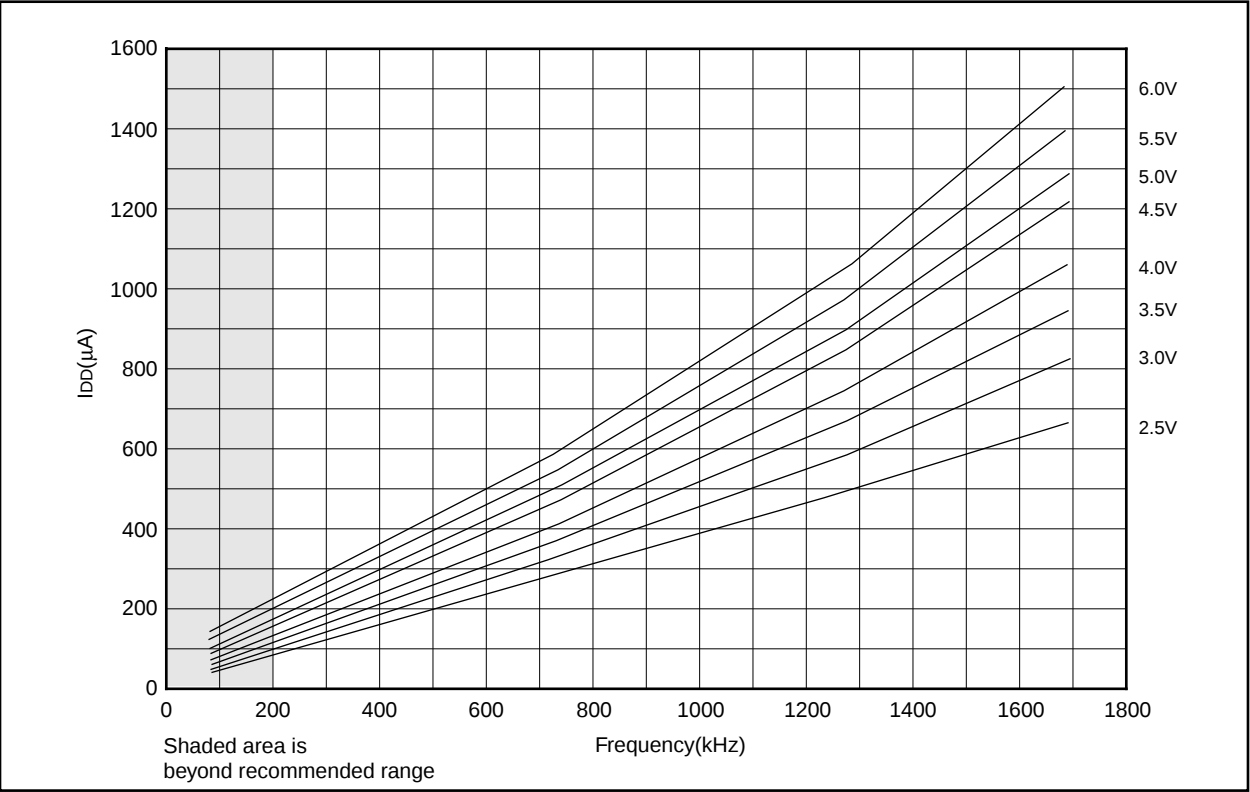


FIGURE 21-15: MAXIMUM I_{DD} vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)

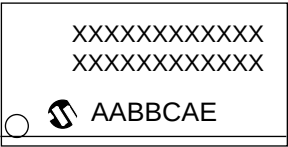


Data based on matrix samples. See first page of this section for details.

PIC16C7X

22.10 Package Marking Information

28-Lead SSOP



Example



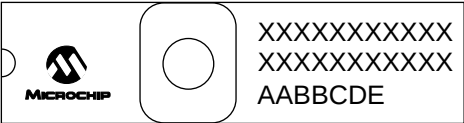
28-Lead PDIP (Skinny DIP)



Example



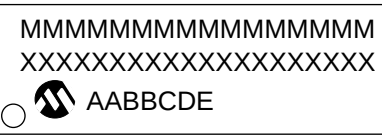
28-Lead Side Brazed Skinny Windowed



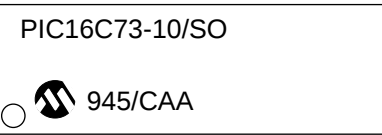
Example



28-Lead SOIC



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calender year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.
	D ₁	Mask revision number for microcontroller
	E	Assembly code of the plant or country of origin in which part was assembled.
	Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIN COMPATIBILITY

Devices that have the same package type and VDD, VSS and MCLR pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only require minor software modification to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

TABLE E-1: PIN COMPATIBLE DEVICES

Pin Compatible Devices	Package
PIC12C508, PIC12C509, PIC12C671, PIC12C672	8-pin
PIC16C154, PIC16CR154, PIC16C156, PIC16CR156, PIC16C158, PIC16CR158, PIC16C52, PIC16C54, PIC16C54A, PIC16CR54A, PIC16C56, PIC16C58A, PIC16CR58A, PIC16C61, PIC16C554, PIC16C556, PIC16C558, PIC16C620, PIC16C621, PIC16C622, PIC16C641, PIC16C642, PIC16C661, PIC16C662, PIC16C710, PIC16C71, PIC16C711, PIC16C715, PIC16F83, PIC16CR83, PIC16F84A, PIC16CR84	18-pin, 20-pin
PIC16C55, PIC16C57, PIC16CR57B	28-pin
PIC16CR62, PIC16C62A, PIC16C63, PIC16CR63, PIC16C66, PIC16C72, PIC16C73A, PIC16C76	28-pin
PIC16CR64, PIC16C64A, PIC16C65A, PIC16CR65, PIC16C67, PIC16C74A, PIC16C77	40-pin
PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, PIC17C44	40-pin
PIC16C923, PIC16C924	64/68-pin
PIC17C756, PIC17C752	64/68-pin

Instruction Set

ADDLW	149
ADDWF	149
ANDLW	149
ANDWF	149
BCF	150
BSF	150
BTFSC	150
BTFSS	151
CALL	151
CLRF	152
CLRW	152
CLRWDT	152
COMF	153
DECF	153
DECFSZ	153
GOTO	154
INCF	154
INCFSZ	155
IORLW	155
IORWF	156
MOVF	156
MOVLW	156
MOVWF	156
NOP	157
OPTION	157
RETFIE	157
RETLW	158
RETURN	158
RLF	159
RRF	159
SLEEP	160
SUBLW	160
SUBWF	161
SWAPF	161
TRIS	161
XORLW	162
XORWF	162
Section	147
Summary Table	148
INT Interrupt	143
INTCON	29
INTCON Register	32
INTEDG bit	31, 143
Internal Sampling Switch (Rss) Impedance	120
Interrupts	129
PortB Change	143
RB7:RB4 Port Change	45
Section	141
TMR0	143
IRP bit	30

L

Loading of PC	40
---------------------	----

M

MCLR	133, 136
Memory	
Data Memory	20
Program Memory	19
Program Memory Maps	
PIC16C72	19
PIC16C73	19
PIC16C73A	19
PIC16C74	19
PIC16C74A	19
PIC16C76	20
PIC16C77	20
Register File Maps	
PIC16C72	21
PIC16C73	21
PIC16C73A	21
PIC16C74	21
PIC16C74A	21
PIC16C76	21
PIC16C77	21
MPASM Assembler	163
MPLAB-C	165
MPSIM Software Simulator	163, 165

O

OERR bit	100
OPCODE	147
OPTION	29
OPTION Register	31
Orthogonal	9
OSC selection	129
Oscillator	
HS	131, 135
LP	131, 135
RC	131
XT	131, 135
Oscillator Configurations	131
Output of TMR2	69

P

P	78, 83
Packaging	
28-Lead Ceramic w/Window	251
28-Lead PDIP	253
28-Lead SOIC	255
28-Lead SSOP	256
40-Lead Cerdip w/Window	252
40-Lead PDIP	254
44-Lead MQFP	258
44-Lead PLCC	257
44-Lead TQFP	259
Paging, Program Memory	40
Parallel Slave Port	50, 54
PCFG0 bit	118
PCFG1 bit	118
PCFG2 bit	118
PCL Register	23, 24, 25, 26, 27, 28, 29, 40
PCLATH	136
PCLATH Register	23, 24, 25, 26, 27, 28, 29, 40
PCON Register	29, 39, 135
PD bit	30, 133, 135
PICDEM-1 Low-Cost PIC16/17 Demo Board	163, 164
PICDEM-2 Low-Cost PIC16CXX Demo Board	163, 164
PICDEM-3 Low-Cost PIC16C9XXX Demo Board	164
PICMASTER In-Circuit Emulator	163

PIC16C7X

Synchronous Serial Port Mode Select bits, SSPM3:SSPM0	79, 84
Synchronous Serial Port Module	77
Synchronous Serial Port Status Register	83

T

T0CS bit	31
T1CKPS0 bit	65
T1CKPS1 bit	65
T1CON	29
T1CON Register	29, 65
T1OSCN bit	65
T1SYNC bit	65
T2CKPS0 bit	70
T2CKPS1 bit	70
T2CON Register	29, 70
TAD	121
Timer Modules, Overview	57
Timer0	

RTCC	136
------------	-----

Timers

Timer0

Block Diagram	59
External Clock	61
External Clock Timing	61
Increment Delay	61
Interrupt	59
Interrupt Timing	60
Overview	57
Prescaler	62
Prescaler Block Diagram	62
Section	59
Switching Prescaler Assignment	63
Synchronization	61
T0CKI	61
T0IF	143
Timing	59
TMR0 Interrupt	143

Timer1

Asynchronous Counter Mode	67
Block Diagram	66
Capacitor Selection	67
External Clock Input	66
External Clock Input Timing	67
Operation in Timer Mode	66
Oscillator	67
Overview	57
Prescaler	66, 68
Resetting of Timer1 Registers	68
Resetting Timer1 using a CCP Trigger Output ..	68
Synchronized Counter Mode	66
T1CON	65
TMR1H	67
TMR1L	67

Timer2

Block Diagram	69
Module	69
Overview	57
Postscaler	69
Prescaler	69
T2CON	70

Timing Diagrams

A/D Conversion	182, 200, 218, 239
Brown-out Reset	134, 175, 209, 228
Capture/Compare/PWM	177, 193, 211, 230
CLKOUT and I/O	174, 190, 208, 227

External Clock Timing	173, 189, 207, 226
I ² C Bus Data	180, 197, 215, 236
I ² C Bus Start/Stop bits	179, 196, 214, 235
I ² C Clock Synchronization	92
I ² C Data Transfer Wait State	90
I ² C Multi-Master Arbitration	92
I ² C Reception (7-bit Address)	95
Parallel Slave Port	194
Power-up Timer	175, 191, 209, 228
Reset	175, 191, 209, 228
SPI Master Mode	87
SPI Mode	178, 195, 213
SPI Mode, Master/Slave Mode, No SS Control	82
SPI Mode, Slave Mode With SS Control	82
SPI Slave Mode (CKE = 1)	88
SPI Slave Mode Timing (CKE = 0)	87
Start-up Timer	175, 191, 209, 228
Time-out Sequence	139
Timer0	59, 176, 192, 210, 229
Timer0 Interrupt Timing	60
Timer0 with External Clock	61
Timer1	176, 192, 210, 229
USART Asynchronous Master Transmission	107
USART Asynchronous Reception	108
USART RX Pin Sampling	104, 105
USART Synchronous Receive	198, 216, 237
USART Synchronous Reception	113
USART Synchronous Transmission	111, 198, 216, 237
Wake-up from Sleep via Interrupt	146
Watchdog Timer	175, 191, 209, 228
TMR0	29
TMR0 Register	25, 27
TMR1CS bit	65
TMR1H	29
TMR1H Register	23, 25, 27
TMR1IE bit	33
TMR1IF bit	35, 36
TMR1L	29
TMR1L Register	23, 25, 27
TMR1ON bit	65
TMR2	29
TMR2 Register	23, 25, 27
TMR2IE bit	33
TMR2IF bit	35, 36
TMR2ON bit	70
TO bit	30
TOUTPS0 bit	70
TOUTPS1 bit	70
TOUTPS2 bit	70
TOUTPS3 bit	70
TRISA	29
TRISA Register	24, 26, 28, 43
TRISB	29
TRISB Register	24, 26, 28, 45
TRISC	29
TRISC Register	24, 26, 28, 48
TRISD	29
TRISD Register	26, 28, 50
TRISE	29
TRISE Register	26, 28, 51
Two's Complement	9
TXIE bit	34
TXIF bit	36
TXREG	29
TXSTA	29
TXSTA Register	99

U

UA	78, 83
Universal Synchronous Asynchronous Receiver Transmitter (USART)	99
Update Address bit, UA	78, 83
USART	
Asynchronous Mode	106
Asynchronous Receiver	108
Asynchronous Reception	109
Asynchronous Transmission	107
Asynchronous Transmitter	106
Baud Rate Generator (BRG)	101
Receive Block Diagram	108
Sampling	104
Synchronous Master Mode	110
Synchronous Master Reception	112
Synchronous Master Transmission	110
Synchronous Slave Mode	114
Synchronous Slave Reception	114
Synchronous Slave Transmit	114
Transmit Block Diagram	106
UV Erasable Devices	7

W

W Register	
ALU	9
Wake-up from SLEEP	145
Watchdog Timer (WDT)	129, 133, 136, 144
WCOL	79, 84
WDT	136
Block Diagram	144
Period	144
Programming Considerations	144
Timeout	136
Word	129
WR pin	54
Write Collision Detect bit, WCOL	79, 84

X

XMIT_MODE	98
-----------------	----

Z

Z bit	30
Zero bit	9

LIST OF EXAMPLES

Example 3-1:	Instruction Pipeline Flow.....	17
Example 4-1:	Call of a Subroutine in Page 1 from Page 0	41
Example 4-2:	Indirect Addressing	41
Example 5-1:	Initializing PORTA.....	43
Example 5-2:	Initializing PORTB.....	45
Example 5-3:	Initializing PORTC	48
Example 5-4:	Read-Modify-Write Instructions on an I/O Port	53
Example 7-1:	Changing Prescaler (Timer0→WDT).....	63
Example 7-2:	Changing Prescaler (WDT→Timer0).....	63
Example 8-1:	Reading a 16-bit Free-Running Timer	67
Example 10-1:	Changing Between Capture Prescalers.....	73
Example 10-2:	PWM Period and Duty Cycle Calculation	75
Example 11-1:	Loading the SSPBUF (SSPSR) Register	80
Example 11-2:	Loading the SSPBUF (SSPSR) Register (PIC16C76/77)	85
Example 12-1:	Calculating Baud Rate Error	101
Equation 13-1:	A/D Minimum Charging Time.....	120
Example 13-1:	Calculating the Minimum Required Acquisition Time	120
Example 13-2:	A/D Conversion.....	122
Example 13-3:	4-bit vs. 8-bit Conversion Times	123
Example 14-1:	Saving STATUS, W, and PCLATH Registers in RAM.....	143

LIST OF TABLES

Table 1-1:	PIC16C7XX Family of Devices	6	Table 12-8:	Registers Associated with Synchronous Master Transmission	111
Table 3-1:	PIC16C72 Pinout Description	13	Table 12-9:	Registers Associated with Synchronous Master Reception	112
Table 3-2:	PIC16C73/73A/76 Pinout Description	14	Table 12-10:	Registers Associated with Synchronous Slave Transmission	115
Table 3-3:	PIC16C74/74A/77 Pinout Description	15	Table 12-11:	Registers Associated with Synchronous Slave Reception	115
Table 4-1:	PIC16C72 Special Function Register Summary	23	Table 13-1:	TAD vs. Device Operating Frequencies	121
Table 4-2:	PIC16C73/73A/74/74A Special Function Register Summary	25	Table 13-2:	Registers/Bits Associated with A/D, PIC16C72	126
Table 4-3:	PIC16C76/77 Special Function Register Summary	27	Table 13-3:	Summary of A/D Registers, PIC16C73/73A/74/74A/76/77	127
Table 5-1:	PORTA Functions	44	Table 14-1:	Ceramic Resonators	131
Table 5-2:	Summary of Registers Associated with PORTA	44	Table 14-2:	Capacitor Selection for Crystal Oscillator	131
Table 5-3:	PORTB Functions	46	Table 14-3:	Time-out in Various Situations, PIC16C73/74	135
Table 5-4:	Summary of Registers Associated with PORTB	47	Table 14-4:	Time-out in Various Situations, PIC16C72/73A/74A/76/77	135
Table 5-5:	PORTC Functions	48	Table 14-5:	Status Bits and Their Significance, PIC16C73/74	135
Table 5-6:	Summary of Registers Associated with PORTC	49	Table 14-6:	Status Bits and Their Significance, PIC16C72/73A/74A/76/77	136
Table 5-7:	PORTD Functions	50	Table 14-7:	Reset Condition for Special Registers	136
Table 5-8:	Summary of Registers Associated with PORTD	50	Table 14-8:	Initialization Conditions for all Registers	136
Table 5-9:	PORTE Functions	52	Table 15-1:	Opcode Field Descriptions	147
Table 5-10:	Summary of Registers Associated with PORTE	52	Table 15-2:	PIC16CXX Instruction Set	148
Table 5-11:	Registers Associated with Parallel Slave Port	55	Table 16-1:	Development Tools from Microchip	166
Table 7-1:	Registers Associated with Timer0	63	Table 17-1:	Cross Reference of Device Specs for Oscillator Configurations and Frequencies of Operation (Commercial Devices)	167
Table 8-1:	Capacitor Selection for the Timer1 Oscillator	67	Table 17-2:	External Clock Timing Requirements	173
Table 8-2:	Registers Associated with Timer1 as a Timer/Counter	68	Table 17-3:	CLKOUT and I/O Timing Requirements	174
Table 9-1:	Registers Associated with Timer2 as a Timer/Counter	70	Table 17-4:	Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer, and brown-out Reset Requirements	175
Table 10-1:	CCP Mode - Timer Resource	71	Table 17-5:	Timer0 and Timer1 External Clock Requirements	176
Table 10-2:	Interaction of Two CCP Modules	71	Table 17-6:	Capture/Compare/PWM Requirements (CCP1)	177
Table 10-3:	Example PWM Frequencies and Resolutions at 20 MHz	75	Table 17-7:	SPI Mode Requirements	178
Table 10-4:	Registers Associated with Capture, Compare, and Timer1	75	Table 17-8:	I ² C Bus Start/Stop Bits Requirements	179
Table 10-5:	Registers Associated with PWM and Timer2	76	Table 17-9:	I ² C Bus Data Requirements	180
Table 11-1:	Registers Associated with SPI Operation	82	Table 17-10:	A/D Converter Characteristics: PIC16C72-04 (Commercial, Industrial, Extended) PIC16C72-10 (Commercial, Industrial, Extended) PIC16C72-20 (Commercial, Industrial, Extended) PIC16LC72-04 (Commercial, Industrial)	181
Table 11-2:	Registers Associated with SPI Operation (PIC16C76/77)	88	Table 17-11:	A/D Conversion Requirements	182
Table 11-3:	I ² C Bus Terminology	89	Table 18-1:	Cross Reference of Device Specs for Oscillator Configurations and Frequencies of Operation (Commercial Devices)	183
Table 11-4:	Data Transfer Received Byte Actions	94			
Table 11-5:	Registers Associated with I ² C Operation	97			
Table 12-1:	Baud Rate Formula	101			
Table 12-2:	Registers Associated with Baud Rate Generator	101			
Table 12-3:	Baud Rates for Synchronous Mode	102			
Table 12-4:	Baud Rates for Asynchronous Mode (BRGH = 0)	102			
Table 12-5:	Baud Rates for Asynchronous Mode (BRGH = 1)	103			
Table 12-6:	Registers Associated with Asynchronous Transmission	107			
Table 12-7:	Registers Associated with Asynchronous Reception	109			