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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c77-04e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C7X device.

Device	Program Memory	Data Memory
PIC16C72	2K x 14	128 x 8
PIC16C73	4K x 14	192 x 8
PIC16C73A	4K x 14	192 x 8
PIC16C74	4K x 14	192 x 8
PIC16C74A	4K x 14	192 x 8
PIC16C76	8K x 14	368 x 8
PIC16C77	8K x 14	386 x 8

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow bit and a digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (2)
Bank 1									-		
80h <sup>(4)</sup>	INDF	Addressing	this location	uses conter	ts of FSR to a	ddress data i	memory (not	a physical re	gister)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h <sup>(4)</sup>	PCL	Program Co	ounter's (PC)	Least Signif	ficant Byte					0000 0000	0000 0000
83h <sup>(4)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000g guuu
84h <sup>(4)</sup>	FSR	Indirect data	a memory ac	ldress pointe	er				-	xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	PORTA Dat	a Direction Re	gister				11 1111	11 1111
86h	TRISB	PORTB Dat	ta Direction F	Register						1111 1111	1111 1111
87h	TRISC	PORTC Da	ta Direction I	Register						1111 1111	1111 1111
88h <sup>(5)</sup>	TRISD	PORTD Da	ta Direction I	Register						1111 1111	1111 1111
89h <b>(5)</b>	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Dat	ta Direction E	Bits	0000 -111	0000 -111
8Ah <sup>(1,4)</sup>	PCLATH	_	_	_	Write Buffer fo	or the upper	5 bits of the I	Program Cou	inter	0 0000	0 0000
8Bh <sup>(4)</sup>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	PSPIE <sup>(3)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	_	—	_	_	—	_	_	CCP2IE	0	0
8Eh	PCON	_	—	—	_	_	_	POR	BOR	dd	uu
8Fh	—	Unimpleme	nted							—	—
90h	—	Unimpleme	nted							—	—
91h	_	Unimpleme	nted							—	—
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	us Serial Por	t (I <sup>2</sup> C mode)	Address Regis	ter				0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/Ā	Р	S	R/W	UA	BF	0000 0000	0000 0000
95h	—	Unimpleme	nted							—	—
96h	_	Unimpleme	nted							—	—
97h	-	Unimpleme	nted							-	—
98h	TXSTA	CSRC	ТХ9	TXEN	SYNC	-	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generator R	egister					-	0000 0000	0000 0000
9Ah	-	Unimpleme	nted							-	—
9Bh	-	Unimpleme	nted							-	—
9Ch	_	Unimpleme	nted							_	_
9Dh	_	Unimpleme	nted							_	_
9Eh	_	Unimpleme	nted							_	_
9Fh	ADCON1	—	_	_	—	—	PCFG2	PCFG1	PCFG0	000	000

## TABLE 4-3: PIC16C76/77 SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the PIC16C76, always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD and PORTE are not physically implemented on the PIC16C76, read as '0'.

### 4.2.2.1 STATUS REGISTER Applicable Devices 72|73|73A|74|74A|76|77

The STATUS register, shown in Figure 4-7, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

- **Note 1:** For those devices that do not use bits IRP and RP1 (STATUS<7:6>), maintain these bits clear to ensure upward compatibility with future products.
- Note 2: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

R/W-0	R/W-0	R/W-0	<u>R-1</u>	<u>R-1</u>	R/W-x	R/W-x	R/W-x	
IRP bit7	RP1	RP0	TO	PD	Z	DC	C bit0	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset
bit 7:	<b>IRP</b> : Regis 1 = Bank 2 0 = Bank 0	ster Bank \$ 2, 3 (100h 0, 1 (00h -	Select bit ( - 1FFh) FFh)	(used for ir	ndirect addr	essing)		
bit 6-5:	<b>RP1:RP0</b> : 11 = Bank 10 = Bank 01 = Bank 00 = Bank Each bank	Register I 3 (180h - 2 (100h - 3 (80h - F 3 (0 (00h - 7 4 is 128 by	3ank Sele 1FFh) 17Fh) FFh) 7Fh) ⁄tes	ct bits (use	ed for direct	addressin	g)	
bit 4:	$\overline{\mathbf{TO}}$ : Time- 1 = After p 0 = A WD	out bit ower-up, o T time-out	CLRWDT in	struction,	or sleep in	struction		
bit 3:	<b>PD</b> : Power 1 = After p 0 = By exe	r-down bit ower-up c ecution of t	or by the C the SLEEF	LRWDT ins	truction n			
bit 2:	<b>Z</b> : Zero bit 1 = The re 0 = The re	sult of an	arithmetic arithmetic	or logic or or logic or	peration is z	ero not zero		
bit 1:	<b>DC</b> : Digit of 1 = A carry 0 = No car	carry/borrc y-out from rry-out froi	w bit (ADD the 4th lo m the 4th ł	WF, ADDLW W order bit	N, SUBLW, S t of the resu bit of the res	UBWF instr Ilt occurred Sult	uctions) (fo I	r $\overline{\mathrm{borrow}}$ the polarity is reversed)
bit 0:	C: Carry/b 1 = A carr 0 = No car Note: For second op the source	orrow bit ( y-out from rry-out fror borrow the perand. Fo e register.	ADDWF, AI the most n the mos polarity is r rotate (R:	DLW , SUB significant t significar s reversed RF, RLF) ir	LW, SUBWF bit of the rent bit of the A subtract structions,	instruction esult occurr result occu ion is exec this bit is lo	ns) red irred uted by add baded with	ding the two's complement of the either the high or low order bit of

# FIGURE 4-7: STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

# FIGURE 4-11: PIE1 REGISTER PIC16C73/73A/74/74A/76/77 (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0							
PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	R	= Readable bit					
bit7							bit0	W	= Writable bit = Unimplemented bit					
								ľ	read as '0'					
	(1)							- n	= Value at POR reset					
bit 7:	PSPIE <sup>(1)</sup> :	Parallel S	lave Port	Read/Writ	e Interrupt	Enable bit								
	1 = Enabl	es the PS	P read/wr	ite interrup	ot •••									
	U = Disables the PSP read/write interrupt													
bit 6:	ADIE: A/D Converter Interrupt Enable bit													
	1 = Enable 0 = Disable 0	les the Α/L	) interrupt	ŀ										
hit E.				.nt Enchla	hit									
DIL D.	1 – Enabl	AKI KECE		ve interru	) DIL Dt									
	0 = Disab	les the US	SART rece	ive interru	ipt									
bit 4:	TXIE: US	ART Trans	mit Interru	upt Enable	e bit									
	1 = Enabl	es the US	ART trans	mit interru	upt									
	0 = Disab	les the US	SART trans	smit interr	upt									
bit 3:	SSPIE: S	ynchronou	is Serial F	ort Interru	pt Enable b	oit								
	1 = Enabl	es the SS	P interrup	t										
	0 = Disab	les the SS	SP interrup	ot										
bit 2:	CCP1IE:	CCP1 Inte	rrupt Ena	ble bit										
	1 = Enabl	es the CC	P1 interru	pt										
	0 = Disab	les the CC	P1 Interru	lpt										
bit 1:	TMR2IE:	TMR2 to F	PR2 Match	Interrupt	Enable bit									
	1 = Enable 0 = Disable 1	es the TM		2 match in 2 match ir	terrupt									
L:4 0.														
DIT U:	1 MR11E:	IMR1 OVE	R1 overflo	rrupt Enat										
	0 = Disab	les the TM	IR1 overfl	ow interru	Dt									
	2.2.0				1									
Note 1:	PIC16C7	3/73A/76 d	devices do	not have	a Parallel S	Slave Port i	implemente	d, t	his bit location is reserved					
	on these	devices, a	lways mai	ntain this l	bit clear.									

## TABLE 5-9:PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/RD/AN5	bit0	ST/TTL <sup>(1)</sup>	Input/output port pin or read control input in parallel slave port mode or analog input: RD 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/WR/AN6	bit1	ST/TTL <sup>(1)</sup>	Input/output port pin or write control input in parallel slave port mode or analog input: WR 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected)
RE2/CS/AN7	bit2	ST/TTL <sup>(1)</sup>	Input/output port pin or chip select control input in parallel slave port mode or analog input: $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE	—	_	—	—	_	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Da	ta Direction	Bits	0000 -111	0000 -111
9Fh	ADCON1	_	_	_	—	—	PCFG2	PCFG1	PCFG0	000	000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTE.

# 11.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

### 11.1 <u>SSP Module Overview</u>

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I<sup>2</sup>C)

The SSP module in  $I^2C$  mode works the same in all PIC16C7X devices that have an SSP module. However the SSP Module in SPI mode has differences between the PIC16C76/77 and the other PIC16C7X devices.

The register definitions and operational description of SPI mode has been split into two sections because of the differences between the PIC16C76/77 and the other PIC16C7X devices. The default reset values of both the SPI modules is the same regardless of the device:

11.2	SPI Mode for PIC16C72/73/73A/74/74A78	В
11.3	SPI Mode for PIC16C76/7783	3
11.4	I2C <sup>™</sup> Overview89	Э
11.5	SSP I2C Operation	3

Refer to Application Note AN578, "Use of the SSP Module in the  $l^2C$  Multi-Master Environment."

The  $\overline{SS}$  pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set the for synchronous slave mode to be enabled. When the  $\overline{SS}$  pin is low, transmission and reception are enabled and the SDO pin is driven. When the  $\overline{SS}$  pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the  $\overline{SS}$  pin is taken low without resetting SPI mode, the transmission will continue from the

point at which it was taken high. External pull-up/ pull-down resistors may be desirable, depending on the application.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.









Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1,2)</sup>	ADIF	RCIF <sup>(2)</sup>	TXIF <sup>(2)</sup>	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1,2)</sup>	ADIE	RCIE <sup>(2)</sup>	TXIE <sup>(2)</sup>	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
87h	TRISC	PORTC Da	ta Directio	on Registe	er					1111 1111	1111 1111
13h	SSPBUF	Synchrono	us Serial I	Port Rece	ive Buffer	/Transmit	Register			xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
85h	TRISA	—	_	PORTA I	PORTA Data Direction Register						11 1111
94h	SSPSTAT	—	—	D/Ā	Р	S	R/W	UA	BF	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port or USART, these bits are unimplemented, read as '0'.

### 13.1 A/D Acquisition Requirements

# Applicable Devices 72 73 73 74 74 76 77

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 13-4. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), Figure 13-4. The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 10 k $\Omega$ . After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 13-1 may be used. This equation calculates the acquisition time to within 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

# EQUATION 13-1: A/D MINIMUM CHARGING TIME

 $VHOLD = (VREF - (VREF/512)) \bullet (1 - e^{(-TCAP/CHOLD(RIC + RSS + RS))})$ 

Given: VHOLD = (VREF/512), for 1/2 LSb resolution

The above equation reduces to:

 $TCAP = -(51.2 \text{ pF})(1 \text{ k}\Omega + \text{Rss} + \text{Rs}) \ln(1/511)$ 

Example 13-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

CHOLD = 51.2 pF

Rs = 10 kΩ

1/2 LSb error

## FIGURE 13-4: ANALOG INPUT MODEL

 $VDD = 5V \rightarrow Rss = 7 \text{ k}\Omega$ 

Temp (application system max.) = 50°C

VHOLD = 0 @ t = 0

- Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.
- Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **Note 3:** The maximum recommended impedance for analog sources is 10 k $\Omega$ . This is required to meet the pin leakage specification.
- Note 4: After a conversion has completed, a 2.0TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

#### EXAMPLE 13-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

- TACQ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient
- TACQ =  $5 \mu s + TCAP + [(Temp 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$
- TCAP = -CHOLD (Ric + Rss + Rs) ln(1/511)-51.2 pF (1 k $\Omega$  + 7 k $\Omega$  + 10 k $\Omega$ ) ln(0.0020) -51.2 pF (18 k $\Omega$ ) ln(0.0020) -0.921 µs (-6.2364) 5.747 µs
- TACQ = 5 μs + 5.747 μs + [(50°C 25°C)(0.05 μs/°C)] 10.747 μs + 1.25 μs 11.997 μs



# 14.0 SPECIAL FEATURES OF THE CPU

Applicable Devices 72 73 73A 74 74A 76 77

What sets a microcontroller apart from other processors are special circuits to deal with the needs of realtime applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- · Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- · In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

# 14.1 Configuration Bits

Applicable Devices

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

#### FIGURE 14-1: CONFIGURATION WORD FOR PIC16C73/74

_				_			CP1	CPO		WDTE	EOSC1	FOSCO	Pegister:	CONFIG
bit13			_				UFI	CFU	FVIRIL	WDIL	10301	bit0	Address	2007h
bit 13-5:	Unimplen	nented	: Read	as '1'										
bit 4:	<b>CP1:CP0</b> : 11 = Code 10 = Uppe 01 = Uppe 00 = All m	Code e protec er half c er 3/4th emory	protecti ction off of progr of prog is code	on bits f am me gram m e protec	mory c emory ted	ode pro code p	otected rotecte	d						
bit 3:	<b>PWRTE</b> : F 1 = Power 0 = Power	Power-u -up Tin -up Tin	up Time her ena her disa	r Enab bled ıbled	le bit									
bit 2:	<b>WDTE</b> : Wa 1 = WDT e 0 = WDT e	atchdog enableo disable	g Timer ป d	Enable	e bit									
bit 1-0:	FOSC1:F0 11 = RC o 10 = HS o 01 = XT o 00 = LP o	OSCO: oscillato oscillato scillato scillato	Oscillat or or r r	tor Sele	ection b	its								

# 14.3 <u>Reset</u> Applicable Devices 72|73|73A|74|74A|76|77

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- MCLR reset during normal operation
- MCLR reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR) (PIC16C72/73A/74A/76/ 77)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the  $\overline{\text{MCLR}}$  and WDT Reset, on  $\overline{\text{MCLR}}$  reset during SLEEP, and Brownout Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different reset situations as indicated in Table 14-5 and Table 14-6. These bits are used in software to determine the nature of the reset. See Table 14-8 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 14-8.

The PIC16C72/73A/74A/76/77 have a  $\overline{\text{MCLR}}$  noise filter in the  $\overline{\text{MCLR}}$  reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive  $\overline{\text{MCLR}}$  pin low.





#### 14.7 Watchdog Timer (WDT) **Applicable Devices** 72 73 73A 74 74A 76 77

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 14.1).

#### 14.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a



FIGURE 14-18: WATCHDOG TIMER BLOCK DIAGRAM

prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The TO bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

14.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.



# FIGURE 14-19: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN <sup>(1)</sup>	CP1	CP0	PWRTE <sup>(1)</sup>	WDTE	FOSC1	FOSC0
81h,181h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 14-1, and Figure 14-2 for operation of these bits.

# Applicable Devices 72 73 73A 74 74A 76 77

### 17.1 DC Characteristics: PIC16C72-04 (Commercial, Industrial, Extended) PIC16C72-10 (Commercial, Industrial, Extended) PIC16C72-20 (Commercial, Industrial, Extended)

			Standa	ard Ope	erating	g Cond	litions (unless otherwise stated)
DC CHA	RACTERISTICS		Operat	ing tem	peratu	re -4۔ 1-	$10^{\circ}$ C $\leq$ IA $\leq$ +125 °C for extended, $10^{\circ}$ C $\leq$ TA $\leq$ +85 °C for industrial and
						0°	$C \leq TA \leq +70^{\circ}C$ for commercial
Param No.	Characteristic	Sym	Min	Тур†	Мах	Units	Conditions
D001 D001A	Supply Voltage	Vdd	4.0 4.5	-	6.0 5.5	> >	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power- on Reset Signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset Signal	Svdd	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
			3.7	4.0	4.4	V	Extended Only
D010	Supply Current (Note 2,5)	IDD	-	2.7	5.0	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D015	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled VDD = 5.0V
D020	Power-down Current	IPD	-	10.5	42	μΑ	VDD = 4.0V, WDT enabled, $-40^{\circ}$ C to $+85^{\circ}$ C
D021	(Note 3,5)		-	1.5	16	μA	$VDD = 4.0V$ , WDT disabled, $-0^{\circ}C$ to $+70^{\circ}C$
D021A				1.5	19	μΑ μΑ	$VD = 4.0V$ , $VD T$ disabled, $-40^{\circ}C$ to $+85^{\circ}C$
D023	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled $VDD = 5.0V$

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD  $\overline{MCLR}$  = VDD; WDT enabled/disabled as specified.

The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VbD and Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

# Applicable Devices 72 73 73A 74 74A 76 77

# FIGURE 17-3: CLKOUT AND I/O TIMING



TABLE 17-3:	<b>CLKOUT AND I/O TIMING REQUIREMENTS</b>

Parameter	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
No.								
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		_	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid		—	—	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		Tosc + 200	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	_	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		_	50	150	ns	
18*	TosH2iol	OSC1 <sup>↑</sup> (Q2 cycle) to PIC16 <b>C</b> 72		100	—	_	ns	
		Port input invalid (I/O in hold time) PIC16LC72		200	—	_	ns	
19*	TioV2osH	Port input valid to OSC1 <sup>↑</sup> (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time PIC16 <b>C</b> 72		—	10	40	ns	
		PIC16 <b>LC</b> 72		_	—	80	ns	
21*	TioF	Port output fall time PIC16 <b>C</b> 72		—	10	40	ns	
		PIC16 <b>LC</b> 72		—	_	80	ns	
22††*	Tinp	INT pin high or low time		Тсү	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high	or low time	Тсү	_	—	ns	

 $^{\ast}$  These parameters are characterized but not tested.

†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

these parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

Applicable Devices 72 73 73A 74 74A 76 77

# 18.0 ELECTRICAL CHARACTERISTICS FOR PIC16C73/74

### Absolute Maximum Ratings †

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR. and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	0.3 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	0 to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iικ (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Ioк (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sunk by PORTC and PORTD (combined) (Note 3)	200 mA
Maximum current sourced by PORTC and PORTD (combined) (Note 3)	200 mA
<b>Note 1:</b> Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VDD - VOH)	$x \text{ IOH} + \sum (\text{VOI } x \text{ IOL})$

- **Note 2:** Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.
- Note 3: PORTD and PORTE are not implemented on the PIC16C73.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# TABLE 18-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C73-04 PIC16C74-04	PIC16C73-10 PIC16C74-10	PIC16C73-20 PIC16C74-20	PIC16LC73-04 PIC16LC74-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 μA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 13.5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 μA max. at 4V Freq: 4 MHz max.
хт	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 μA max. at 4V Freq: 4 MHz max.	VDD:         4.5V to 5.5V         VDD:         4.5V to 5.5V         V           IDD:         2.7 mA typ. at 5.5V         IDD:         2.7 mA typ. at 5.5V         IDD:         2.7 mA typ. at 5.5V         IDD:           IPD:         1.5 μA typ. at 4V         IPD:         1.5 μA typ. at 4V         IPD:         1.5 μA typ. at 4V         IPD:           Freq:         4 MHz max.         Freq:         4 MHz max.         Freq:         4 MHz max.		VDD: 3.0V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 13.5 μA max. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 μA max. at 4V Freq: 4 MHz max.
нs	VDD:         4.5V to 5.5V           IDD:         13.5 mA typ. at 5.5V           IPD:         1.5 μA typ. at 4.5V           Freq:         4 MHz max.	VDD:         4.5V to 5.5V           IDD:         15 mA max. at 5.5V           IPD:         1.5 μA typ. at 4.5V           Freq:         10 MHz max.	VDD:         4.5V to 5.5V           IDD:         30 mA max. at 5.5V           IPD:         1.5 μA typ. at 4.5V           Freq:         20 MHz max.	Not recommended for use in HS mode	VDD:         4.5V to 5.5V           IDD:         30 mA max. at 5.5V           IPD:         1.5 μA typ. at 4.5V           Freq:         20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 μA typ. at 32 kHz, 4.0V IPD: 0.9 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 3.0V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 13.5 μA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 μA max. at 32 kHz, 3.0V IPD: 13.5 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

# Applicable Devices 72 73 73A 74 74A 76 77

## FIGURE 18-11: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



#### TABLE 18-11: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 <b>C</b> 73/74		_	80	ns	
		Clock high to data out valid	PIC16 <b>LC</b> 73/74	—	-	100	ns	
121	Tckrf	Clock out rise time and fall time	PIC16 <b>C</b> 73/74	—	—	45	ns	
		(Master Mode)	PIC16 <b>LC</b> 73/74	—	-	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC16 <b>C</b> 73/74	—	—	45	ns	
			PIC16 <b>LC</b> 73/74		—	50	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### FIGURE 18-12: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



## TABLE 18-12: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
125	TdtV2ckL	$\frac{\text{SYNC RCV (MASTER \& SLAVE)}}{\text{Data setup before CK} \downarrow (\text{DT setup time})}$	15		_	ns	
126	TckL2dtl	Data hold after CK $\downarrow$ (DT hold time)	15	_	—	ns	

+: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16C7X

# Applicable Devices 72 73 73A 74 74A 76 77



#### FIGURE 20-17: A/D CONVERSION TIMING

### TABLE 20-14: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
130	TAD	A/D clock period	PIC16 <b>C</b> 76/77	1.6	_	_	μs	Tosc based, VREF ≥ 3.0V
			PIC16LC76/77	2.0	_	—	μs	Tosc based, VREF full range
			PIC16 <b>C</b> 76/77	2.0	4.0	6.0	μs	A/D RC Mode
			PIC16LC76/77	3.0	6.0	9.0	μs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		_	9.5		TAD	
132	TACQ	Acquisition time		Note 2	20	—	μs	
				5*		_	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start		_	Tosc/2 §	_	_	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
135	Tswc	Switching from convert	$\rightarrow$ sample time	1.5 §	—		TAD	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 13.1 for min conditions.

# 22.3 28-Lead Plastic Dual In-line (300 mil) (SP)



	Package Group: Plastic Dual In-Line (PLA)							
		Millimeters			Inches			
Symbol	Min	Max	Notes	Min	Max	Notes		
α	0°	10°		0°	10°			
Α	3.632	4.572		0.143	0.180			
A1	0.381	_		0.015	_			
A2	3.175	3.556		0.125	0.140			
В	0.406	0.559		0.016	0.022			
B1	1.016	1.651	Typical	0.040	0.065	Typical		
B2	0.762	1.016	4 places	0.030	0.040	4 places		
B3	0.203	0.508	4 places	0.008	0.020	4 places		
С	0.203	0.331	Typical	0.008	0.013	Typical		
D	34.163	35.179		1.385	1.395			
D1	33.020	33.020	Reference	1.300	1.300	Reference		
E	7.874	8.382		0.310	0.330			
E1	7.112	7.493		0.280	0.295			
e1	2.540	2.540	Typical	0.100	0.100	Typical		
eA	7.874	7.874	Reference	0.310	0.310	Reference		
eB	8.128	9.652		0.320	0.380			
L	3.175	3.683		0.125	0.145			
N	28	-		28	-			
S	0.584	1.220		0.023	0.048			

# 22.7 44-Lead Plastic Leaded Chip Carrier (Square)(PLCC)



	Pa	ckage Group: F	Plastic Leaded C	hip Carrier (PL	CC)		
		Millimeters		Inches			
Symbol	Min	Мах	Notes	Min	Max	Notes	
А	4.191	4.572		0.165	0.180		
A1	2.413	2.921		0.095	0.115		
D	17.399	17.653		0.685	0.695		
D1	16.510	16.663		0.650	0.656		
D2	15.494	16.002		0.610	0.630		
D3	12.700	12.700	Reference	0.500	0.500	Reference	
E	17.399	17.653		0.685	0.695		
E1	16.510	16.663		0.650	0.656		
E2	15.494	16.002		0.610	0.630		
E3	12.700	12.700	Reference	0.500	0.500	Reference	
N	44	44		44	44		
CP	-	0.102		_	0.004		
LT	0.203	0.381		0.008	0.015		

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