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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc74a-04i-l

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NOTES:

#### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. The special function registers can be classified into two sets (core and peripheral). Those registers associated with the "core" functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (3)
Bank 0											
00h <sup>(1)</sup>	INDF	Addressing	this location	uses conten	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Signif	icant Byte					0000 0000	0000 0000
03h <sup>(1)</sup>	STATUS	IRP <sup>(4)</sup>	RP1 <sup>(4)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h <sup>(1)</sup>	FSR	Indirect data	a memory ad	dress pointe	er					XXXX XXXX	uuuu uuuu
05h	PORTA	—	—	PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read		0x 0000	0u 0000
06h	PORTB	PORTB Dat	a Latch whe	n written: PC	ORTB pins wh	nen read				xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Dat	ta Latch whe	n written: PC	ORTC pins w	nen read				xxxx xxxx	uuuu uuuu
08h	_	Unimpleme	nted							—	—
09h	_	Unimpleme	nted							_	_
0Ah <sup>(1,2)</sup>	PCLATH	_	_	—	Write Buffer	for the uppe	er 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh <b>(1)</b>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
0Dh	_	Unimpleme	nted							—	_
0Eh	TMR1L	Holding reg	Holding register for the Least Significant Byte of the 16-bit TMR1 register						xxxx xxxx	uuuu uuuu	
0Fh	TMR1H	Holding reg	ister for the N	Aost Signific	ant Byte of th	ne 16-bit TMF	R1 register			xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronou	is Serial Port	Receive Bu	ffer/Transmit	Register				xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Co	mpare/PWM	Register (LS	SB)					xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Co	mpare/PWM	Register (M	SB)					XXXX XXXX	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
18h	_	Unimpleme	nted							_	_
19h	_	Unimplemented						_	_		
1Ah	-	Unimpleme	Unimplemented						—	_	
1Bh	_	Unimpleme	Unimplemented						_	_	
1Ch	_	Unimpleme	Unimplemented							_	_
1Dh	_	Unimpleme	nted							_	_
1Eh	ADRES	A/D Result	Register							xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	0000 00-0

TABLE 4-1: PIC16C72 SPECIAL FUNCTION REGISTER SUMMARY

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C72, always maintain these bits clear.

### 5.7 Parallel Slave Port Applicable Devices 72 73 73 74 74 76 77

PORTD operates as an 8-bit wide Parallel Slave Port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through  $\overline{RD}$  control input pin RE0/ $\overline{RD}$ /AN5 and  $\overline{WR}$  control input pin RE1/ $\overline{WR}$ /AN6.

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD/AN5 to be the RD input, RE1/ WR/AN6 to be the WR input and RE2/CS/AN7 to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set) and the A/D port configuration bits PCFG2:PCFG0 (ADCON1<2:0>) must be set, which will configure pins RE2:RE0 as digital I/O.

There are actually two 8-bit latches, one for data-out (from the PIC16/17) and one for data input. The user writes 8-bit data to PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored, since the microprocessor is controlling the direction of data flow.

A write to the PSP occurs when both the  $\overline{CS}$  and  $\overline{WR}$ lines are first detected low. When either the  $\overline{CS}$  or  $\overline{WR}$ lines become high (level triggered), then the Input Buffer Full status flag bit IBF (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete (Figure 5-12). The interrupt flag bit PSPIF (PIR1<7>) is also set on the same Q4 clock cycle. IBF can only be cleared by reading the PORTD input latch. The input Buffer Overflow status flag bit IBOV (TRISE<5>) is set if a second write to the Parallel Slave Port is attempted when the previous byte has not been read out of the buffer.

A read from the PSP occurs when both the  $\overline{CS}$  and  $\overline{RD}$  lines are first detected low. The Output Buffer Full status flag bit OBF (TRISE<6>) is cleared immediately (Figure 5-13) indicating that the PORTD latch is waiting to be read by the external bus. When either the  $\overline{CS}$  or  $\overline{RD}$  pin becomes high (level triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware.

When not in Parallel Slave Port mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in firmware.

An interrupt is generated and latched into flag bit PSPIF when a read or write operation is completed. PSPIF must be cleared by the user in firmware and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).

#### FIGURE 5-11: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)



## 8.5 <u>Resetting Timer1 using a CCP Trigger</u> Output

## Applicable Devices

The CCP2 module is not implemented on the PIC16C72 device.

If the CCP1 or CCP2 module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1.

Note:	The special event triggers from the CCP1
	and CCP2 modules will not set interrupt
	flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL registers pair effectively becomes the period register for Timer1.

### 8.6 Resetting of Timer1 Register Pair (TMR1H, TMR1L) Applicable Devices 72|73|73A|74|74A|76|77

TMR1H and TMR1L registers are not reset to 00h on a POR or any other reset except by the CCP1 and CCP2 special event triggers.

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other resets, the register is unaffected.

#### 8.7 <u>Timer1 Prescaler</u> Applicable Devices

72 73 73A 74 74A 76 77

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1,2)</sup>	ADIF	RCIF <sup>(2)</sup>	TXIF <sup>(2)</sup>	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1,2)</sup>	ADIE	RCIE <sup>(2)</sup>	TXIE <sup>(2)</sup>	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								XXXX XXXX	uuuu uuuu
0Fh	TMR1H	Holding reg	lolding register for the Most Significant Byte of the 16-bit TMR1 register							xxxx xxxx	uuuu uuuu
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu

## TABLE 8-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A/76, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port or a USART, these bits are unimplemented, read as '0'.

#### 10.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

#### EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

CLRF	CCP1CON	;Turn CCP module off
MOVLW	NEW_CAPT_PS	;Load the W reg with
		; the new prescaler
		; mode value and CCP ON
MOVWF	CCP1CON	;Load CCP1CON with this
		; value

#### 10.2 <u>Compare Mode</u>

Applicable Devices

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- · Remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

#### FIGURE 10-3: COMPARE MODE OPERATION BLOCK DIAGRAM



#### 10.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note:	Clearing the CCP1CON register will force
	the RC2/CCP1 compare output latch to the
	default low level. This is not the data latch.

#### 10.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

#### 10.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

#### 10.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCP2 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

For the PIC16C72 only, the special event trigger output of CCP1 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

Note: The special event trigger from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

#### 11.4.2 ADDRESSING I<sup>2</sup>C DEVICES

There are two address formats. The simplest is the 7-bit address format with a  $R/\overline{W}$  bit (Figure 11-15). The more complex is the 10-bit address with a  $R/\overline{W}$  bit (Figure 11-16). For 10-bit address format, two bytes must be transmitted with the first five bits specifying this to be a 10-bit address.

#### FIGURE 11-15: 7-BIT ADDRESS FORMAT



### FIGURE 11-16: I<sup>2</sup>C 10-BIT ADDRESS FORMAT



#### 11.4.3 TRANSFER ACKNOWLEDGE

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit ( $\overline{ACK}$ ) (Figure 11-17). When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (Figure 11-14).

#### FIGURE 11-17: SLAVE-RECEIVER ACKNOWLEDGE



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level, Figure 11-18. The slave will inherently stretch the clock, when it is a transmitter, but will not when it is a receiver. The slave will have to clear the SSPCON<4> bit to enable clock stretching when it is a receiver.



#### FIGURE 11-18: DATA TRANSFER WAIT STATE

#### 11.4.4 MULTI-MASTER

The  $I^2C$  protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

#### 11.4.4.1 ARBITRATION

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure 11-22), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

#### FIGURE 11-22: MULTI-MASTER ARBITRATION (TWO MASTERS)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

#### 11.2.4.2 Clock Synchronization

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure 11-23.

#### FIGURE 11-23: CLOCK SYNCHRONIZATION





FIGURE 14-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



#### FIGURE 14-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)



# PIC16C7X

[ label ]	IORWF	f,d					
0 ≤ f ≤ 127 d ∈ [0,1]							
(W) .OR.	$(f) \rightarrow (de)$	estination	)				
Z							
00	0100	dfff	ffff				
Inclusive OR the W register with regis- ter 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.							
1							
1							
Q1	Q2	Q3	Q4				
Decode	Read register 'f'	Process data	Write to destination				
IORWF		RESULT,	0				
Before In	struction						
		= 0x13	}				
After Inst	ruction	- 0,01					
	RESULT	= 0x13	3				
	W	= 0x93	3				
	$[label] \\ 0 \le f \le 12 \\ d \in [0,1] \\ (W) .OR. \\ Z \\ 00 \\ Inclusive C \\ ter 'f'. If 'd' \\ W register \\ back in reg \\ 1 \\ 1 \\ Q1 \\ \hline Decode \\ IORWF \\ Before In \\ After Inst \\ \end{bmatrix}$	$\begin{bmatrix} label \end{bmatrix} \text{ IORWF} \\ 0 \leq f \leq 127 \\ d \in [0,1] \\ (W) .OR. (f) \rightarrow (de Z \\ \hline 00 & 0100 \\ \\ \text{Inclusive OR the W} \\ \text{ter 'f'. If 'd' is 0 the re W register. If 'd' is 1 \\ \text{back in register. If 'd' is 1 } \\ \text{back in register. If 'd' is 1 } \\ \text{back in register 'f'. } \\ 1 \\ 1 \\ Q1 & Q2 \\ \hline Decode & Read \\ register \\ 'f' \\ \hline IORWF \\ \hline Before Instruction \\ RESULT \\ W \\ After Instruction \\ RESULT \\ W \\ 7 \\ \end{bmatrix}$	$\begin{bmatrix} label \end{bmatrix} \text{ IORWF}  f,d \\ 0 \le f \le 127 \\ d \in [0,1] \\ (W) .OR. (f) → (destination Z \\ \hline 00 & 0100 & dfff \\ \text{Inclusive OR the W register witter 'f'. If 'd' is 0 the result is place W register. If 'd' is 1 the result back in register 'f'. \\ 1 \\ 1 \\ Q1 & Q2 & Q3 \\ \hline Decode & Read register 'f'. \\ IORWF & RESULT , \\ Before Instruction \\ RESULT = 0x13 \\ W & = 0x91 \\ After Instruction \\ RESULT = 0x13 \\ W & = 0x93 \\ Z & = 1 \\ \end{bmatrix}$				

MOVLW	Move Literal to W						
Syntax:	[ label ]	MOVLW	/ k				
Operands:	$0 \le k \le 2\xi$	55					
Operation:	$k \to (W)$						
Status Affected:	None						
Encoding:	11	00xx	kkkk	kkkk			
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read literal 'k'	Process data	Write to W			
Example	MOVLW After Inst	0x5A ruction					
		= W	0x5A				

MOVF	Move f							
Syntax:	[ label ]	MOVF	f,d					
Operands:	$0 \le f \le 127$ $d \in [0,1]$							
Operation:	$(f) \rightarrow (des$	stination	)					
Status Affected:	Z							
Encoding:	00	1000	dfff	ffff				
Description:	The contents of register f is moved to a destination dependant upon the status of d. If $d = 0$ , destination is W register. If $d = 1$ , the destination is file register f itself. $d = 1$ is useful to test a file register for since status flag Z is affected.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to destination				
Example	MOVF	FSR,	0					
	After Instruction W = value in FSR register Z = 1							

MOVWF	Move W	to f					
Syntax:	[ label ]	MOVW	= f				
Operands:	$0 \le f \le 12$	27					
Operation:	$(W) \rightarrow (f)$						
Status Affected:	None						
Encoding:	00	0000	lff	ffff			
Description:	Move data from W register to register						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Proces data	S Write register 'f'			
Example	MOVWF	OPTIC	N_REG				
	Before Instruction OPTION = 0xFF W = 0x4F						
	After Inst	ruction OPTION W	= 0x	(4F			

## Applicable Devices 72 73 73A 74 74A 76 77

## FIGURE 17-10: I<sup>2</sup>C BUS DATA TIMING



#### TABLE 17-9: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Мах	Units	Conditions
100	Тнідн	Clock high time	100 kHz mode	4.0	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5TCY	—		
102	Tr	SDA and SCL rise	100 kHz mode	_	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	—	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup	100 kHz mode	4.7	—	μs	
		time	400 kHz mode	0.6	—	μs	
109	ΤΑΑ	Output valid from	100 kHz mode		3500	ns	Note 1
		CIOCK	400 kHz mode	_	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3		μs	start
	Cb	Bus capacitive loading		-	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz)S I<sup>2</sup>C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

## Applicable Devices 72 73 73A 74 74A 76 77



#### TABLE 18-10: I<sup>2</sup>C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	Thigh	Clock high time	100 kHz mode	4.0	_	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	0.6	_	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a mini- mum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a mini- mum of 10 MHz
			SSP Module	1.5Tcy	—		
102	Tr	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition	100 kHz mode	4.7	—	μs	Only relevant for repeated
		setup time	400 kHz mode	0.6	—	μs	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	—	μs	After this period the first clock
		time	400 kHz mode	0.6	—	μs	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup	100 kHz mode	4.7		μs	
		time	400 kHz mode	0.6	—	μs	
109	ΤΑΑ	Output valid from	100 kHz mode		3500	ns	Note 1
		CIOCK	400 kHz mode		—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3		μs	start
	Cb	Bus capacitive loading		-	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I<sup>2</sup>C-bus device can be used in a standard-mode (100 kHz) I<sup>2</sup>C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C bus specification) before the SCL line is released.

## Applicable Devices 72 73 73A 74 74A 76 77

19.1 DC Characteristics: PIC16C73A/74A-04 (Commercial, Industrial, Extended) PIC16C73A/74A-10 (Commercial, Industrial, Extended) PIC16C73A/74A-20 (Commercial, Industrial, Extended)

DC CH	ARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}$ C $\leq$ TA $\leq$ +125 $^{\circ}$ C for extended,				
						-4 0°	$10^{\circ}C \le TA \le +85^{\circ}C$ for industrial and $C \le TA \le +70^{\circ}C$ for commercial
Param No.	Characteristic	Sym	Min	Тур†	Мах	Units	Conditions
D001 D001A	Supply Voltage	Vdd	4.0 4.5	-	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
			3.7	4.0	4.4	V	Extended Range Only
D010	Supply Current (Note 2,5)	IDD	-	2.7	5	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013			-	10	20	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D015*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled VDD = 5.0V
D020	Power-down Current	IPD	-	10.5	42	μA	$VDD = 4.0V$ , WDT enabled, $-40^{\circ}C$ to $+85^{\circ}C$
D021	(Note 3,5)		-	1.5	16	μΑ	VDD = $4.0V$ , WDT disabled, $-0^{\circ}C$ to $+70^{\circ}C$
D021A			-	2.5	19	μΑ	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023*	Brown-out Reset Current (Note 6)	$\Delta$ IBOR	-	350	425	μA	BOR enabled VDD = 5.0V

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

 $\overline{\text{MCLR}}$  = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

 Applicable Devices
 72
 73
 73A
 74
 74A
 76
 77

## FIGURE 19-10: I<sup>2</sup>C BUS START/STOP BITS TIMING



TABLE 19-9. I C DUS START/STUP DITS REQUIREMENT	TABLE 19-9:	I <sup>2</sup> C BUS START/STOP BITS REQUIREMENTS
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Parameter No.	Sym	Characteristic		Min	Тур	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START
		Setup time	400 kHz mode	600	_	—	113	condition
91	THD:STA	START condition	100 kHz mode	4000	—	—	ne	After this period the first clock
		Hold time	400 kHz mode	600	—	—	115	pulse is generated
92	Tsu:sto	STOP condition	100 kHz mode	4700	—	—	ne	
		Setup time	400 kHz mode	600	—	—	113	
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ne	
		Hold time	400 kHz mode	600	—	—	115	

# PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77

## 20.0 ELECTRICAL CHARACTERISTICS FOR PIC16C76/77

#### Absolute Maximum Ratings †

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR. and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	0.3 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	0 to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	
Maximum current into VDD pin	
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3)	
Maximum current sunk by PORTC and PORTD (combined) (Note 3)	
Maximum current sourced by PORTC and PORTD (combined) (Note 3)	
<b>Note 1:</b> Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VDD - VA)	OH) X IOH} + $\Sigma$ (VOI X IOL)
Note 2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, n	nay cause latch-up. Thus,

**lote 2:** Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. I hus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to VSS.

Note 3: PORTD and PORTE are not implemented on the PIC16C76.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## Applicable Devices 72 73 73A 74 74A 76 77

## 20.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2	ppS	3. TCC:ST	(I <sup>2</sup> C specifications only)
2. TppS		4. Ts	(I <sup>2</sup> C specifications only)
Т			
F	Frequency	Т	Time
Lower	case letters (pp) and their meanings:		
рр			
сс	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	TOCKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Upper	case letters and their meanings:		
S			
F	Fall	P	Period
H	High	R	Rise
	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I <sup>2</sup> C only			
AA	output access	High	High
BUF	Bus free	Low	Low
Tcc:st	(I <sup>2</sup> C specifications only)	_	
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		
FIGURE	20-1: LOAD CONDITIONS		
			Logd condition 2
	Load condition 1		Load condition 2
	VDD/2		
	Pin	P	
	Vss		▼ Vss
	$R_{1} = 464\Omega$		
	$C_1 = 50 \text{ pc}$ for all pipe avaant $OSO2$ but inc		
	ports		
	15 pF for OSC2 output		
	Note: PORTD and PORTE are not implemented	d on the PIC1	6C76.

## Applicable Devices 72 73 73A 74 74A 76 77

## 21.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

**Note:** The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean  $+3\sigma$ ) and (mean  $-3\sigma$ ) respectively where  $\sigma$  is standard deviation.

FIGURE 21-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)



FIGURE 21-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)



## 22.3 28-Lead Plastic Dual In-line (300 mil) (SP)



Package Group: Plastic Dual In-Line (PLA)						
		Millimeters			Inches	
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
Α	3.632	4.572		0.143	0.180	
A1	0.381	_		0.015	_	
A2	3.175	3.556		0.125	0.140	
В	0.406	0.559		0.016	0.022	
B1	1.016	1.651	Typical	0.040	0.065	Typical
B2	0.762	1.016	4 places	0.030	0.040	4 places
B3	0.203	0.508	4 places	0.008	0.020	4 places
С	0.203	0.331	Typical	0.008	0.013	Typical
D	34.163	35.179		1.385	1.395	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	7.874	8.382		0.310	0.330	
E1	7.112	7.493		0.280	0.295	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.874	7.874	Reference	0.310	0.310	Reference
eB	8.128	9.652		0.320	0.380	
L	3.175	3.683		0.125	0.145	
N	28	-		28	-	
S	0.584	1.220		0.023	0.048	

#### Package Marking Information (Cont'd)

44-Lead TQFP



Example



Legend:	MMM XXX AA BB C	Microchip part number information Customer specific information* Year code (last 2 digits of calender year) Week code (week of January 1 is week '01') Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.
	D <sub>1</sub> E	Mask revision number for microcontroller Assembly code of the plant or country of origin in which
	—	part was assembled.
Note:	In the eve line, it will available	nt the full Microchip part number cannot be marked on one be carried over to the next line thus limiting the number of characters for customer specific information.

\* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

#### E.3 PIC16C15X Family of Devices

		PIC16C154	PIC16CR154	PIC16C156	PIC16CR156	PIC16C158	PIC16CR158
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x12 words)	512		1K	—	2К	—
Memory	ROM Program Memory (x12 words)	—	512	_	1K		2К
	RAM Data Memory (bytes)	25	25	25	25	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	12	12	12
	Voltage Range (Volts)	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5
Features	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC; 20-pin SSOP					

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

### E.4 PIC16C5X Family of Devices

		PIC16C52	PIC16C54	PIC16C54A	PIC16CR54A	PIC16C55	PIC16C56
Clock	Maximum Frequency of Operation (MHz)	4	20	20	20	20	20
	EPROM Program Memory (x12 words)	384	512	512	—	512	1K
Memory	ROM Program Memory (x12 words)	—	—	—	512	—	—
	RAM Data Memory (bytes)	25	25	25	25	24	25
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	12	20	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.0-6.25	2.5-6.25	2.5-6.25
Features	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP

		PIC16C57	PIC16CR57B	PIC16C58A	PIC16CR58A
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20
	EPROM Program Memory (x12 words)	2К	_	2K	_
Memory	ROM Program Memory (x12 words)	_	2K	_	2K
	RAM Data Memory (bytes)	72	72	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	I/O Pins	20	20	12	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.5-6.25
Features	Number of Instructions	33	33	33	33
	Packages	28-pin DIP, SOIC, SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

## PIC16C7X

Registers
FSR Summary 20
INDF
Summary
INTCON Summary 29
Maps
PIC16C72
PIC16C73A 21
PIC16C74
PIC16C74A
PIC16C7622
PIC16C7722
OPTION
Summary28
Summary
PCLATH
Summary29
PORTB
Summary
Reset Conditions
Section 80
SSPCON
Diagram79
SSPSR
Section80
SSPSTAT83
Diagram
Section
Summary 20
Summary
TMRO
Summary28
Summary 29
Reset
Reset Conditions for Special Registers
RP0 bit
RP1 bit
RX9 DIT
RA9D bit
S
SDI
SDO
Serial Communication Interface (SCI) Module, See USART
Services
One-Time-Programmable (OTP)7
Quick-Turnaround-Production (QTP)
Serialized Quick-Turnaround Production (SQTP) /
SCI
SDA
SLEEP
SMP
Software Simulator (MPSIM) 165
SPBRG

SPBRC Register	26 28
Or biol Register	
Special Event Trigger	125
Special Features of the CPU	129
Special Function Registers	
PIC16C72	23
PIC16C73	25, 27
PIC16C73A	25 27
	25 27
PIC10074	
PIC16C74A	
PIC16C76	27
PIC16C77	27
Special Function Registers, Section	23
SPEN bit	100
SDI	
Dia de Dia marte	00.05
BIOCK Diagram	80, 85
Master Mode	86
Master Mode Timing	87
Mode	80
Serial Clock	
Serial Data In	85
Sorial Data Out	
Slave Mode Timing	88
Slave Mode Timing Diagram	87
Slave Select	85
SPI clock	86
SPI Mode	85
SEDCON	
55P51A1	83
SPI Clock Edge Select bit, CKE	83
SPI Data Input Sample Phase Select bit, SMP	83
SPI Mode	80
SREN bit	100
	00
66D	
SSP	
SSP Module Overview	77
SSP Module Overview Section	77 77
SSP Module Overview Section SSPBUF	77 77 86
SSP Module Overview Section SSPBUF SSPCON	77 77 86 84
SSP Module Overview Section SSPBUF SSPCON SSPSR	77 77 86 84 86
SSP Module Overview Section SSPBUF SSPCON SSPSR	77 77 
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT	77 
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register SSPBUF SSPBUF Register SSPCON SSPCON Register SSPCON Register SSPCO	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register SSPADD Register SSPBUF Register SSPCON SSPCON Register SSPCON Register SSPCON Register SSPEN SSPIE bit	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD SSPADD Register SSPBUF Register SSPBUF Register SSPCON Register SSPCON Register SSPCON Register SSPEN SSPEN SSPIE bit SSPIF bit	
SSP Module Overview Section SSPBUF SSPCON SSPSR SSPSTAT SSP in I <sup>2</sup> C Mode - See I <sup>2</sup> C SSPADD Register SSPADD Register SSPBUF Register SSPBUF Register SSPCON Register SSPCON Register SSPEN SSPIE bit SSPIF bit SSPM3:SSPM0 SSPOV	
SSP Module Overview	