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Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc74at-04-pt

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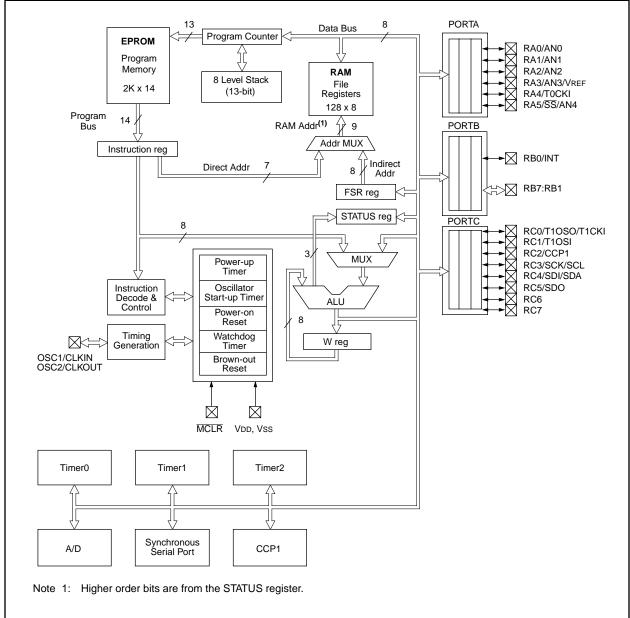
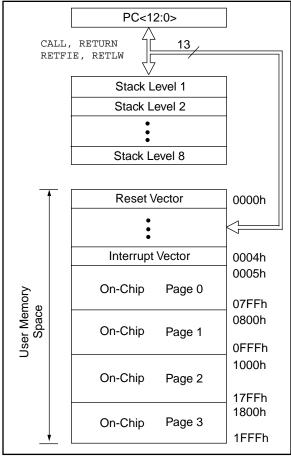


FIGURE 4-3: PIC16C76/77 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Applicable Devices 72 73 73 74 74 76 77

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1:RP0 (STATUS<6:5>)

- = 00 \rightarrow Bank0
- = 01 \rightarrow Bank1
- = $10 \rightarrow \text{Bank2}$
- = 11 \rightarrow Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some "high use" special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (3)
Bank 1	•	•			•	•		•	•		·
80h ⁽¹⁾	INDF	Addressing	Addressing this location uses contents of FSR to address data memory (not a physical register)						register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect data	a memory ad	dress pointe	er					xxxx xxxx	uuuu uuuu
85h	TRISA	_	—	PORTA Dat	ta Direction F	Register				11 1111	11 1111
86h	TRISB	PORTB Dat	ta Direction F	Register						1111 1111	1111 1111
87h	TRISC	PORTC Da	ta Direction F	Register						1111 1111	1111 1111
88h	_	Unimpleme	nted							-	_
89h	-	Unimpleme	nted							-	-
8Ah ^(1,2)	PCLATH	—	—	—	Write Buffe	for the uppe	er 5 bits of th	e PC		0 0000	0 0000
8Bh (1)	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	—	ADIE	—	_	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	-0 0000
8Dh	—	Unimpleme	nted							—	—
8Eh	PCON	—	—	—	_	—	—	POR	BOR	dd	uu
8Fh	—	Unimpleme	nted							—	—
90h	_	Unimpleme	nted							_	—
91h	_	Unimpleme	nted							_	—
92h	PR2	Timer2 Peri	od Register							1111 1111	1111 1111
93h	SSPADD	Synchronou	us Serial Port	(I ² C mode)	Address Re	gister				0000 0000	0000 0000
94h	SSPSTAT	—	—	D/Ā	Р	S	R/W	UA	BF	00 0000	00 0000
95h	—	Unimpleme	nted							—	—
96h	_	Unimpleme	nted							_	_
97h	_	Unimpleme	nted							_	_
98h	—	Unimpleme	Unimplemented							—	—
99h	—	Unimpleme	Unimplemented							—	—
9Ah	_	Unimpleme	Unimplemented							_	—
9Bh	—	Unimpleme	nted							—	—
9Ch	_	Unimpleme	nted							-	—
9Dh	—	Unimpleme	nted							—	—
9Eh	—	Unimpleme	nted							_	_
9Fh	ADCON1	—	-	—	-	_	PCFG2	PCFG1	PCFG0	000	000

TABLE 4-1: PIC16C72 SPECIAL FUNCTION REGISTER SUMMARY (Cont.'d)

 $\label{eq:legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.$

Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C72, always maintain these bits clear.

11.3 SPI Mode for PIC16C76/77

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This section contains register definitions and operational characteristics of the SPI module on the PIC16C76 and PIC16C77 only.

FIGURE 11-7: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)(PIC16C76/77)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0		
SMP	CKE	D/Ā	Р	S	R/W	UA	BF	R = Readable bit	
bit7							bit0	W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset	
bit 7:	SMP: SPI data input sample phase <u>SPI Master Mode</u> 1 = Input data sampled at end of data output time 0 = Input data sampled at middle of data output time <u>SPI Slave Mode</u> SMP must be cleared when SPI is used in slave mode								
bit 6:	CKE : SPI Clock Edge Select (Figure 11-11, Figure 11-12, and Figure 11-13) $\frac{CKP = 0}{1 = Data transmitted on rising edge of SCK}$ $0 = Data transmitted on falling edge of SCK$ $\frac{CKP = 1}{1 = Data transmitted on falling edge of SCK}$ $0 = Data transmitted on falling edge of SCK$								
bit 5:	1 = Indi	cates tha	t the last b) ed or transmi ed or transmi				
bit 4:	detecte 1 = Indi	d last, SS cates tha	SPEN is cl	eared) t has been	cleared whe			lisabled, or when the Start bit is	
bit 3:	detecte 1 = Indi	d last, SS cates tha	SPEN is cl	eared) t has been	cleared whe			lisabled, or when the Stop bit is	
bit 2:	R/W : Read/Write bit information (I ² C mode only) This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or ACK bit. 1 = Read 0 = Write								
bit 1:	1 = Indi	cates tha	t the user	it I ² C mode needs to u I to be upda	pdate the ad	dress in the	e SSPADD re	egister	
bit 0:	BF: Buf	fer Full S	tatus bit						
	1 = Rec 0 = Rec	eive com eive not	complete,	es) PBUF is ful SSPBUF is					
	1 = Trar		rogress, S	SPBUF is t PBUF is en					

Figure 11-19 and Figure 11-20 show Master-transmitter and Master-receiver data transfer sequences.

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while

SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 11-21.

FIGURE 11-19: MASTER-TRANSMITTER SEQUENCE

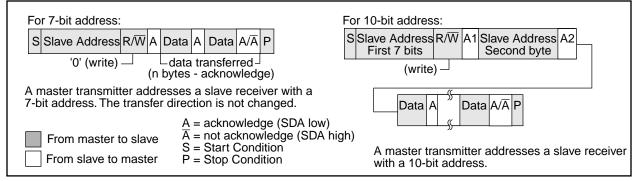
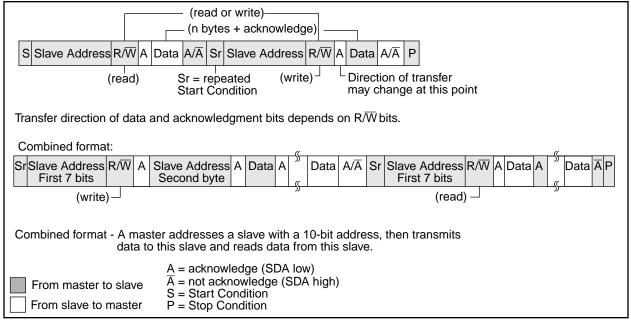


FIGURE 11-20: MASTER-RECEIVER SEQUENCE

For 7-bit address:	Fc	or 10-bit address:				
S Slave Address R/W A D	ata A Data A P S	Slave Address R/W A1 Slave Address A2 First 7 bits Second byte				
	data transferred- rtes - acknowledge)	(write)				
A master reads a slave imm	ediately after the first byte.					
From master to slave	$\begin{array}{l} A = acknowledge (SDA low) \\ \overline{A} = not acknowledge (SDA high) \\ S = Start Condition \\ P = Stop Condition \end{array}$	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $				

FIGURE 11-21: COMBINED FORMAT



12.1 USART Baud Rate Generator (BRG) Applicable Devices 72 73 73A 74 74A 76 77

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table 12-1 shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 12-1. From this, the error in baud rate can be determined.

Example 12-1 shows the calculation of the baud rate error for the following conditions:

Fosc = 16 MHz Desired Baud Rate = 9600 BRGH = 0 SYNC = 0

EXAMPLE 12-1: CALCULATING BAUD RATE ERROR

Desired Baud rate = Fosc / (64 (X + 1))

 $9600 = \frac{16000000}{(64 (X + 1))}$

 $X = \lfloor 25.042 \rfloor = 25$

Calculated Baud Rate=16000000 / (64 (25 + 1))

= 9615

- Error = (Calculated Baud Rate Desired Baud Rate) Desired Baud Rate
 - = (9615 9600) / 9600

= 0.16%

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the Fosc/(16(X + 1)) equation can reduce the baud rate error in some cases.

Note:	For the PIC16C73/73A/74/74A, the asyn- chronous high speed mode (BRGH = 1) may experience a high rate of receive errors. It is recommended that BRGH = 0. If you desire a higher baud rate than BRGH = 0 can support, refer to the device errata for additional information, or use the PIC16C76/77.
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Writing a new value to the SPBRG register, causes the BRG timer to be reset (or cleared), this ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

TABLE 12-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate= Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	NA

X = value in SPBRG (0 to 255)

TABLE 12-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
99h SPBRG Baud Rate Generator Register							0000 0000	0000 0000			

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used by the BRG.

13.2 <u>Selecting the A/D Conversion Clock</u> Applicable Devices

72 73 73A 74 74A 76 77

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5TAD per 8-bit conversion. The source of the A/D conversion clock is software selectable. The four possible options for TAD are:

- 2Tosc
- 8Tosc
- 32Tosc
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 $\mu s.$

Table 13-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

13.3 Configuring Analog Port Pins Applicable Devices 72/73/73A/74/74A/76/77

The ADCON1, TRISA, and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

- Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.
- **Note 2:** Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

AD Cloc	k Source (TAD)	Device Frequency					
Operation	ADCS1:ADCS0	20 MHz	5 MHz	1.25 MHz	333.33 kHz		
2Tosc	00	100 ns ⁽²⁾	400 ns ⁽²⁾	1.6 μs	6 μs		
8Tosc	01	400 ns ⁽²⁾	1.6 μs	6.4 μs	24 μs ⁽³⁾		
32Tosc	10	1.6 μs	6.4 μs	25.6 μs ⁽³⁾	96 μs ⁽³⁾		
RC ⁽⁵⁾	11	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ^(1,4)	2 - 6 μs ⁽¹⁾		

TABLE 13-1: TAD vs. DEVICE OPERATING FREQUENCIES

Legend: Shaded cells are outside of recommended range.

- 2: These values violate the minimum required TAD time.
- 3: For faster conversion times, the selection of another clock source is recommended.
- 4: When device frequency is greater than 1 MHz, the RC A/D conversion clock source is recommended for sleep operation only.
- 5: For extended voltage devices (LC), please refer to Electrical Specifications section.

Note 1: The RC source has a typical TAD time of 4 μ s.

13.4.1 FASTER CONVERSION - LOWER RESOLUTION TRADE-OFF

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the TAD time violates the minimum specified time (see the applicable electrical specification). Once the TAD time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section.) The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

Conversion time = $2TAD + N \cdot TAD + (8 - N)(2TOSC)$ Where: N = number of bits of resolution required. Since the TAD is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D oscillator may be changed. Example 13-3 shows a comparison of time required for a conversion with 4-bits of resolution, versus the 8-bit resolution conversion. The example is for devices operating at 20 MHz and 16 MHz (The A/D clock is programmed for 32Tosc), and assumes that immediately after 6TAD, the A/D clock is programmed for 2Tosc.

The 2TOSC violates the minimum TAD time since the last 4-bits will not be converted to correct values.

EXAMPLE 13-3:	4-BIT vs. 8-BIT CON	/ERSION TIMES

	- (1)	Resolution		
	Freq. (MHz) ⁽¹⁾	4-bit	8-bit	
TAD	20	1.6 μs	1.6 μs	
	16	2.0 μs	2.0 μs	
Tosc	20	50 ns	50 ns	
	16	62.5 ns	62.5 ns	
2TAD + N • TAD + (8 - N)(2TOSC)	20	10 μs	16 μs	
	16	12.5 μs	20 µs	

Note 1: PIC16C7X devices have a minimum TAD time of 1.6 µs.

14.2 Oscillator Configurations Applicable Devices 72/73/73A/74/74A/76/77

14.2.1 OSCILLATOR TYPES

The PIC16CXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor
- 14.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 14-3). The PIC16CXX Oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/ CLKIN pin (Figure 14-4).

FIGURE 14-3: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)

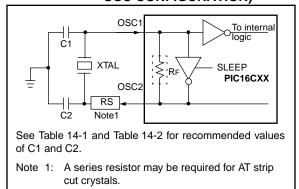


FIGURE 14-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

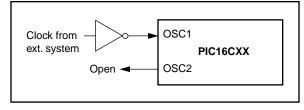


TABLE 14-1: CERAMIC RESONATORS

Ranges Tested:						
Mode	Freq	OSC2				
XT	455 kHz	68 - 100 pF	68 - 100 pF			
	2.0 MHz	15 - 68 pF	15 - 68 pF			
	4.0 MHz	15 - 68 pF	15 - 68 pF			
HS	8.0 MHz	10 - 68 pF	10 - 68 pF			
	16.0 MHz	10 - 22 pF	10 - 22 pF			
	These values are for design guidance only. See notes at bottom of page.					
Resonato	rs Used:					
455 kHz	Panasonic E	FO-A455K04B	± 0.3%			
2.0 MHz	Murata Erie	CSA2.00MG	± 0.5%			
4.0 MHz	Murata Erie CSA4.00MG ± 0.5%					
8.0 MHz	Murata Erie CSA8.00MT ± 0.5%					
16.0 MHz	Murata Erie	CSA16.00MX	± 0.5%			
All reso	onators used did	d not have built-in	capacitors.			

TABLE 14-2:CAPACITOR SELECTION
FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

These values are for design guidance only. See notes at bottom of page.

Crystals Used								
32 kHz	Epson C-001R32.768K-A	\pm 20 PPM						
200 kHz	STD XTL 200.000KHz	± 20 PPM						
1 MHz	ECS ECS-10-13-1	\pm 50 PPM						
4 MHz	ECS ECS-40-20-1	\pm 50 PPM						
8 MHz	EPSON CA-301 8.000M-C	\pm 30 PPM						
20 MHz	EPSON CA-301 20.000M-C	\pm 30 PPM						

Note 1: Recommended values of C1 and C2 are identical to the ranges tested (Table 14-1).

- 2: Higher capacitance increases the stability of oscillator but also increases the start-up time.
- 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

PIC16C7X

Register	Applicable Devices					es		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
SSPADD	72	73	73A	74	74A	76	77	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	72	73	73A	74	74A	76	77	00 0000	00 0000	uu uuuu
TXSTA	72	73	73A	74	74A	76	77	0000 -010	0000 -010	uuuu -uuu
SPBRG	72	73	73A	74	74A	76	77	0000 0000	0000 0000	uuuu uuuu
ADCON1	72	73	73A	74	74A	76	77	000	000	uuu

TABLE 14-8: INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 14-7 for reset value for specific condition.

14.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 14.8 for details on SLEEP mode.

14.5.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 7.0)

14.5.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 5.2)

Note:	For the PIC16C73/74, if a change on the
	I/O pin should occur when the read opera-
	tion is being executed (start of the Q2
	cycle), then the RBIF interrupt flag may not
	get set.

14.6 <u>Context Saving During Interrupts</u> Applicable Devices

72 73 73A 74 74A 76 77

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 14-1 stores and restores the STATUS, W, and PCLATH registers. The register, W_TEMP, must be defined in each bank and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1).

The example:

- a) Stores the W register.
- b) Stores the STATUS register in bank 0.
- c) Stores the PCLATH register.
- d) Executes the ISR code.
- e) Restores the STATUS register (and bank select bit).
- f) Restores the W and PCLATH registers.

EXAMPLE 14-1: SAVING STATUS, W, AND PCLATH REGISTERS IN RAM

MOVWF SWAPF CLRF	W_TEMP STATUS,W STATUS	;Copy W to TEMP register, could be bank one or zero ;Swap status to be saved into W ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF	STATUS_TEMP	;Save status to bank zero STATUS_TEMP register
MOVF	PCLATH, W	;Only required if using pages 1, 2 and/or 3
MOVWF	PCLATH_TEMP	;Save PCLATH into W
CLRF	PCLATH	;Page zero, regardless of current page
BCF	STATUS, IRP	;Return to Bank 0
MOVF	FSR, W	;Copy FSR to W
MOVWF	FSR_TEMP	;Copy FSR from W to FSR_TEMP
:		
:(ISR)		
:		
MOVF	PCLATH_TEMP, W	;Restore PCLATH
MOVWF	PCLATH	;Move W into PCLATH
SWAPF	STATUS_TEMP,W	;Swap STATUS_TEMP register into W
		;(sets bank to original state)
MOVWF	STATUS	;Move W into STATUS register
SWAPF	W_TEMP,F	;Swap W_TEMP
SWAPF	W_TEMP,W	;Swap W_TEMP into W

PIC16C7X

CLRF	Clear f									
Syntax:	[label] CLRF f									
Operands:	$0 \le f \le 127$									
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$								
Status Affected:	Z									
Encoding:	00	0001	lfff	ffff						
Description:	The contents of register 'f' are cleared and the Z bit is set.									
Words:	1									
Cycles:	1									
Q Cycle Activity:	Q1	Q2	Q3	Q4						
	Decode	Read register 'f'	Process data	Write register 'f'						
Example	CLRF FLAG_REG									
	Before Instruction									
	FLAG_REG = 0x5A After Instruction									
		FLAG RE	EG =	0x00						
		Ζ	=	1						

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Encoding:	00 0001 0xxx xxxx
Description:	W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Q Cycle Activity:	Q1 Q2 Q3 Q4
	Decode No- Operation Process Write to W
Example	CLRW
	Before Instruction
	W = 0x5A
	After Instruction W = 0x00
	Z = 1
CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
-	None $00h \rightarrow WDT$
Operands:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler,
Operands:	None $00h \rightarrow WDT$
Operands:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$
Operands: Operation:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$
Operands: Operation: Status Affected:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$
Operands: Operation: Status Affected: Encoding:	None $00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ OU 0000 0110 0100 CLRWDT instruction resets the Watch- dog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are
Operands: Operation: Status Affected: Encoding: Description:	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ CLRWDT instruction resets the Watch- dog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.
Operands: Operation: Status Affected: Encoding: Description: Words:	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ OO 0000 0110 0100 CLRWDT instruction resets the Watch- dog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set. 1
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	None $00h \rightarrow WDT$ $0 \rightarrow WDT prescaler,$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ $Oldsymbol{ODD} Ollolololololololololololololololololol$
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \\ \hline \overline{TO}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watch-dog Timer. It also resets the vacch-dog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set. 1 1 2 2 2 2 3 2 4 2 2 2 3 2 4 2 2 2 3 2 4 2 2 3 2 4 2 2 3 2 4 2 2 3 3 4 3 3 3 4 3 3 3 4 3 3 5 5 5 5 5 5 5
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \\ \hline \overline{TO}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watch-dog Timer. It also resets the Vatch-dog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set. 1 1 2 2 2 2 2 2 2 2 3 2 4 2 2 2 2 3 2 4 2 2 2 2 3 2 4 2 2 2 3 2 4 2 2 2 3 2 4 2 2 2 3 2 4 2 2 2 2 3 2 4 2 2 2 2 2 3 2 4 2 2 2 2 2 2 2 2 2 2 2 2 2
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \\ \hline \overline{TO}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \end{array}$ CLRWDT instruction resets the Watch-dog Timer. It also resets the vacch-dog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set. 1 1 2 2 2 2 3 2 4 2 2 2 3 2 4 2 2 2 3 2 4 2 2 3 2 4 2 2 3 2 4 2 2 3 3 4 3 3 3 4 3 3 3 4 3 3 5 5 5 5 5 5 5
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{T0} \\ 1 \rightarrow \overline{PD} \\ \hline \overline{T0}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline CLRWDT \ instruction \ resets \ the \ Watch-dog \ Timer. \ It \ also \ resets \ the \ prescaler \ of \ the \ WDT \ instruction \ resets \ the \ prescaler \ of \ the \ WDT. \ Status \ bits \ \overline{T0} \ and \ \overline{PD} \ are \ set. \\ \hline 1 \\ 1 \\ \hline 1 \\ \hline Q1 Q2 Q3 Q4 \\ \hline \hline Decode \hline No- \ Operation \ Process \ Clear \ WDT \ Counter \\ \hline CLRWDT \\ \hline Before \ Instruction \\ \hline WDT \ counter \ = \ ? \\ After \ Instruction \\ \hline \end{array}$
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	None $\begin{array}{l} \text{None} \\ \text{O0h} \rightarrow \text{WDT} \\ \text{O} \rightarrow \text{WDT prescaler}, \\ 1 \rightarrow \overline{\text{TO}} \\ 1 \rightarrow \overline{\text{PD}} \\ \hline \overline{\text{TO}}, \overline{\text{PD}} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \\ \hline \text{CLRWDT instruction resets the Watch-dog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set. \\ 1 \\ 1 \\ \hline \\ Q1 & Q2 & Q3 & Q4 \\ \hline \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ CLRWDT \\ \hline \\ CLRWDT \\ \hline \\ CLRWDT \\ \hline \\ Before Instruction \\ \hline \\ WDT counter = ? \\ \end{array}$
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	None $\begin{array}{c} 00h \rightarrow WDT \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \\ \hline \overline{TO}, \overline{PD} \\ \hline \hline 00 & 0000 & 0110 & 0100 \\ \hline \\ CLRWDT \ instruction \ resets \ the \ Watch-dog \ Timer. It also \ resets \ the \ Watch-dog \ Timer. It also \ resets \ the \ prescaler \ of \ the \ WDT. \ Status \ bits \ \overline{TO} \ and \ \overline{PD} \ are \ set. \\ \hline 1 \\ 1 \\ \hline \\ \hline \\ Q1 & Q2 & Q3 & Q4 \\ \hline \hline \\ \hline \\ \hline \\ CLRWDT \\ \hline \\ CLRWDT \\ \hline \\ CLRWDT \\ \hline \\ Before \ Instruction \\ \qquad WDT \ counter \ = \ ? \\ After \ Instruction \\ \qquad WDT \ counter \ = \ 0x00 \\ \hline \end{array}$

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17.2 DC Characteristics: PIC16LC72-04 (Commercial, Industrial)

DC CHA	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C$ $\leq TA \leq +85^{\circ}C$ for industrial and $0^{\circ}C$ $\leq TA \leq +70^{\circ}C$ for commercial									
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions			
D001	Supply Voltage	Vdd	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)			
D002*	RAM Data Retention Volt- age (Note 1)	Vdr	-	1.5	-	V				
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details			
D004*	VDD rise rate to ensure internal Power-on Reset signal	Svdd	0.05	-	-	V/ms	See section on Power-on Reset for details			
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN bit in configuration word enabled			
D010	Supply Current (Note 2,5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)			
D010A			-	22.5	48	μA	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled			
D015*	Brown-out Reset Current (Note 6)	Δ IBOR	-	350	425	μA	BOR enabled VDD = 5.0V			
D020 D021 D021A	Power-down Current (Note 3,5)	IPD	- - -	7.5 0.9 0.9	30 5 5	μΑ μΑ μΑ	$\label{eq:VDD} \begin{array}{l} \text{VDD} = 3.0\text{V}, \text{WDT enabled}, -40^{\circ}\text{C to} +85^{\circ}\text{C} \\ \text{VDD} = 3.0\text{V}, \text{WDT disabled}, 0^{\circ}\text{C to} +70^{\circ}\text{C} \\ \text{VDD} = 3.0\text{V}, \text{WDT disabled}, -40^{\circ}\text{C to} +85^{\circ}\text{C} \end{array}$			
D023*	Brown-out Reset Current (Note 6)	Δ IBOR	-	350	425	μA	BOR enabled VDD = 5.0V			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

 The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption. The test conditions for all IDD measurements in active operation mode are:

 $OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD <math>\overline{MCLR} = VDD; WDT$ enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

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18.5 <u>Timing Diagrams and Specifications</u>

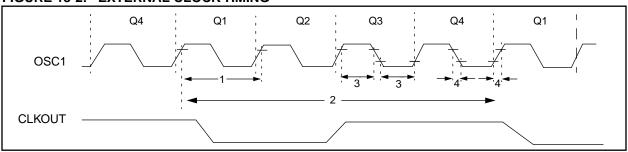


FIGURE 18-2: EXTERNAL CLOCK TIMING

TABLE 18-2: EXTERNAL CLOCK TIMING REQUIREMENTS

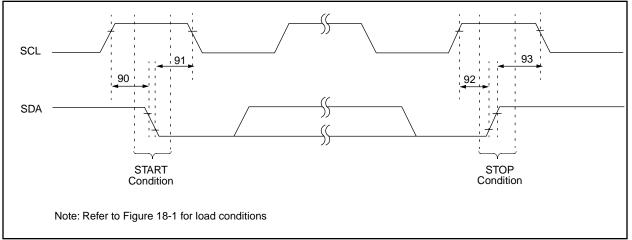
Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT and RC osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	10	MHz	HS osc mode (-10)
			DC	_	20	MHz	HS osc mode (-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode
		(Note 1)	0.1	_	4	MHz	XT osc mode
			4	_	20	MHz	HS osc mode
			5	_	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	_	—	ns	XT and RC osc mode
		(Note 1)	250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	_	μs	LP osc mode
		Oscillator Period	250	_	—	ns	RC osc mode
		(Note 1)	250	_	10,000	ns	XT osc mode
			250	_	250	ns	HS osc mode (-04)
			100	_	250	ns	HS osc mode (-10)
			50	—	250	ns	HS osc mode (-20)
			5	_	—	μs	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	200	_	DC	ns	TCY = 4/FOSC
3	TosL,	External Clock in (OSC1) High or	50	_	—	ns	XT oscillator
	TosH	Low Time	2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise or	_	_	25	ns	XT oscillator
	TosF	Fall Time	_	_	50	ns	LP oscillator
			_	_	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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FIGURE 18-9: I²C BUS START/STOP BITS TIMING



Parameter No.	Sym	Characteristic		Min	Тур	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	_	_	ns	Only relevant for repeated START
		Setup time	400 kHz mode	600		—	113	condition
91	THD:STA	START condition	100 kHz mode	4000		—	ns	After this period the first clock
		Hold time	400 kHz mode	600	—	—	115	pulse is generated
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—	115	
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—	113	

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FIGURE 20-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

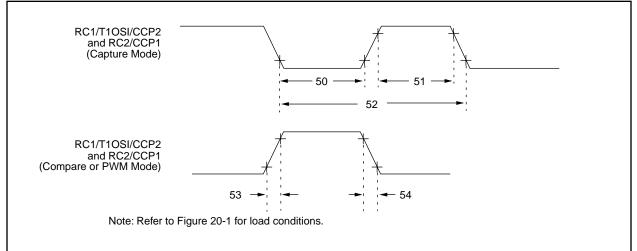


TABLE 20-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Sym	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 and CCP2	No Prescaler	No Prescaler		—		ns	
	input low tir	input low time		PIC16 C 76/77	10	_	_	ns	
			With Prescaler	PIC16 LC 76/77	20	—	-	ns	
51*	51* TccH CCP1 and CCP2		No Prescaler		0.5TCY + 20			ns	
	input high time		PIC16 C 76/77	10	—		ns		
			With Prescaler	PIC16 LC 76/77	20	—	—	ns	
52*	TccP	CCP1 and CCP2 i	CCP1 and CCP2 input period				_	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP1 and CCP2 of	output rise time	PIC16 C 76/77	-	10	25	ns	
				PIC16 LC 76/77	_	25	45	ns	
54*	TccF	CCP1 and CCP2 output fall time		PIC16 C 76/77	_	10	25	ns	
				PIC16 LC 76/77	_	25	45	ns	

* These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

t

Applicable Devices 72 73 73 74 74 76 77 FIGURE 21-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

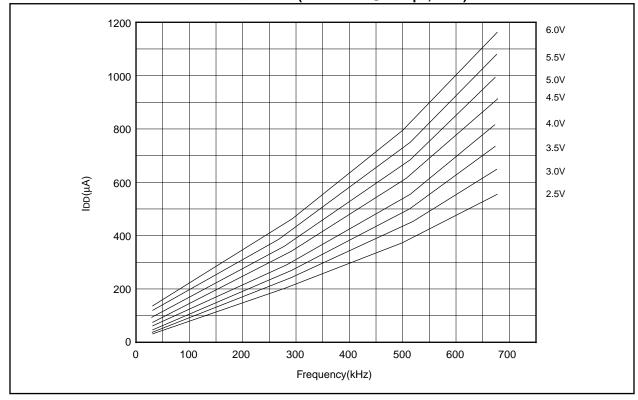
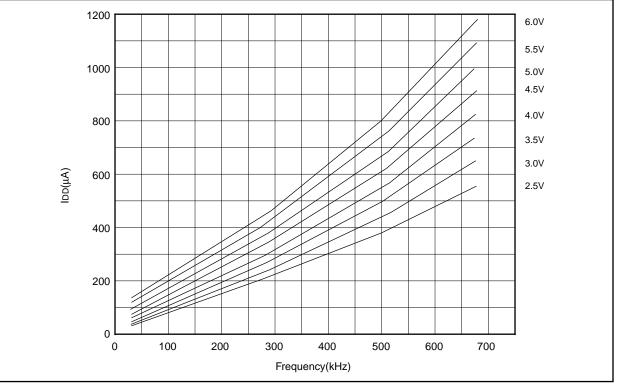
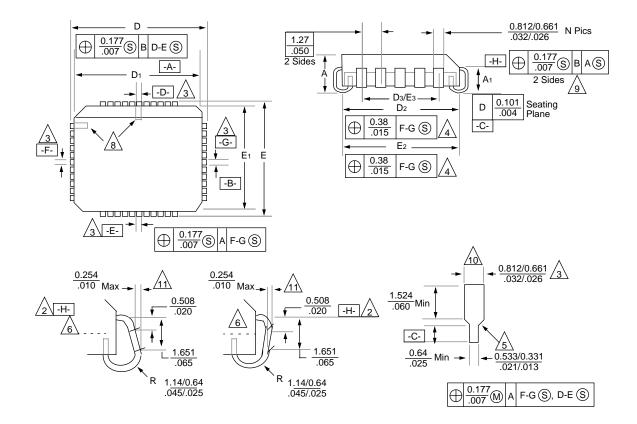


FIGURE 21-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

22.7 44-Lead Plastic Leaded Chip Carrier (Square)(PLCC)



	Package Group: Plastic Leaded Chip Carrier (PLCC)										
		Millimeters		Inches							
Symbol	Min	Max	Notes	Min	Max	Notes					
А	4.191	4.572		0.165	0.180						
A1	2.413	2.921		0.095	0.115						
D	17.399	17.653		0.685	0.695						
D1	16.510	16.663		0.650	0.656						
D2	15.494	16.002		0.610	0.630						
D3	12.700	12.700	Reference	0.500	0.500	Reference					
E	17.399	17.653		0.685	0.695						
E1	16.510	16.663		0.650	0.656						
E2	15.494	16.002		0.610	0.630						
E3	12.700	12.700	Reference	0.500	0.500	Reference					
Ν	44	44		44	44						
CP	-	0.102		_	0.004						
LT	0.203	0.381		0.008	0.015						

Synchronous Serial Port Mode Select bits	
SSPM3:SSPM0	79, 84
Synchronous Serial Port Module	
Synchronous Serial Port Status Register	
т	
TOCS bit	
T1CKPS0 bit	
T1CKPS1 bit	
T1CON	
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I ² C Data Transfer Wait State			
I ² C Multi-Master Arbitration			
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Reset			
SPI Master Mode			
SPI Mode SPI Mode, Master/Slave Mode, No			
SPI Mode, Slave Mode With SS Co			
SPI Slave Mode (CKE = 1)			
SPI Slave Mode Timing (CKE = 0)			
Start-up Timer			
Time-out Sequence			
Timer0			
Timer0 Interrupt Timing			
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USART Synchronous Receive		198, 2	216, 237
USART Synchronous Reception			113
USART Synchronous Transmission			
Wake-up from Sleep via Interrupt			
Watchdog Timer			
TMR0			
TMR0 Register			,
TMR1CS bit			65
TMR1H			29
TMR1H Register		23	29 3, 25, 27
TMR1H Register TMR1IE bit		23	29 3, 25, 27 33
TMR1H Register TMR1IE bit TMR1IF bit		2:	
TMR1H Register TMR1IE bit TMR1IF bit TMR1IF bit		2:	29 3, 25, 27 33 35, 36 29
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register		2:	29 3, 25, 27 33 35, 36 29 3, 25, 27
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit		2:	
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit TMR2		2:	
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit TMR2 TMR2 Register		2:	
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit TMR2 TMR2 Register TMR2IE bit		2:	
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit TMR2 TMR2 Register TMR2IE bit TMR2IF bit		2:	
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit		2:	29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 3, 25, 27 33 35, 36 70
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit TMR2 TMR2 Register TMR2IE bit TMR2IF bit		2:	29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 35, 36 70 30
TMR1H Register TMR1IE bit TMR1IF bit TMR1L TMR1L Register TMR1ON bit TMR2 TMR2 Register TMR2IE bit TMR2IE bit TMR2IF bit TMR2ON bit		2:	29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 3, 25, 27 33 35, 36 70 30 70
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO bit TOUTPS0 bit		2:	29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 3, 25, 27 33 35, 36 70 30 70 70
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO bit TOUTPS0 bit TOUTPS1 bit			29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 3, 25, 27 3, 33 35, 36 70 70 70 70 70
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO bit TOUTPS0 bit TOUTPS1 bit TOUTPS2 bit TOUTPS2 bit TOUTPS3 bit TOUTPS3 bit TOUTPS3 bit		22	29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 33 35, 36 70 70 70 70 70 70 70 29
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO bit TOUTPS0 bit TOUTPS1 bit TOUTPS2 bit TOUTPS2 bit TOUTPS3 bit TOUTPS3 bit TRISA Register			29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 35, 36 70 70 70 70 70 70 70 29 5, 28, 43
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO UTPS0 bit TOUTPS1 bit TOUTPS2 bit TOUTPS2 bit TOUTPS3 bit TOUTPS3 bit TRISA Register TRISA Register TRISB			29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 35, 36 70 70 70 70 70 70 70 29 6, 28, 43 29
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO UTPS0 bit TOUTPS0 bit TOUTPS1 bit TOUTPS2 bit TOUTPS2 bit TOUTPS3 bit TRISA Register TRISB TRISB Register			29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 35, 36 70 70 70 70 70 70 70 70 29 5, 28, 43 29 5, 28, 45
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO UTPS0 bit TOUTPS1 bit TOUTPS2 bit TOUTPS2 bit TOUTPS3 bit TOUTPS3 bit TRISA Register TRISB TRISB Register TRISB Register TRISC			29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 35, 36 70
TMR1H Register TMR1IE bit TMR1IF bit TMR1L Register TMR1ON bit TMR2 Register TMR2 Register TMR2IE bit TMR2IF bit TMR2ON bit TO UTPS0 bit TOUTPS0 bit TOUTPS1 bit TOUTPS2 bit TOUTPS2 bit TOUTPS3 bit TRISA Register TRISB TRISB Register TRISC TRISC Register			29 3, 25, 27 33 35, 36 29 3, 25, 27 65 29 3, 25, 27 33 35, 36 70 70 70 70 70 70 70 70 70 29 5, 28, 43 29 5, 28, 48
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