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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

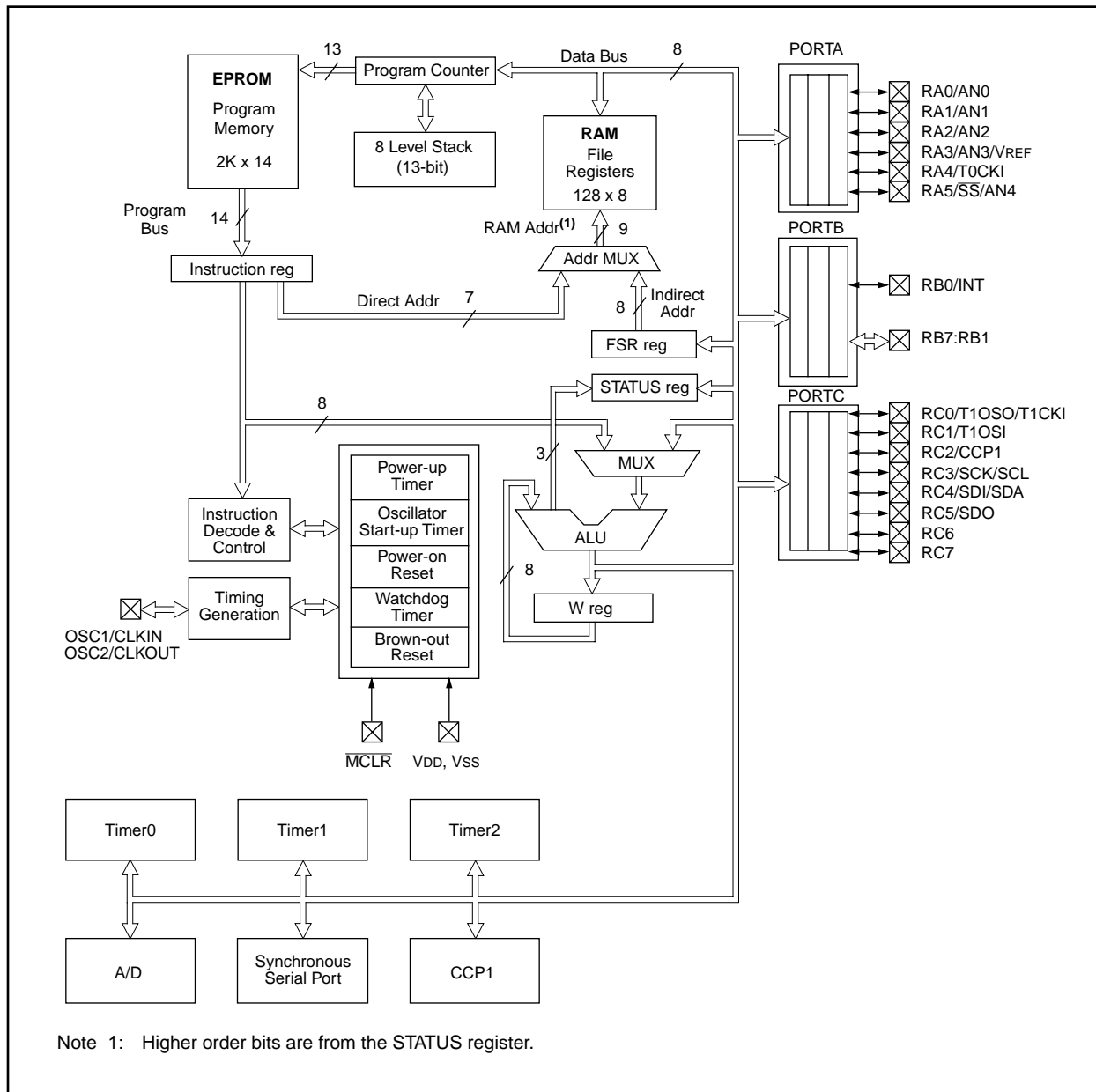
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lc77t-04-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16lc77t-04-pt</a>


# PIC16C7X

**FIGURE 3-1: PIC16C72 BLOCK DIAGRAM**



**FIGURE 4-4: PIC16C72 REGISTER FILE MAP**


File Address			File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADDD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh	ADRES		9Eh
1Fh	ADCON0	ADCON1	9Fh
20h	General Purpose Register	General Purpose Register	A0h
			BFh
			C0h
7Fh	Bank 0	Bank 1	FFh

 Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

**FIGURE 4-5: PIC16C73/73A/74/74A REGISTER FILE MAP**

File Address			File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	PORTD <sup>(2)</sup>	TRISD <sup>(2)</sup>	88h
09h	PORTE <sup>(2)</sup>	TRISE <sup>(2)</sup>	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	PIR2	PIE2	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON		90h
11h	TMR2		91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L		95h
16h	CCPR1H		96h
17h	CCP1CON		97h
18h	RCSTA	TXSTA	98h
19h	TXREG	SPBRG	99h
1Ah	RCREG		9Ah
1Bh	CCPR2L		9Bh
1Ch	CCPR2H		9Ch
1Dh	CCP2CON		9Dh
1Eh	ADRES		9Eh
1Fh	ADCON0	ADCON1	9Fh
20h			A0h
	General Purpose Register	General Purpose Register	
7Fh			FFh
	Bank 0	Bank 1	

 Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.  
 Note 2: These registers are not physically implemented on the PIC16C73/73A, read as '0'.

# PIC16C7X

**TABLE 5-1: PORTA FUNCTIONS**

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/ $\overline{SS}$ /AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

Legend: TTL = TTL input, ST = Schmitt Trigger input

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

## 10.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 10-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

### EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON    ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                        ; the new prescaler
                        ; mode value and CCP ON
MOVWF   CCP1CON    ;Load CCP1CON with this
                        ; value
```

## 10.2 Compare Mode

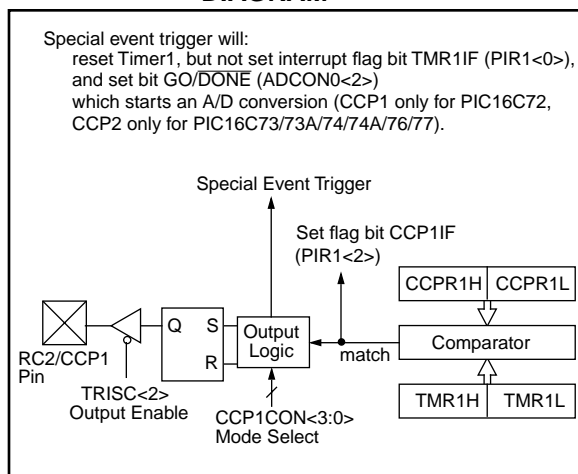
Applicable Devices							
72	73	73A	74	74A	76	77	

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven High
- Driven Low
- Remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

**FIGURE 10-3: COMPARE MODE OPERATION BLOCK DIAGRAM**



## 10.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

**Note:** Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

## 10.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

## 10.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

## 10.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCP2 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

For the PIC16C72 only, the special event trigger output of CCP1 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

**Note:** The special event trigger from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

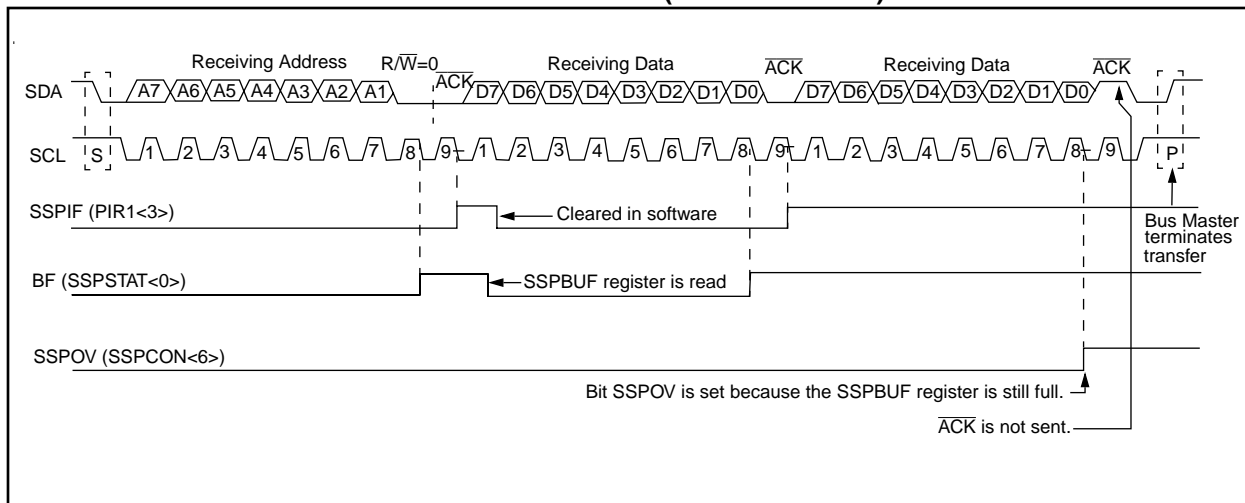
## 11.5.1.2 RECEPTION

When the  $R/\overline{W}$  bit of the address byte is clear and an address match occurs, the  $R/\overline{W}$  bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge ( $\overline{ACK}$ ) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

**FIGURE 11-25: I<sup>2</sup>C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)**



## 12.4 USART Synchronous Slave Mode

Applicable Devices						
72	73	73A	74	74A	76	77

Synchronous slave mode differs from the Master mode in the fact that the shift clock is supplied externally at the RC6/TX/CK pin (instead of being supplied internally in master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

### 12.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the synchronous master and slave modes are identical except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- The second word will remain in TXREG register.
- Flag bit TXIF will not be set.
- When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- If enable bit TXIE is set, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- Clear bits CREN and SREN.
- If interrupts are desired, then set enable bit TXIE.
- If 9-bit transmission is desired, then set bit TX9.
- Enable the transmission by setting enable bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.

### 12.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the synchronous master and slave modes is identical except in the case of the SLEEP mode. Also, bit SREN is a don't care in slave mode.

If receive is enabled, by setting bit CREN, prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

Steps to follow when setting up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- If interrupts are desired, then set enable bit RCIE.
- If 9-bit reception is desired, then set bit RX9.
- To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete and an interrupt will be generated, if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing bit CREN.

NOP		No Operation			
Syntax:	[ <i>label</i> ] NOP				
Operands:	None				
Operation:	No operation				
Status Affected:	None				
Encoding:	00	0000	0xx0	0000	
Description:	No operation.				
Words:	1				
Cycles:	1				
Q Cycle Activity:	Q1	Q2	Q3	Q4	
	Decode	No-Operation	No-Operation	No-Operation	
Example	NOP				

RETFIE		Return from Interrupt								
Syntax:	[ <i>label</i> ] RETFIE									
Operands:	None									
Operation:	TOS → PC, 1 → GIE									
Status Affected:	None									
Encoding:	00				0000	0000	1001			
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.									
Words:	1									
Cycles:	2									
Q Cycle Activity:	Q1				Q2		Q3		Q4	
1st Cycle	Decode		No-Operation		Set the GIE bit		Pop from the Stack			
2nd Cycle	No-Operation		No-Operation		No-Operation		No-Operation			

Example

```

RETFIE
After Interrupt
    PC =  TOS
    GIE =  1

```

OPTION	Load Option Register			
Syntax:	[ <i>label</i> ] OPTION			
Operands:	None			
Operation:	(W) → OPTION			
Status Affected:	None			
Encoding:	00	0000	0110	0010
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.			
Words:	1			
Cycles:	1			
Example	<div><b>To maintain upward compatibility with future PIC16CXX products, do not use this instruction.</b></div>			



# PIC16C7X

## SLEEP

Syntax: [ *label* ] SLEEP

Operands: None

Operation: 00h → WDT,  
0 → WDT prescaler,  
1 →  $\overline{TO}$ ,  
0 →  $\overline{PD}$

Status Affected:  $\overline{TO}$ ,  $\overline{PD}$

Encoding: 

00	0000	0110	0011
----	------	------	------

Description: The power-down status bit,  $\overline{PD}$  is cleared. Time-out status bit,  $\overline{TO}$  is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 14.8 for more details.

Words: 1

Cycles: 1

Q Cycle Activity: 

Q1	Q2	Q3	Q4
Decode	No-Operation	No-Operation	Go to Sleep

Example: SLEEP

## SUBLW

### Subtract W from Literal

Syntax: [ *label* ] SUBLW k

Operands:  $0 \leq k \leq 255$

Operation:  $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Encoding: 

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity: 

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example 1: SUBLW 0x02

Before Instruction

W = 1  
C = ?  
Z = ?

After Instruction

W = 1  
C = 1; result is positive  
Z = 0

Example 2: Before Instruction

W = 2  
C = ?  
Z = ?

After Instruction

W = 0  
C = 1; result is zero  
Z = 1

Example 3: Before Instruction

W = 3  
C = ?  
Z = ?

After Instruction

W = 0xFF  
C = 0; result is negative  
Z = 0

# PIC16C7X

## XORLW Exclusive OR Literal with W

Syntax: `[label] XORLW k`

Operands:  $0 \leq k \leq 255$

Operation:  $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Encoding: 

11	1010	kkkk	kkkk
----	------	------	------

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity: 

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example: `XORLW 0xAF`  
Before Instruction  
W = 0xB5  
After Instruction  
W = 0x1A

## XORWF Exclusive OR W with f

Syntax: `[label] XORWF f,d`

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:  $(W) .XOR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Encoding: 

00	0110	dfff	ffff
----	------	------	------

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity: 

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to destination

Example `XORWF REG 1`  
Before Instruction  
REG = 0xAF  
W = 0xB5  
After Instruction  
REG = 0x1A  
W = 0xB5

FIGURE 17-9: I<sup>2</sup>C BUS START/STOP BITS TIMING

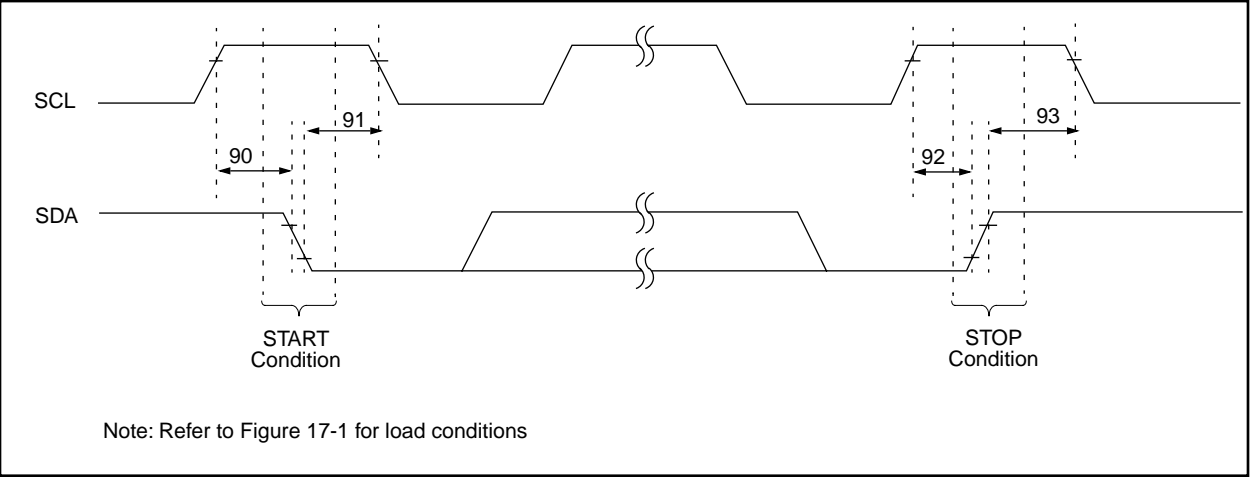
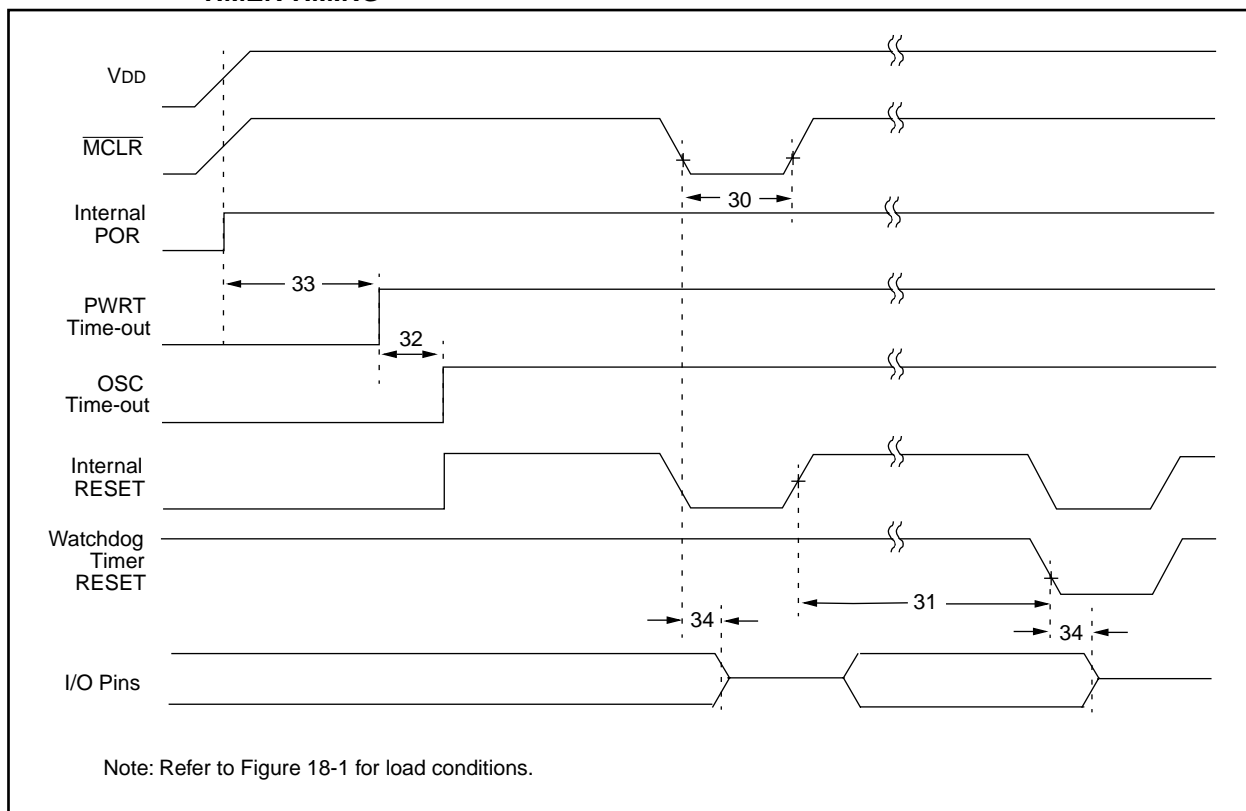


TABLE 17-8: I<sup>2</sup>C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

**FIGURE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**TABLE 18-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	100	—	—	ns	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	Tioz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	100	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 19.2 DC Characteristics: PIC16LC73A/74A-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN bit in configuration word enabled
D010	Supply Current (Note 2,5)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	μA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3,5)	IPD	-	7.5	30	μA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	μA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	μA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	Brown-out Reset Current (Note 6)	ΔIBOR	-	350	425	μA	BOR enabled VDD = 5.0V

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

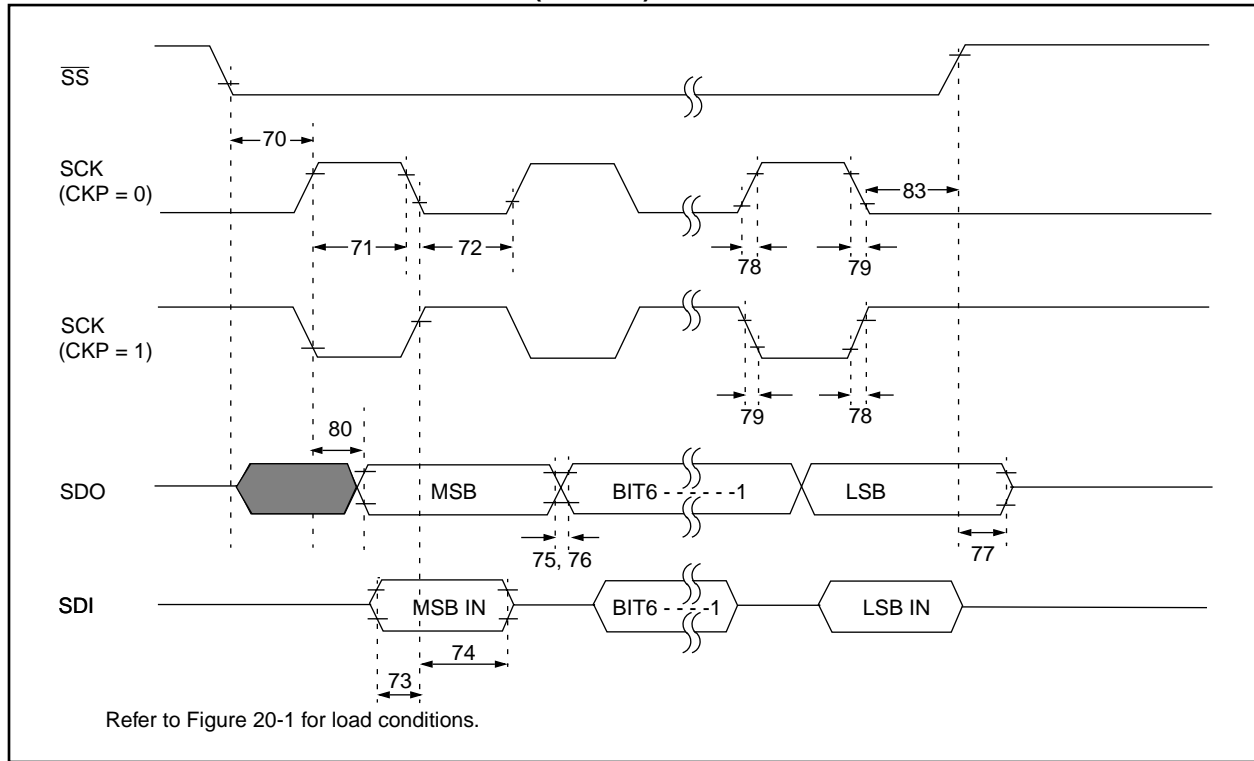
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{ext}$  (mA) with Rext in kOhm.

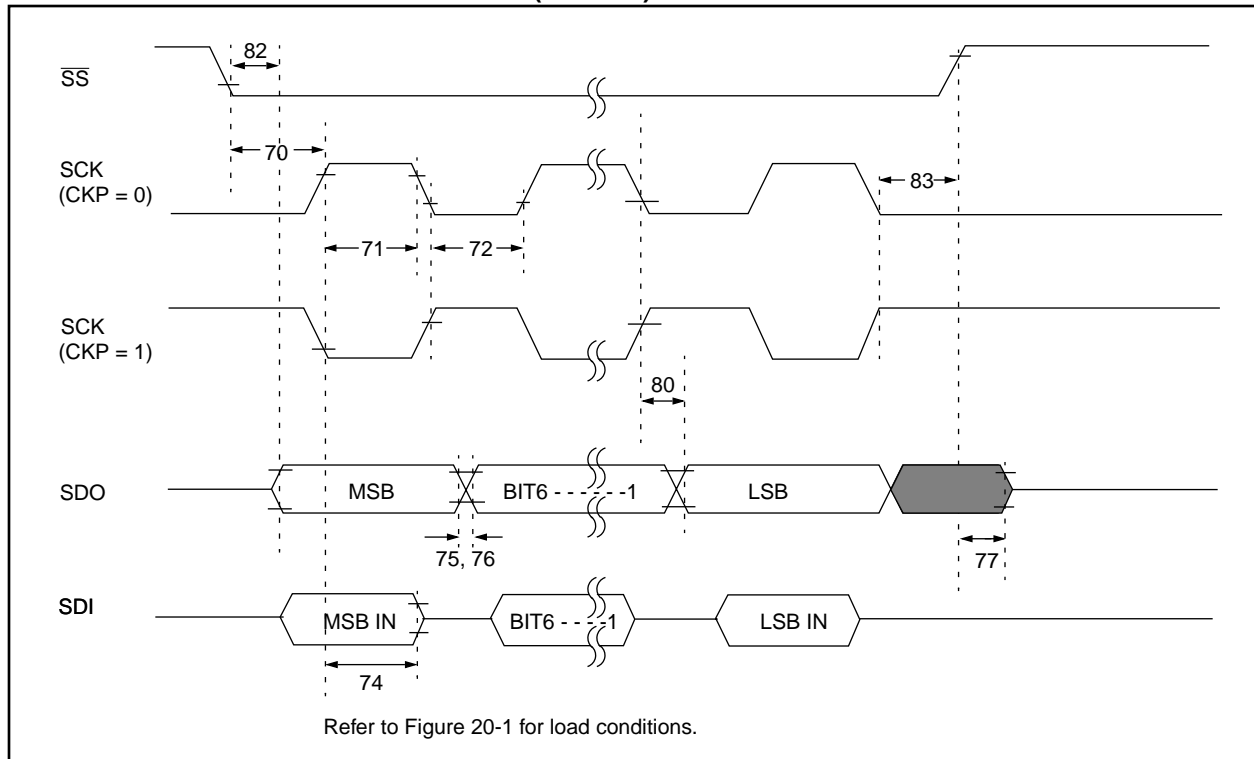
5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

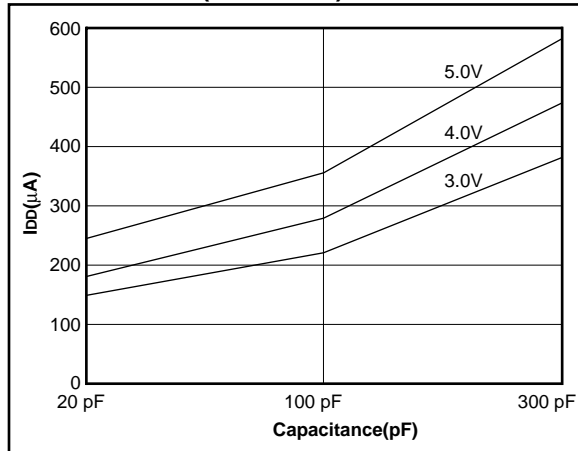
**FIGURE 20-11: SPI SLAVE MODE TIMING (CKE = 0)**



**FIGURE 20-12: SPI SLAVE MODE TIMING (CKE = 1)**



**FIGURE 21-18: TYPICAL  $I_{DD}$  vs. CAPACITANCE @ 500 kHz (RC MODE)**

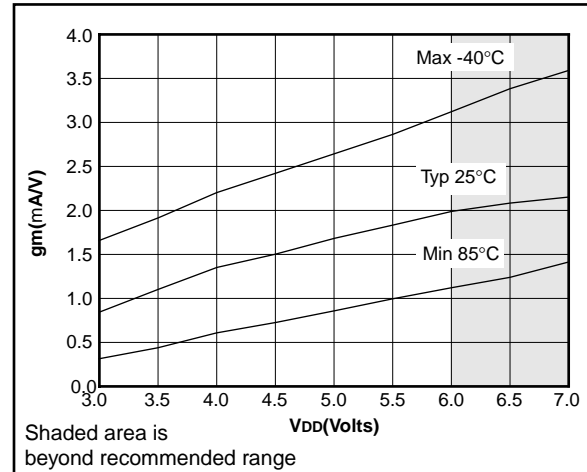


**TABLE 21-1: RC OSCILLATOR FREQUENCIES**

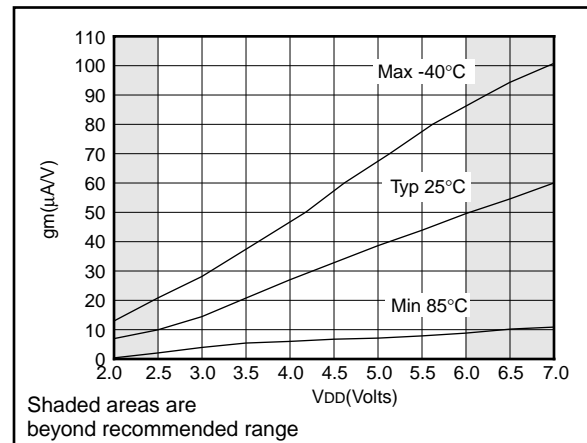
Cext	Rext	Average	
		Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviation from average value for  $V_{DD} = 5V$ .

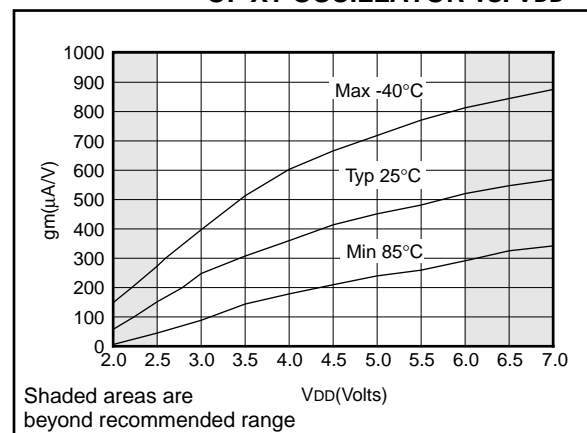
**FIGURE 21-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs.  $V_{DD}$**



**FIGURE 21-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs.  $V_{DD}$**



**FIGURE 21-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs.  $V_{DD}$**



Data based on matrix samples. See first page of this section for details.

# PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77

FIGURE 21-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)

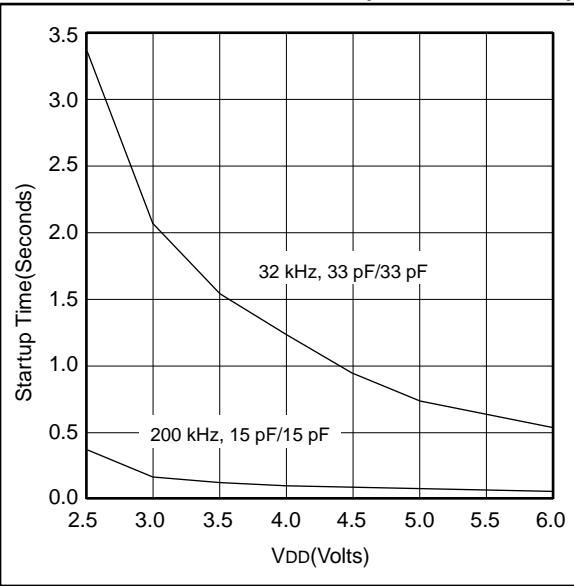


FIGURE 21-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)

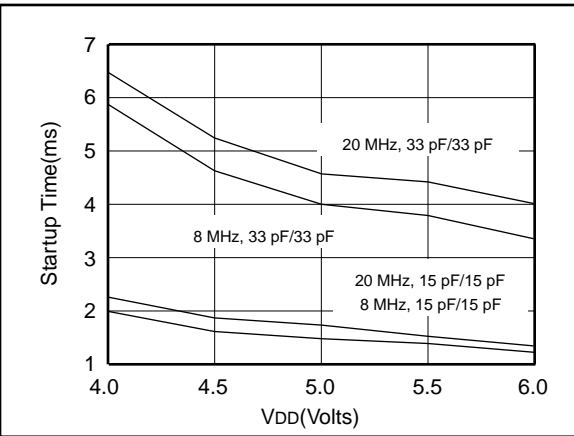


FIGURE 21-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)

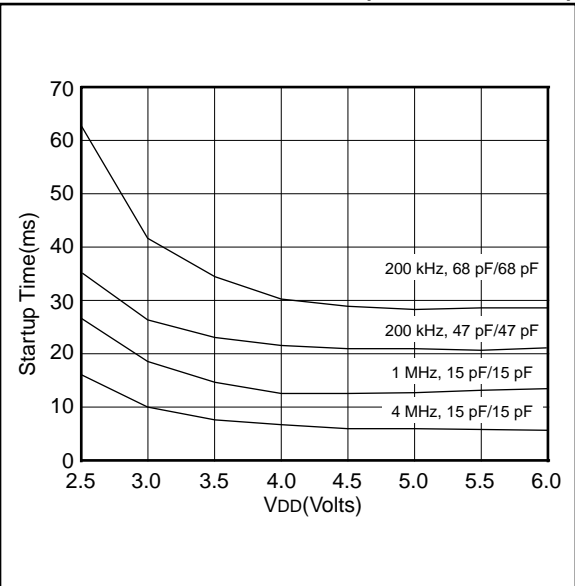


TABLE 21-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF
Crystals Used			
32 kHz	Epson C-001R32.768K-A	± 20 PPM	
200 kHz	STD XTL 200.000KHz	± 20 PPM	
1 MHz	ECS ECS-10-13-1	± 50 PPM	
4 MHz	ECS ECS-40-20-1	± 50 PPM	
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM	
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM	

Data based on matrix samples. See first page of this section for details.



# PIC16C7X

## E.3 PIC16C15X Family of Devices

		PIC16C154	PIC16CR154	PIC16C156	PIC16CR156	PIC16C158	PIC16CR158
<b>Clock</b>	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x12 words)	512	—	1K	—	2K	—
<b>Memory</b>	ROM Program Memory (x12 words)	—	512	—	1K	—	2K
	RAM Data Memory (bytes)	25	25	25	25	73	73
<b>Peripherals</b>	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
<b>Features</b>	I/O Pins	12	12	12	12	12	12
	Voltage Range (Volts)	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5	3.0-5.5	2.5-5.5
	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

## E.4 PIC16C5X Family of Devices

		PIC16C52	PIC16C54	PIC16C54A	PIC16CR54A	PIC16C55	PIC16C56
<b>Clock</b>	Maximum Frequency of Operation (MHz)	4	20	20	20	20	20
	EPROM Program Memory (x12 words)	384	512	512	—	512	1K
<b>Memory</b>	ROM Program Memory (x12 words)	—	—	—	512	—	—
	RAM Data Memory (bytes)	25	25	25	25	24	25
<b>Peripherals</b>	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
<b>Features</b>	I/O Pins	12	12	12	12	20	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.0-6.25	2.5-6.25	2.5-6.25
	Number of Instructions	33	33	33	33	33	33
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP

		PIC16C57	PIC16CR57B	PIC16C58A	PIC16CR58A
<b>Clock</b>	Maximum Frequency of Operation (MHz)	20	20	20	20
	EPROM Program Memory (x12 words)	2K	—	2K	—
<b>Memory</b>	ROM Program Memory (x12 words)	—	2K	—	2K
	RAM Data Memory (bytes)	72	72	73	73
<b>Peripherals</b>	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
<b>Features</b>	I/O Pins	20	20	12	12
	Voltage Range (Volts)	2.5-6.25	2.5-6.25	2.0-6.25	2.5-6.25
	Number of Instructions	33	33	33	33
	Packages	28-pin DIP, SOIC, SSOP	28-pin DIP, SOIC, SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

## E.8 PIC16C8X Family of Devices

		PIC16F83	PIC16CR83	PIC16F84	PIC16CR84
<b>Clock</b>	Maximum Frequency of Operation (MHz)	10	10	10	10
	Flash Program Memory	512	—	1K	—
<b>Memory</b>	EEPROM Program Memory	—	—	—	—
	ROM Program Memory	—	512	—	1K
	Data Memory (bytes)	36	36	68	68
	Data EEPROM (bytes)	64	64	64	64
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
<b>Peripherals</b>	Interrupt Sources	4	4	4	4
	I/O Pins	13	13	13	13
	Voltage Range (Volts)	2.0-6.0	2.0-6.0	2.0-6.0	2.0-6.0
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C8X Family devices use serial programming with clock pin RB6 and data pin RB7.

## E.9 PIC16C9XX Family Of Devices

		PIC16C923	PIC16C924
<b>Clock</b>	Maximum Frequency of Operation (MHz)	8	8
<b>Memory</b>	EPROM Program Memory	4K	4K
	Data Memory (bytes)	176	176
<b>Peripherals</b>	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/PWM Module(s)	1	1
	Serial Port(s) (SPI/I <sup>2</sup> C, USART)	SPI/I <sup>2</sup> C	SPI/I <sup>2</sup> C
	Parallel Slave Port	—	—
	A/D Converter (8-bit) Channels	—	5
	LCD Module	4 Com, 32 Seg	4 Com, 32 Seg
	Interrupt Sources	8	9
<b>Features</b>	I/O Pins	25	25
	Input Pins	27	27
	Voltage Range (Volts)	3.0-6.0	3.0-6.0
	In-Circuit Serial Programming	Yes	Yes
	Brown-out Reset	—	—
	Packages	64-pin SDIP <sup>(1)</sup> , TQFP; 68-pin PLCC, Die	64-pin SDIP <sup>(1)</sup> , TQFP; 68-pin PLCC, Die

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C9XX Family devices use serial programming with clock pin RB6 and data pin RB7.

# PIC16C7X

## E.10 PIC17CXXX Family of Devices

		PIC17C42A	PIC17CR42	PIC17C43	PIC17CR43	PIC17C44
Clock	Maximum Frequency of Operation (MHz)	33	33	33	33	33
Memory	EPROM Program Memory (words)	2K	—	4K	—	8K
	ROM Program Memory (words)	—	2K	—	4K	—
	RAM Data Memory (bytes)	232	232	454	454	454
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3
	Captures/PWM Module(s)	2	2	2	2	2
	Serial Port(s) (USART)	Yes	Yes	Yes	Yes	Yes
Features	Hardware Multiply	Yes	Yes	Yes	Yes	Yes
	External Interrupts	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	11	11	11	11	11
	I/O Pins	33	33	33	33	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	Number of Instructions	58	58	58	58	58
	Packages	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP	40-pin DIP; 44-pin PLCC, MQFP, TQFP

		PIC17C752	PIC17C756
Clock	Maximum Frequency of Operation (MHz)	33	33
Memory	EPROM Program Memory (words)	8K	16K
	ROM Program Memory (words)	—	—
	RAM Data Memory (bytes)	454	902
Peripherals	Timer Module(s)	TMR0, TMR1, TMR2, TMR3	TMR0, TMR1, TMR2, TMR3
	Captures/PWM Module(s)	4/3	4/3
	Serial Port(s) (USART)	2	2
Features	Hardware Multiply	Yes	Yes
	External Interrupts	Yes	Yes
	Interrupt Sources	18	18
	I/O Pins	50	50
	Voltage Range (Volts)	3.0-6.0	3.0-6.0
	Number of Instructions	58	58
	Packages	64-pin DIP; 68-pin LCC, 68-pin TQFP	64-pin DIP; 68-pin LCC, 68-pin TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

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# PIC16C6X

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