



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc77t-04i-pt

2.0 PIC16C7X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C7X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C7X family, there are two device "types" as indicated in the device number:

1. **C**, as in PIC16**C**74. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**74. These devices have EPROM type memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in Cerdip package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® Plus and PRO MATE® II programmers both support programming of the PIC16C7X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

PIC16C7X

TABLE 3-2: PIC16C73/73A/76 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	1	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
RA0/AN0	2	2	I/O	TTL	PORTA is a bi-directional I/O port. RA0 can also be analog input0 RA1 can also be analog input1 RA2 can also be analog input2 RA3 can also be analog input3 or analog reference voltage RA4 can also be the clock input to the Timer0 module. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.
RA1/AN1	3	3	I/O	TTL	
RA2/AN2	4	4	I/O	TTL	
RA3/AN3/VREF	5	5	I/O	TTL	
RA4/T0CKI	6	6	I/O	ST	
RA5/SS/AN4	7	7	I/O	TTL	
RB0/INT	21	21	I/O	TTL/ST ⁽¹⁾	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0 can also be the external interrupt pin. Interrupt on change pin. Interrupt on change pin. Interrupt on change pin. Serial programming clock. Interrupt on change pin. Serial programming data.
RB1	22	22	I/O	TTL	
RB2	23	23	I/O	TTL	
RB3	24	24	I/O	TTL	
RB4	25	25	I/O	TTL	
RB5	26	26	I/O	TTL	
RB6	27	27	I/O	TTL/ST ⁽²⁾	
RB7	28	28	I/O	TTL/ST ⁽²⁾	
RC0/T1OSO/T1CKI	11	11	I/O	ST	PORTC is a bi-directional I/O port. RC0 can also be the Timer1 oscillator output or Timer1 clock input. RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output. RC2 can also be the Capture1 input/Compare1 output/PWM1 output. RC3 can also be the synchronous serial clock input/output for both SPI and I ² C modes. RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode). RC5 can also be the SPI Data Out (SPI mode). RC6 can also be the USART Asynchronous Transmit or Synchronous Clock. RC7 can also be the USART Asynchronous Receive or Synchronous Data.
RC1/T1OSI/CCP2	12	12	I/O	ST	
RC2/CCP1	13	13	I/O	ST	
RC3/SCK/SCL	14	14	I/O	ST	
RC4/SDI/SDA	15	15	I/O	ST	
RC5/SDO	16	16	I/O	ST	
RC6/TX/CK	17	17	I/O	ST	
RC7/RX/DT	18	18	I/O	ST	
Vss	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

4.0 MEMORY ORGANIZATION

Applicable Devices							
72	73	73A	74	74A	76	77	

4.1 Program Memory Organization

The PIC16C7X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

Device	Program Memory	Address Range
PIC16C72	2K x 14	0000h-07FFh
PIC16C73	4K x 14	0000h-0FFFh
PIC16C73A	4K x 14	0000h-0FFFh
PIC16C74	4K x 14	0000h-0FFFh
PIC16C74A	4K x 14	0000h-0FFFh
PIC16C76	8K x 14	0000h-1FFFh
PIC16C77	8K x 14	0000h-1FFFh

For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C72 PROGRAM MEMORY MAP AND STACK

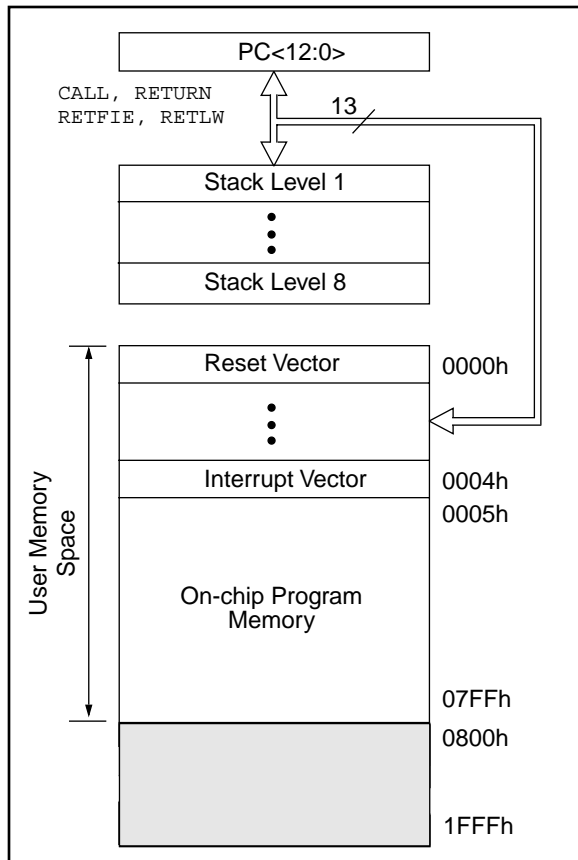
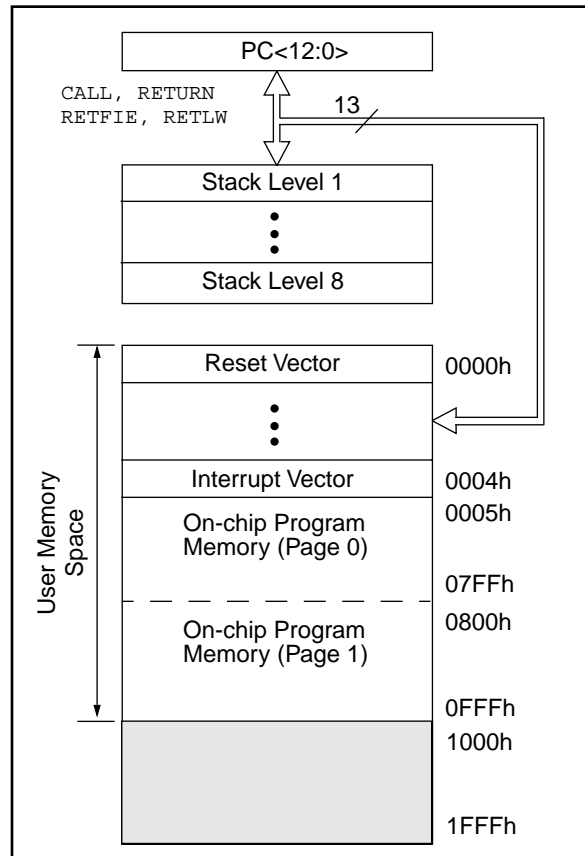


FIGURE 4-2: PIC16C73/73A/74/74A PROGRAM MEMORY MAP AND STACK



PIC16C7X

TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/ \overline{SS} /AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

5.6 I/O Programming Considerations

Applicable Devices				
72	73	73A	74	74A
76	77			

5.6.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched to an output, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-4 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 5-4: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

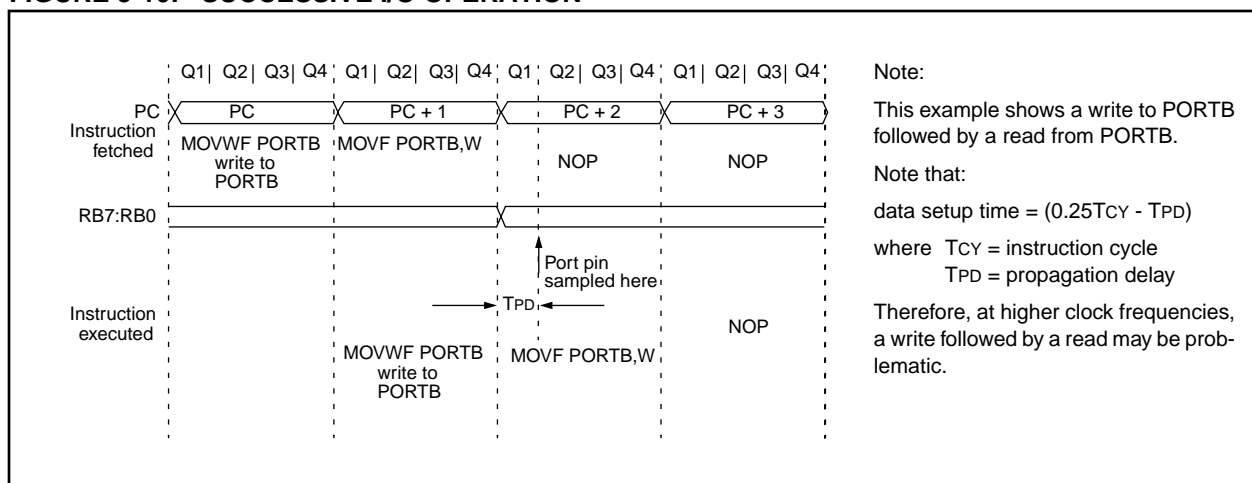
```
;Initial PORT settings: PORTB<7:4> Inputs
;                          PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;
;          PORT latch  PORT pins
;          -----
BCF PORTB, 7    ; 01pp pppp    11pp pppp
BCF PORTB, 6    ; 10pp pppp    11pp pppp
BSF STATUS, RP0 ;
BCF TRISB, 7    ; 10pp pppp    11pp pppp
BCF TRISB, 6    ; 10pp pppp    10pp pppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-10). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-10: SUCCESSIVE I/O OPERATION



The \overline{SS} pin allows a synchronous slave mode. The SPI must be in slave mode (SSPCON<3:0> = 04h) and the TRISA<5> bit must be set for synchronous slave mode to be enabled. When the \overline{SS} pin is low, transmission and reception are enabled and the SDO pin is driven. When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. If the \overline{SS} pin is taken low without resetting SPI mode, the transmission will continue from the

point at which it was taken high. External pull-up/pull-down resistors may be desirable, depending on the application.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 11-5: SPI MODE TIMING, MASTER MODE OR SLAVE MODE W/O \overline{SS} CONTROL

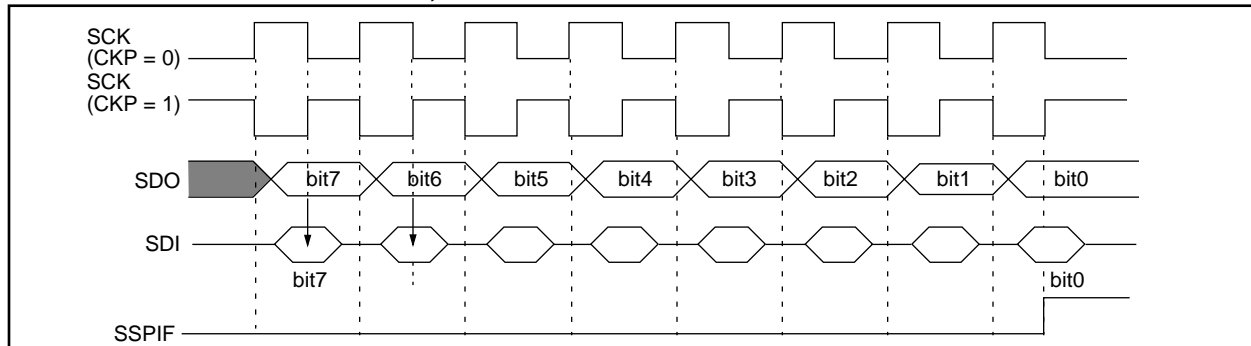


FIGURE 11-6: SPI MODE TIMING, SLAVE MODE WITH \overline{SS} CONTROL

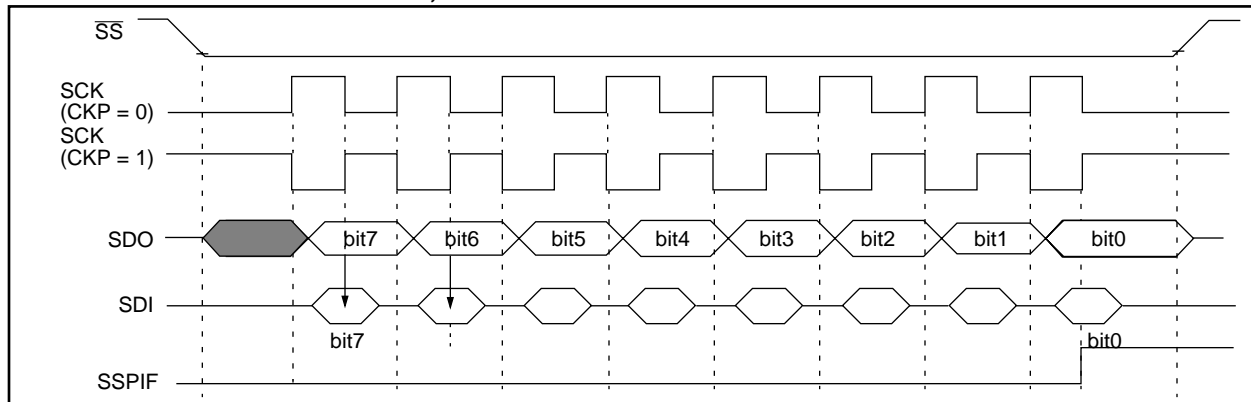


TABLE 11-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ^(1,2)	ADIF	RCIF ⁽²⁾	TXIF ⁽²⁾	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE ^(1,2)	ADIE	RCIE ⁽²⁾	TXIE ⁽²⁾	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
94h	SSPSTAT	—	—	D/A	P	S	R/W	UA	BF	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A, always maintain these bits clear.

2: The PIC16C72 does not have a Parallel Slave Port or USART, these bits are unimplemented, read as '0'.

PIC16C7X

TABLE 12-3: BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	FOSC = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	9.766	+1.73	255	9.622	+0.23	185
19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
96	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25	94.20	-1.88	18
300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	-0.57	5
500	500	0	9	500	0	7	500	0	4	NA	-	-
HIGH	5000	-	0	4000	-	0	2500	-	0	1789.8	-	0
LOW	19.53	-	255	15.625	-	255	9.766	-	255	6.991	-	255

BAUD RATE (K)	FOSC = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	NA	-	-	NA	-	-	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	-	-	NA	-	-	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.6	0	131	9.615	+0.16	103	9.622	+0.23	92	9.615	+0.16	25	NA	-	-
19.2	19.2	0	65	19.231	+0.16	51	19.04	-0.83	46	19.24	+0.16	12	NA	-	-
76.8	79.2	+3.13	15	76.923	+0.16	12	74.57	-2.90	11	83.34	+8.51	2	NA	-	-
96	97.48	+1.54	12	1000	+4.17	9	99.43	+3.57	8	NA	-	-	NA	-	-
300	316.8	+5.60	3	NA	-	-	298.3	-0.57	2	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	1267	-	0	100	-	0	894.9	-	0	250	-	0	8.192	-	0
LOW	4.950	-	255	3.906	-	255	3.496	-	255	0.9766	-	255	0.032	-	255

TABLE 12-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD RATE (K)	FOSC = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	-
96	104.2	+8.51	2	NA	-	-	NA	-	-	NA	-	-
300	312.5	+4.17	0	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	312.5	-	0	250	-	0	156.3	-	0	111.9	-	0
LOW	1.221	-	255	0.977	-	255	0.6104	-	255	0.437	-	255

BAUD RATE (K)	FOSC = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46	1.202	+0.16	12	NA	-	-
2.4	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22	2.232	-6.99	6	NA	-	-
9.6	9.9	+3.13	7	NA	-	-	9.322	-2.90	5	NA	-	-	NA	-	-
19.2	19.8	+3.13	3	NA	-	-	18.64	-2.90	2	NA	-	-	NA	-	-
76.8	79.2	+3.13	0	NA	-	-	NA	-	-	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	79.2	-	0	62.500	-	0	55.93	-	0	15.63	-	0	0.512	-	0
LOW	0.3094	-	255	3.906	-	255	0.2185	-	255	0.0610	-	255	0.0020	-	255

TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Transmission.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A/76, always maintain these bits clear.

TABLE 12-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
1Ah	RCREG	USART Receive Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16C73/73A/76, always maintain these bits clear.

PIC16C7X

14.7 Watchdog Timer (WDT)

Applicable Devices

72 73 73A 74 74A 76 77

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 14.1).

14.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a

prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The \overline{TO} bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

14.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 14-18: WATCHDOG TIMER BLOCK DIAGRAM

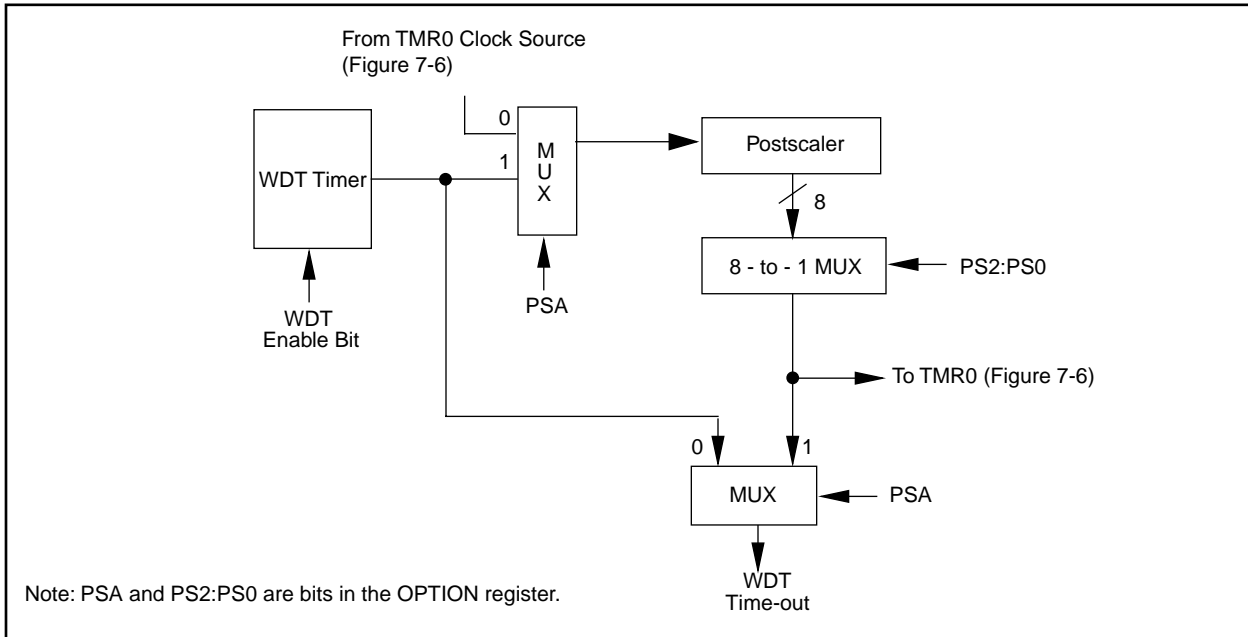


FIGURE 14-19: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN ⁽¹⁾	CP1	CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h, 181h	OPTION	\overline{RBPU}	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 14-1, and Figure 14-2 for operation of these bits.

PIC16C7X

IORWF Inclusive OR W with f

Syntax:	[<i>label</i>] IORWF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(W) .OR. (f) \rightarrow (destination)			
Status Affected:	Z			
Encoding:	00	0100	dfff	ffff
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination

Example IORWF RESULT, 0

Before Instruction

RESULT = 0x13
W = 0x91

After Instruction

RESULT = 0x13
W = 0x93
Z = 1

MOVF Move f

Syntax:	[<i>label</i>] MOVF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) \rightarrow (destination)			
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The contents of register f is moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to destination

Example MOVF FSR, 0

After Instruction

W = value in FSR register
Z = 1

MOVLW Move Literal to W

Syntax:	[<i>label</i>] MOVLW k			
Operands:	$0 \leq k \leq 255$			
Operation:	$k \rightarrow (W)$			
Status Affected:	None			
Encoding:	11	00xx	kkkk	kkkk
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write to W

Example

MOVLW 0x5A

After Instruction

W = 0x5A

MOVWF Move W to f

Syntax:	[<i>label</i>] MOVWF f			
Operands:	$0 \leq f \leq 127$			
Operation:	(W) \rightarrow (f)			
Status Affected:	None			
Encoding:	00	0000	1fff	ffff
Description:	Move data from W register to register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write register 'f'

Example

MOVWF OPTION_REG

Before Instruction

OPTION = 0xFF
W = 0x4F

After Instruction

OPTION = 0x4F
W = 0x4F

FIGURE 17-9: I²C BUS START/STOP BITS TIMING

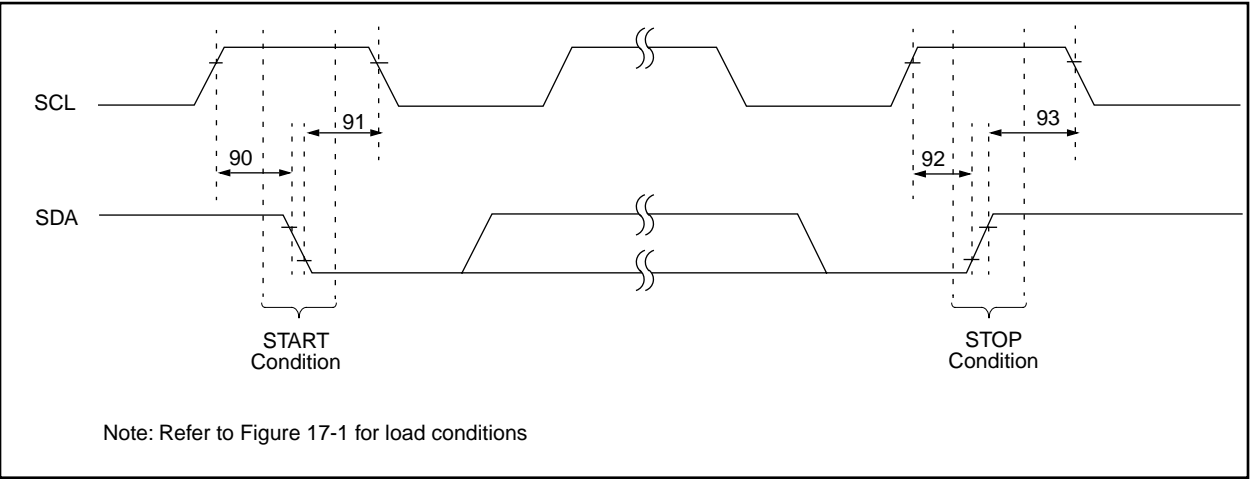


TABLE 17-8: I²C BUS START/STOP BITS REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

FIGURE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

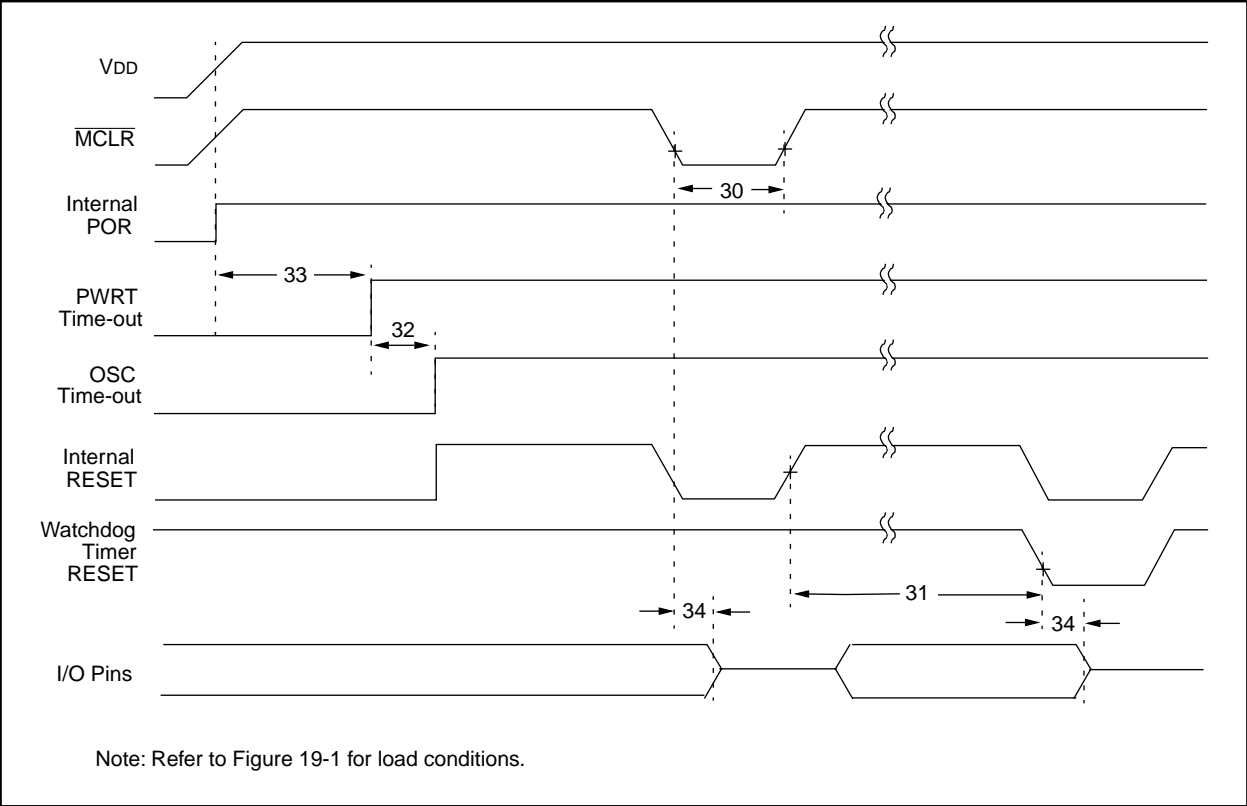


FIGURE 19-5: BROWN-OUT RESET TIMING

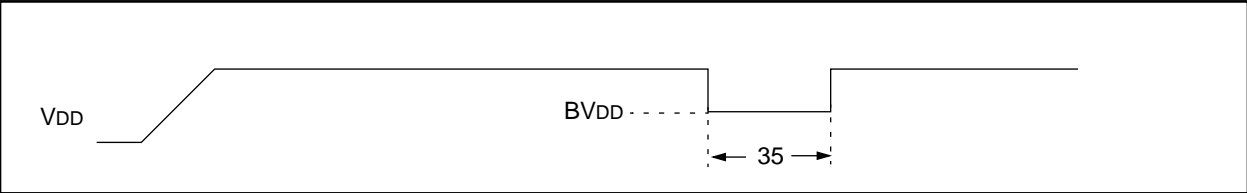


TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset pulse width	100	—	—	μs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77

FIGURE 20-9: SPI MASTER MODE TIMING (CKE = 0)

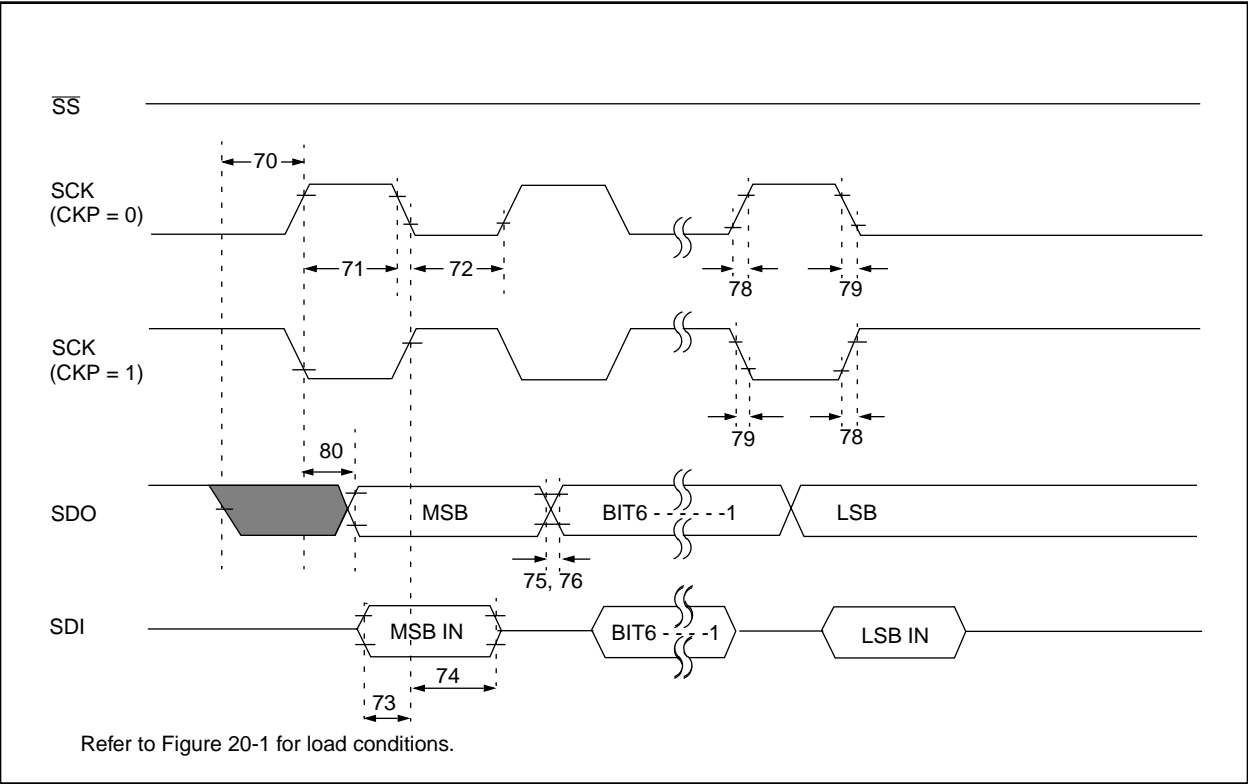
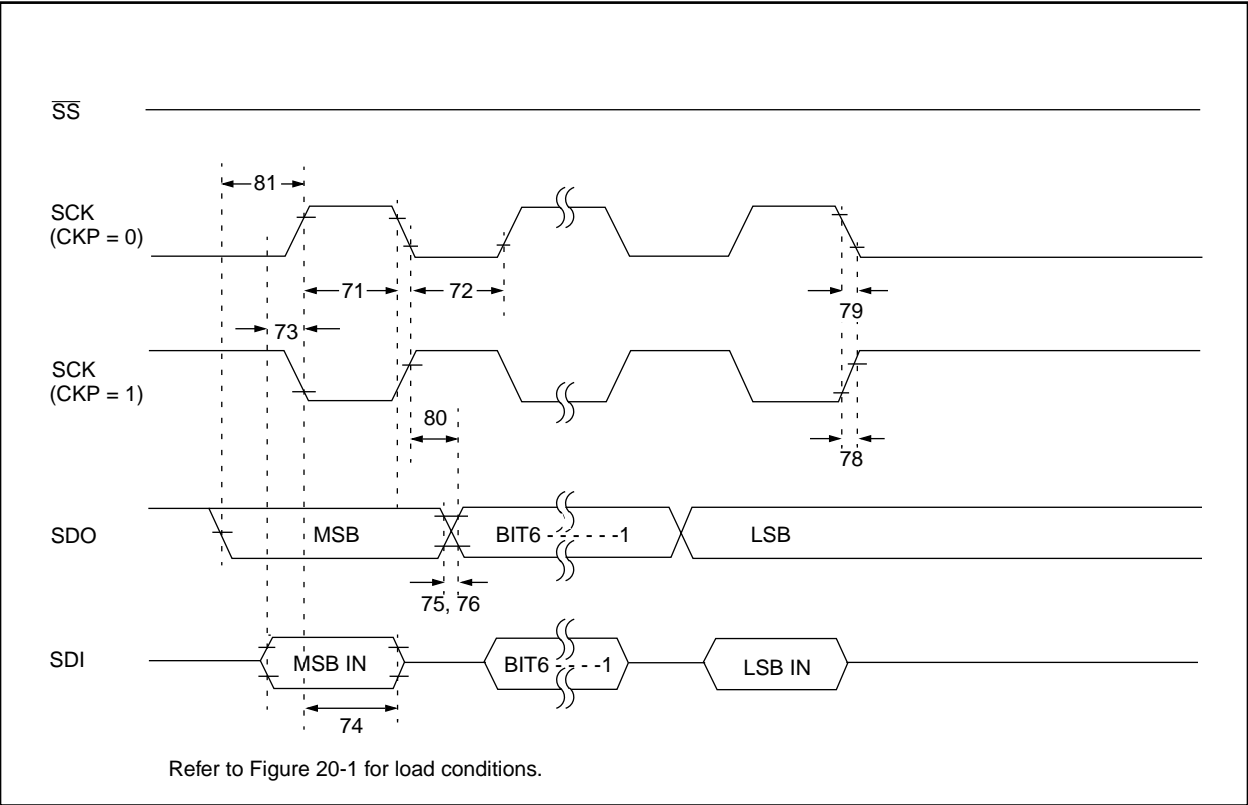


FIGURE 20-10: SPI MASTER MODE TIMING (CKE = 1)



PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77

FIGURE 20-14: I²C BUS DATA TIMING

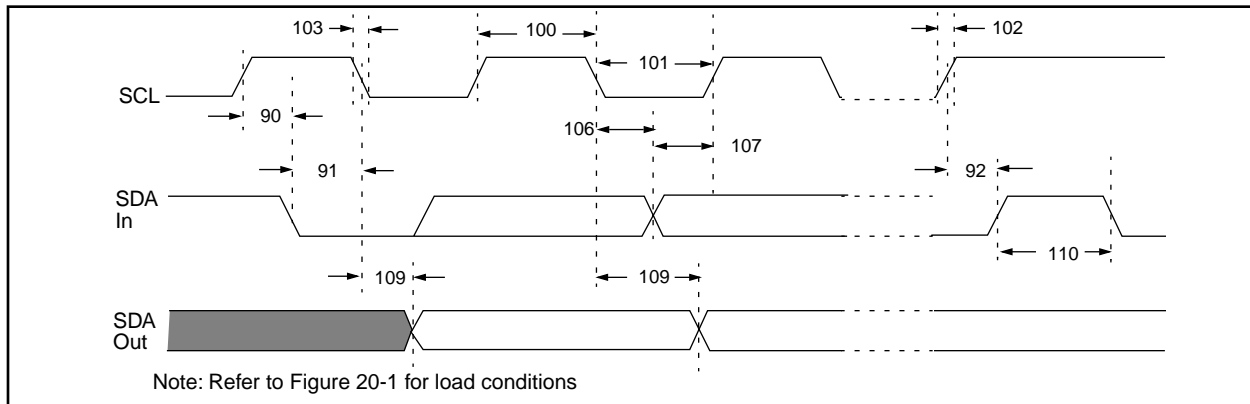


TABLE 20-10: I²C BUS DATA REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	μs
			400 kHz mode	0.6	—	μs
			SSP Module	1.5T _{CY}	—	
101	TLOW	Clock low time	100 kHz mode	4.7	—	μs
			400 kHz mode	1.3	—	μs
			SSP Module	1.5T _{CY}	—	
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns
			400 kHz mode	20 + 0.1Cb	300	ns
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns
			400 kHz mode	20 + 0.1Cb	300	ns
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs
			400 kHz mode	0.6	—	μs
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs
			400 kHz mode	0.6	—	μs
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns
			400 kHz mode	0	0.9	μs
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns
			400 kHz mode	100	—	ns
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs
			400 kHz mode	0.6	—	μs
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns
			400 kHz mode	—	—	ns
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs
			400 kHz mode	1.3	—	μs
	Cb	Bus capacitive loading	—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

- 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

PIC16C7X

Applicable Devices 72 73 73A 74 74A 76 77

TABLE 20-13: A/D CONVERTER CHARACTERISTICS:

PIC16C76/77-04 (Commercial, Industrial, Extended)
 PIC16C76/77-10 (Commercial, Industrial, Extended)
 PIC16C76/77-20 (Commercial, Industrial, Extended)
 PIC16LC76/77-04 (Commercial, Industrial)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	8-bits	bit	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A02	EABS	Total Absolute error	—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral linearity error	—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	EDL	Differential linearity error	—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A05	EFS	Full scale error	—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A06	EOFF	Offset error	—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity	—	guaranteed	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage	3.0V	—	VDD + 0.3	V	
A25	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	PIC16C76/77	—	180	—	Average current consumption when A/D is on. (Note 1)
			PIC16LC76/77	—	90	—	
A50	IREF	VREF input current (Note 2)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 13.1.
			—	—	10	μA	During A/D Conversion cycle

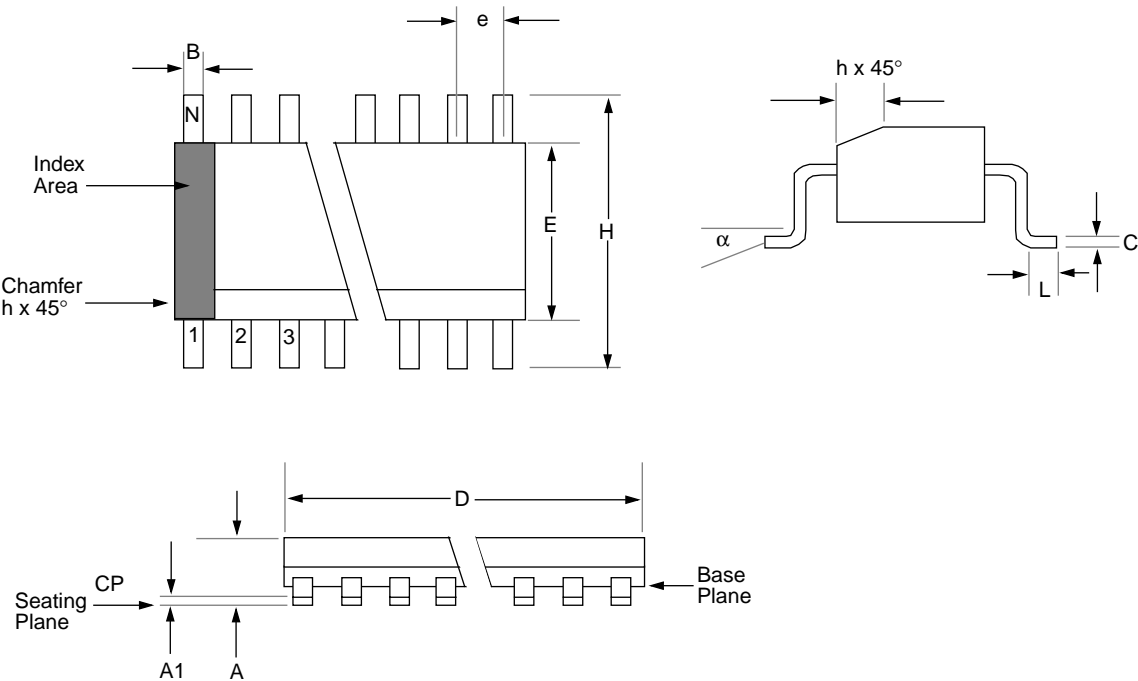
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

22.5 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body) (SO)



Package Group: Plastic SOIC (SO)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	17.703	18.085		0.697	0.712	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	28	28		28	28	
CP	—	0.102		—	0.004	

PIC16C7X

LIST OF FIGURES

Figure 3-1:	PIC16C72 Block Diagram	10	Figure 8-1:	T1CON: Timer1 Control Register (Address 10h)	65
Figure 3-2:	PIC16C73/73A/76 Block Diagram	11	Figure 8-2:	Timer1 Block Diagram	66
Figure 3-3:	PIC16C74/74A/77 Block Diagram	12	Figure 9-1:	Timer2 Block Diagram	69
Figure 3-4:	Clock/Instruction Cycle	17	Figure 9-2:	T2CON: Timer2 Control Register (Address 12h)	70
Figure 4-1:	PIC16C72 Program Memory Map and Stack	19	Figure 10-1:	CCP1CON Register (Address 17h)/ CCP2CON Register (Address 1Dh)	72
Figure 4-2:	PIC16C73/73A/74/74A Program Memory Map and Stack	19	Figure 10-2:	Capture Mode Operation Block Diagram	72
Figure 4-3:	PIC16C76/77 Program Memory Map and Stack	20	Figure 10-3:	Compare Mode Operation Block Diagram	73
Figure 4-4:	PIC16C72 Register File Map	21	Figure 10-4:	Simplified PWM Block Diagram	74
Figure 4-5:	PIC16C73/73A/74/74A Register File Map	21	Figure 10-5:	PWM Output	74
Figure 4-6:	PIC16C76/77 Register File Map	22	Figure 11-1:	SSPSTAT: Sync Serial Port Status Register (Address 94h)	78
Figure 4-7:	Status Register (Address 03h, 83h, 103h, 183h)	30	Figure 11-2:	SSPCON: Sync Serial Port Control Register (Address 14h)	79
Figure 4-8:	OPTION Register (Address 81h, 181h)	31	Figure 11-3:	SSP Block Diagram (SPI Mode)	80
Figure 4-9:	INTCON Register (Address 0Bh, 8Bh, 10Bh, 18Bh)	32	Figure 11-4:	SPI Master/Slave Connection	81
Figure 4-10:	PIE1 Register PIC16C72 (Address 8Ch)	33	Figure 11-5:	SPI Mode Timing, Master Mode or Slave Mode w/o SS Control	82
Figure 4-11:	PIE1 Register PIC16C73/73A/ 74/74A/76/77 (Address 8Ch)	34	Figure 11-6:	SPI Mode Timing, Slave Mode with SS Control	82
Figure 4-12:	PIR1 Register PIC16C72 (Address 0Ch)	35	Figure 11-7:	SSPSTAT: Sync Serial Port Status Register (Address 94h)(PIC16C76/77)	83
Figure 4-13:	PIR1 Register PIC16C73/73A/ 74/74A/76/77 (Address 0Ch)	36	Figure 11-8:	SSPCON: Sync Serial Port Control Register (Address 14h)(PIC16C76/77)	84
Figure 4-14:	PIE2 Register (Address 8Dh)	37	Figure 11-9:	SSP Block Diagram (SPI Mode) (PIC16C76/77)	85
Figure 4-15:	PIR2 Register (Address 0Dh)	38	Figure 11-10:	SPI Master/Slave Connection PIC16C76/77)	86
Figure 4-16:	PCON Register (Address 8Eh)	39	Figure 11-11:	SPI Mode Timing, Master Mode (PIC16C76/77)	87
Figure 4-17:	Loading of PC In Different Situations	40	Figure 11-12:	SPI Mode Timing (Slave Mode With CKE = 0) (PIC16C76/77)	87
Figure 4-18:	Direct/Indirect Addressing	41	Figure 11-13:	SPI Mode Timing (Slave Mode With CKE = 1) (PIC16C76/77)	88
Figure 5-1:	Block Diagram of RA3:RA0 and RA5 Pins	43	Figure 11-14:	Start and Stop Conditions	89
Figure 5-2:	Block Diagram of RA4/T0CKI Pin	43	Figure 11-15:	7-bit Address Format	90
Figure 5-3:	Block Diagram of RB3:RB0 Pins	45	Figure 11-16:	I ² C 10-bit Address Format	90
Figure 5-4:	Block Diagram of RB7:RB4 Pins (PIC16C73/74)	46	Figure 11-17:	Slave-receiver Acknowledge	90
Figure 5-5:	Block Diagram of RB7:RB4 Pins (PIC16C72/73A/ 74A/76/77)	46	Figure 11-18:	Data Transfer Wait State	90
Figure 5-6:	PORTC Block Diagram (Peripheral Output Override)	48	Figure 11-19:	Master-transmitter Sequence	91
Figure 5-7:	PORTD Block Diagram (in I/O Port Mode)	50	Figure 11-20:	Master-receiver Sequence	91
Figure 5-8:	PORTE Block Diagram (in I/O Port Mode)	51	Figure 11-21:	Combined Format	91
Figure 5-9:	TRISE Register (Address 89h)	51	Figure 11-22:	Multi-master Arbitration (Two Masters)	92
Figure 5-10:	Successive I/O Operation	53	Figure 11-23:	Clock Synchronization	92
Figure 5-11:	PORTD and PORTE Block Diagram (Parallel Slave Port)	54	Figure 11-24:	SSP Block Diagram (I ² C Mode)	93
Figure 5-12:	Parallel Slave Port Write Waveforms	55	Figure 11-25:	I ² C Waveforms for Reception (7-bit Address)	95
Figure 5-13:	Parallel Slave Port Read Waveforms	55	Figure 11-26:	I ² C Waveforms for Transmission (7-bit Address)	96
Figure 7-1:	Timer0 Block Diagram	59	Figure 11-27:	Operation of the I ² C Module in IDLE_MODE, RCV_MODE or XMIT_MODE	98
Figure 7-2:	Timer0 Timing: Internal Clock/No Prescale	59	Figure 12-1:	TXSTA: Transmit Status and Control Register (Address 98h)	99
Figure 7-3:	Timer0 Timing: Internal Clock/Prescale 1:2	60	Figure 12-2:	RCSTA: Receive Status and Control Register (Address 18h)	100
Figure 7-4:	Timer0 Interrupt Timing	60	Figure 12-3:	RX Pin Sampling Scheme. BRGH = 0 (PIC16C73/73A/74/74A)	104
Figure 7-5:	Timer0 Timing with External Clock	61	Figure 12-4:	RX Pin Sampling Scheme, BRGH = 1 (PIC16C73/73A/74/74A)	104
Figure 7-6:	Block Diagram of the Timer0/WDT Prescaler	62			

Figure 12-5:	RX Pin Sampling Scheme, BRGH = 1 (PIC16C73/73A/74/74A)	104	Figure 17-4:	Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing	175
Figure 12-6:	RX Pin Sampling Scheme, BRGH = 0 OR BRGH = 1 (PIC16C76/77)	105	Figure 17-5:	Brown-out Reset Timing	175
Figure 12-7:	USART Transmit Block Diagram	106	Figure 17-6:	Timer0 and Timer1 External Clock Timings	176
Figure 12-8:	Asynchronous Master Transmission	107	Figure 17-7:	Capture/Compare/PWM Timings (CCP1)	177
Figure 12-9:	Asynchronous Master Transmission (Back to Back)	107	Figure 17-8:	SPI Mode Timing	178
Figure 12-10:	USART Receive Block Diagram	108	Figure 17-9:	I ² C Bus Start/Stop Bits Timing	179
Figure 12-11:	Asynchronous Reception	108	Figure 17-10:	I ² C Bus Data Timing	180
Figure 12-12:	Synchronous Transmission	111	Figure 17-11:	A/D Conversion Timing	182
Figure 12-13:	Synchronous Transmission (Through TXEN)	111	Figure 18-1:	Load Conditions	188
Figure 12-14:	Synchronous Reception (Master Mode, SREN)	113	Figure 18-2:	External Clock Timing	189
Figure 13-1:	ADCON0 Register (Address 1Fh)	117	Figure 18-3:	CLKOUT and I/O Timing	190
Figure 13-2:	ADCON1 Register (Address 9Fh)	118	Figure 18-4:	Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing	191
Figure 13-3:	A/D Block Diagram	119	Figure 18-5:	Timer0 and Timer1 External Clock Timings	192
Figure 13-4:	Analog Input Model	120	Figure 18-6:	Capture/Compare/PWM Timings (CCP1 and CCP2)	193
Figure 13-5:	A/D Transfer Function	125	Figure 18-7:	Parallel Slave Port Timing (PIC16C74)	194
Figure 13-6:	Flowchart of A/D Operation	126	Figure 18-8:	SPI Mode Timing	195
Figure 14-1:	Configuration Word for PIC16C73/74	129	Figure 18-9:	I ² C Bus Start/Stop Bits Timing	196
Figure 14-2:	Configuration Word for PIC16C72/73A/74A/76/77	130	Figure 18-10:	I ² C Bus Data Timing	197
Figure 14-3:	Crystal/Ceramic Resonator Operation (HS, XT or LP OSC Configuration)	131	Figure 18-11:	USART Synchronous Transmission (Master/Slave) Timing	198
Figure 14-4:	External Clock Input Operation (HS, XT or LP OSC Configuration)	131	Figure 18-12:	USART Synchronous Receive (Master/Slave) Timing	198
Figure 14-5:	External Parallel Resonant Crystal Oscillator Circuit	132	Figure 18-13:	A/D Conversion Timing	200
Figure 14-6:	External Series Resonant Crystal Oscillator Circuit	132	Figure 19-1:	Load Conditions	206
Figure 14-7:	RC Oscillator Mode	132	Figure 19-2:	External Clock Timing	207
Figure 14-8:	Simplified Block Diagram of On-chip Reset Circuit	133	Figure 19-3:	CLKOUT and I/O Timing	208
Figure 14-9:	Brown-out Situations	134	Figure 19-4:	Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing	209
Figure 14-10:	Time-out Sequence on Power-up (MCLR not Tied to VDD): Case 1	139	Figure 19-5:	Brown-out Reset Timing	209
Figure 14-11:	Time-out Sequence on Power-up (MCLR Not Tied To VDD): Case 2	139	Figure 19-6:	Timer0 and Timer1 External Clock Timings	210
Figure 14-12:	Time-out Sequence on Power-up (MCLR Tied to VDD)	139	Figure 19-7:	Capture/Compare/PWM Timings (CCP1 and CCP2)	211
Figure 14-13:	External Power-on Reset Circuit (for Slow VDD Power-up)	140	Figure 19-8:	Parallel Slave Port Timing (PIC16C74A)	212
Figure 14-14:	External Brown-out Protection Circuit 1	140	Figure 19-9:	SPI Mode Timing	213
Figure 14-15:	External Brown-out Protection Circuit 2	140	Figure 19-10:	I ² C Bus Start/Stop Bits Timing	214
Figure 14-16:	Interrupt Logic	142	Figure 19-11:	I ² C Bus Data Timing	215
Figure 14-17:	INT Pin Interrupt Timing	142	Figure 19-12:	USART Synchronous Transmission (Master/Slave) Timing	216
Figure 14-18:	Watchdog Timer Block Diagram	144	Figure 19-13:	USART Synchronous Receive (Master/Slave) Timing	216
Figure 14-19:	Summary of Watchdog Timer Registers	144	Figure 19-14:	A/D Conversion Timing	218
Figure 14-20:	Wake-up from Sleep Through Interrupt	146	Figure 20-1:	Load Conditions	225
Figure 14-21:	Typical In-Circuit Serial Programming Connection	146	Figure 20-2:	External Clock Timing	226
Figure 15-1:	General Format for Instructions	147	Figure 20-3:	CLKOUT and I/O Timing	227
Figure 17-1:	Load Conditions	172	Figure 20-4:	Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing	228
Figure 17-2:	External Clock Timing	173	Figure 20-5:	Brown-out Reset Timing	228
Figure 17-3:	CLKOUT and I/O Timing	174	Figure 20-6:	Timer0 and Timer1 External Clock Timings	229
			Figure 20-7:	Capture/Compare/PWM Timings (CCP1 and CCP2)	230
			Figure 20-8:	Parallel Slave Port Timing (PIC16C77)	231

PIC16C6X

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (602) 786-7578.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager
RE: Reader Response
Total Pages Sent _____
From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: **PIC16C6X**

Literature Number: **DS30390E**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?
