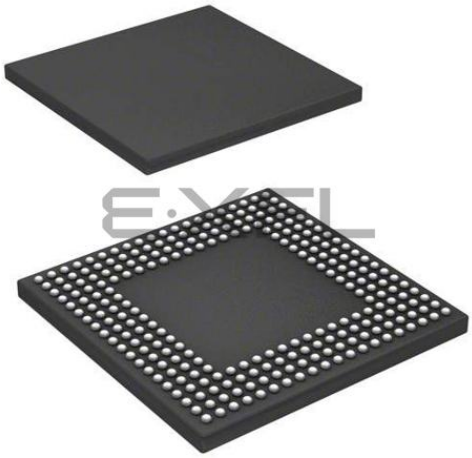

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Program Memory Type	ROMless
EEPROM Size	-
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If the delay slot instruction has a second data transfer, two checks are performed in step 2, as in the above case (Instructions that make two accesses to memory).

If the accepted exception (the highest-priority exception) is a delay slot instruction re-execution type exception, the branch instruction PR register write operation (PC → PR operation performed in a BSR, BSRF, or JSR instruction) is not disabled.

8.6 Usage Notes

1. Return from exception handling
   A. Check the BL bit in SR with software. If SPC and SSR have been saved to external memory, set the BL bit in SR to 1 before restoring them.
   B. Issue an RTE instruction. When RTE is executed, the SPC contents are saved in PC, the SSR contents are saved in SR, and branch is made to the SPC address to return from the exception handling routine.
2. If an exception or interrupt occurs when BL bit in SR = 1
   A. Exception

      When an exception other than a user break occurs, a manual reset is executed. The value in EXPEVT at this time is H'0000 0020; the SPC and SSR contents are undefined.
   B. Interrupt

      If an ordinary interrupt occurs, the interrupt request is held pending and is accepted after the BL bit in SR has been cleared to 0 by software. If a nonmaskable interrupt (NMI) occurs, it can be held pending or accepted according to the setting made by software.

      In sleep or standby mode, however, an interrupt is accepted even if the BL bit in SR is set to 1.
3. SPC when an exception occurs
   A. Re-execution type exception

      The PC value for the instruction at which the exception occurred is set in SPC, and the instruction is re-executed after returning from the exception handling routine. If an exception occurs in a delay slot instruction, however, the PC value for the delay slot instruction is saved in SPC regardless of whether or not the preceding delay slot instruction condition is satisfied.
   B. Completion type exception or interrupt

      The PC value for the instruction following that at which the exception occurred is set in SPC. If an exception occurs in a branch instruction with delay slot, however, the PC value for the branch destination is saved in SPC.
4. An exception must not be generated in an RTE instruction delay slot, as the operation cannot be guaranteed in this case.

Bit	Bit Name	Initial Value	R/W	Description
7	A6BST2	0	R/W	Area 6 Burst ROM Control
6	A6BST1	0	R/W	These bits specify whether burst ROM interface is used in area 6. When burst ROM interface is used, they also specify the number of accesses in a burst. When area 6 is an MPX interface area, the settings of these bits are ignored. When area 6 is used as a PCMCIA area, these bits should be cleared to 0. 000: Area 6 is accessed as SRAM interface. 001: Area 6 is accessed as burst ROM interface (4 consecutive accesses). Can be used with 8-, 16-, or 32-bit bus width 010: Area 6 is accessed as burst ROM interface (8 consecutive accesses). Can be used with 8-, 16-, or 32-bit bus width 011: Area 6 is accessed as burst ROM interface (16 consecutive accesses). Can only be used with 8- or 16-bit bus width. The setting of 32-bit bus width is prohibited. 100: Area 6 is accessed as burst ROM interface (32 consecutive accesses). Can only be used with 8-bit bus width 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
5	A6BST0	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
28 27 26	A6B2 A6B1 A6B0	1 1 1	R/W R/W R/W	Area 6 Burst Pitch These bits specify the number of wait cycles to be inserted for the second and following data accesses in burst transfer when area 6 is specified as burst ROM area. 000: Inserted wait cycles: 0, $\overline{RDY}$ pin: Disabled 001: Inserted wait cycles: 1, $\overline{RDY}$ pin: Enabled 010: Inserted wait cycles: 2, $\overline{RDY}$ pin: Enabled 011: Inserted wait cycles: 3, $\overline{RDY}$ pin: Enabled 100: Inserted wait cycles: 4, $\overline{RDY}$ pin: Enabled 101: Inserted wait cycles: 5, $\overline{RDY}$ pin: Enabled 110: Inserted wait cycles: 6, $\overline{RDY}$ pin: Enabled 111: Inserted wait cycles: 7, $\overline{RDY}$ pin: Enabled
25 24 23	A5W2 A5W1 A5W0	1 1 1	R/W R/W R/W	Area 5 Wait Control These bits specify the number of wait cycles to be inserted for area 5. For the case where an MPX interface setting is made, see table 10.7. 000: Inserted wait cycles: 0, $\overline{RDY}$ pin: Disabled 001: Inserted wait cycles: 1, $\overline{RDY}$ pin: Enabled 010: Inserted wait cycles: 2, $\overline{RDY}$ pin: Enabled 011: Inserted wait cycles: 3, $\overline{RDY}$ pin: Enabled 100: Inserted wait cycles: 6, $\overline{RDY}$ pin: Enabled 101: Inserted wait cycles: 9, $\overline{RDY}$ pin: Enabled 110: Inserted wait cycles: 12, $\overline{RDY}$ pin: Enabled 111: Inserted wait cycles: 15, $\overline{RDY}$ pin: Enabled

Bit	Bit Name	Initial Value	R/W	Description
15 14 13	A3W2 A3W1 A3W0	1 1 1	R/W R/W R/W	Area 3 Wait Control These bits specify the number of wait cycles to be inserted for area 3. An external wait input is available for SRAM and MPX interfaces and is not available for synchronous DRAM interface. For the case where an MPX interface setting is made, see table 10.7. • When SRAM interface is in use: Inserted wait cycles / $\overline{RDY}$ pin 000: 0 — Disabled 001: 1 — Enabled 010: 2 — Enabled 011: 3 — Enabled 100: 6 — Enabled 101: 9 — Enabled 110: 12 — Enabled 111: 15 — Enabled • When synchronous DRAM interface is in use*[1]: Synchronous DRAM $\overline{CAS}$ latency cycles 000: Setting prohibited 001: 1*[2] 010: 2 011: 3 100: 4*[2] 101: 5*[2] 110: Setting prohibited 111: Setting prohibited
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

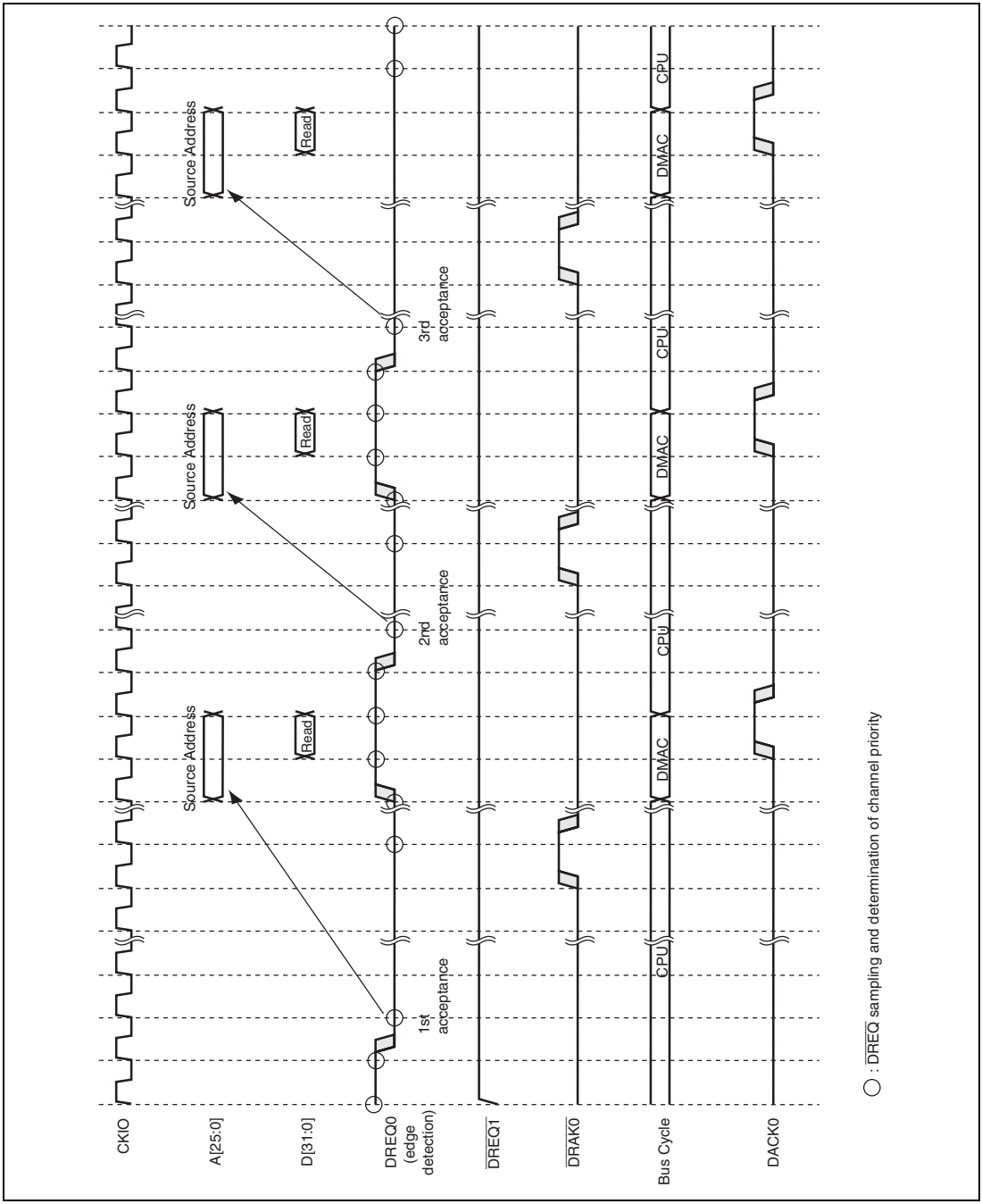

Figure 11.24 Single Address Mode/Cycle Steal Mode in DMABRG Mode External Bus → External Device/ DREQ (Edge Detection)

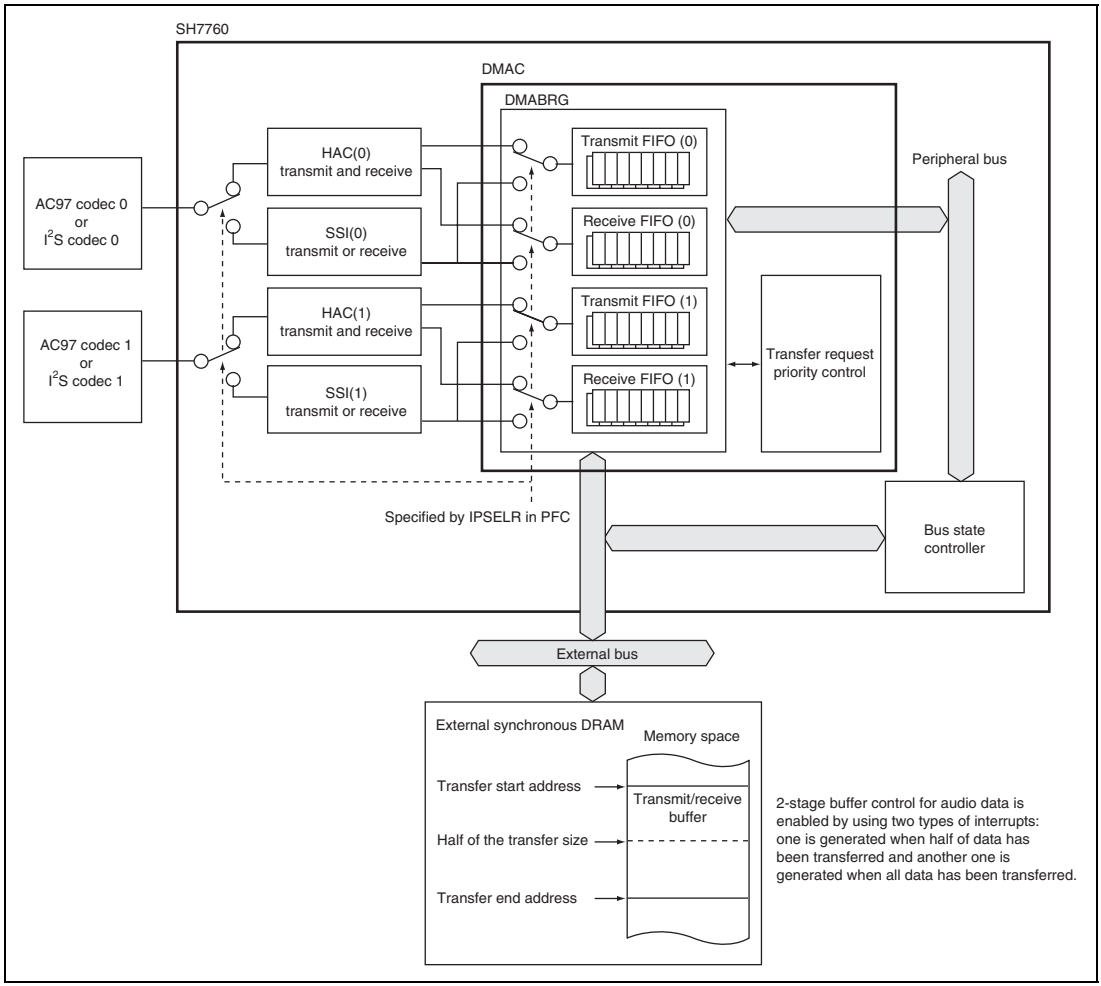

Figure 11.31 Configuration of DMA for HAC/SSI

Bit	Bit Name	Initial Value	R/W	Description
6	RDRF	0	R/W	Receive Data Register Full Indicates that received data is stored in SIRDR*[1]. 0: Indicates that no valid received data is stored in SIRDR. [Clearing Conditions] • On reset • When data is read from SIRDR • When 0 is written to the RDRF bit 1: Indicates that valid received data is stored in SIRDR. [Setting Condition]*[2] • When serial reception is completed normally, and received data is transferred from SIRSR to SIRDR. Notes: 1. In the T = 0 mode, when the receiver detects a parity error, it retains the previous state without affecting the SIRDR contents and RDRF flag. On the other hand, in the T = 1 mode, when the receiver detects a parity error, it transfers the received data to SIRDR, and sets the RDRF flag to 1. In both the T = 0 and T = 1 modes, clearing the RE bit in SISCR to 0 will retain the previous state without affecting the SIRDR contents and RDRF flag. 2. Writing 1 will retain the original value.

(2) Slave Transmitter

This mode cannot be used.

(3) Master Receiver

This mode allows the SSI module to receive a serial bit stream from another device and store it in memory.

The shift register clock can be supplied from an external device or from an internal clock.

The word select pin is used as an output flow control. The module always asserts the word select signal to indicate it can receive more data continuously. It is the responsibility of the host CPU to ensure it can transmit data to the SSI module in time to ensure no data is lost.

(4) Master Transmitter

This mode allows the module to transmit a serial bit stream from internal memory to another device.

The shift register clock can be supplied from an external device or from an internal clock.

The word select pin is used as an output flow control. The module always asserts the word select signal to indicate it will transmit more data continuously. Word select signal is not asserted until the first word is ready to transmit however. It is the responsibility of the receiving device to ensure it can receive the serial data in time to ensure no data is lost.

When the configuration for data transfer is completed, the SSI module can work with the minimum interaction with CPU. The CPU specifies settings for the SSI module and DMAC then handles overflow/ underflow interrupts if required.

20.4.4 Operation Modes

There are three modes of operation: configuration, enabled and disabled. Figure 20.20 shows the transition diagram between these operation modes.

(1) Reception Using DMA Controller

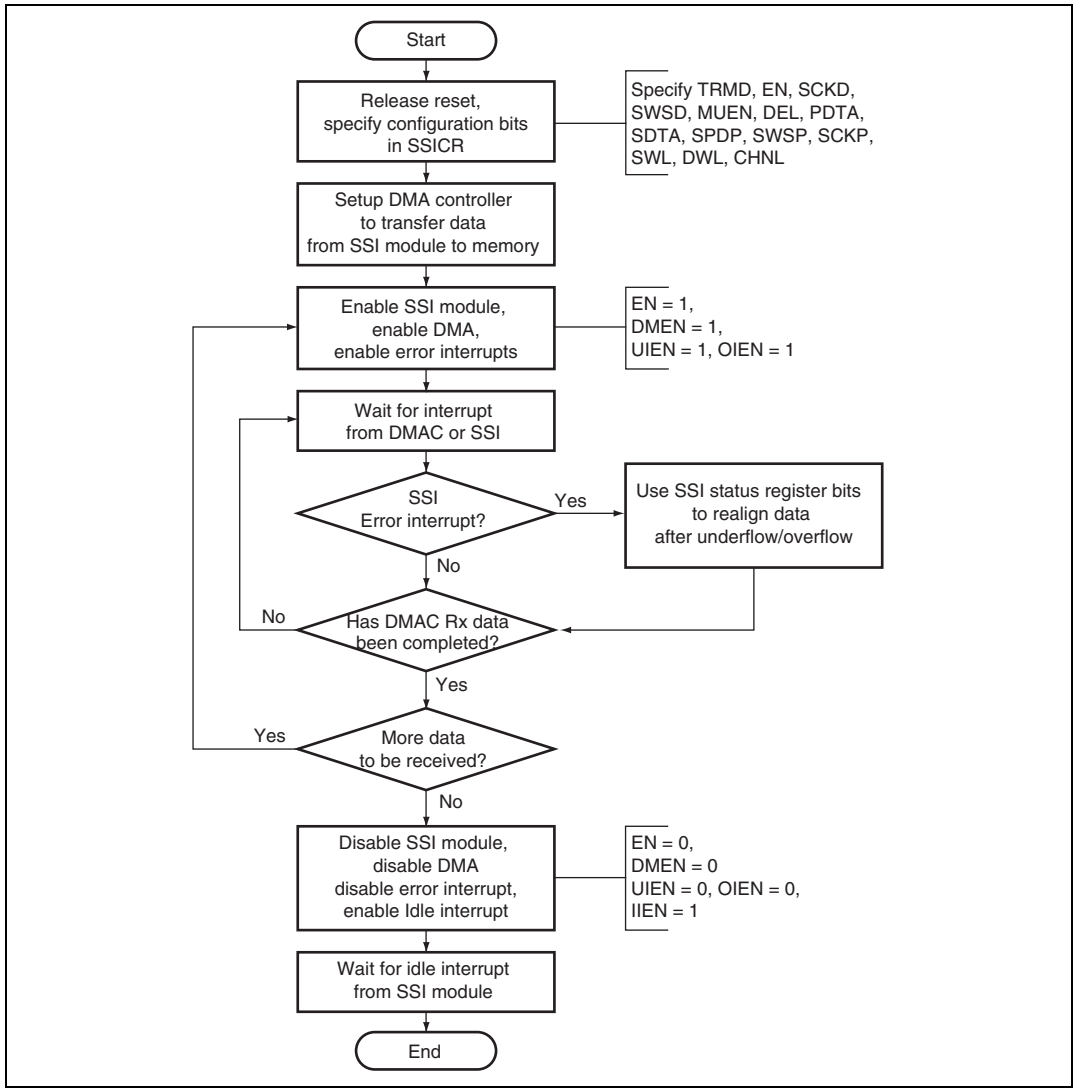

Figure 20.23 Reception using DMA Controller

Bit	Bit Name	Initial Value	R/W	Description
12	IRR12	0	R/W	Wake-up on Bus Activity Indicates that a CAN bus activity is present. When the HCAN is in sleep mode and a recessive to dominant bit transition takes place on the CAN bus, this bit is set. The operation of this interrupt is configured in the Master Control Register. (MCR7 – Auto-wake Mode). This interrupt is cleared by writing a 1 to this bit position. Writing a 0 has no effect. 0: Bus idle state Clearing condition: Write a 1 to this bit. 1: CAN bus activity is detected in HCAN2 sleep mode. Setting condition: Bit transition, from recessive to dominant, is detected in sleep mode.
11, 10	—	All 0	R	Reserved The write value should always be 0. The read value is not guaranteed.
9	IRR9	0	R/W	Message Overrun/Overwrite Interrupt Flag Indicates that a message has been received but the existing message in the matching Mailbox has not been read due to the corresponding CANRXPR or CANRFPR set to 1. The received message is either abandoned (overrun) or overwritten depeding on the value of the NMC (New Message Control) bit. This bit is cleared by writing a 1 to the correspondent bit position in CANUMSR (Unread Message Status Register). Writing a 0 has no effect. 0: No message overrun/overwrite Clearing condition: Clean all bits in CANUMSR. 1: Receive message overrun and its storage has been rejected or message overwrite. Setting condition: Message is received while the corresponding CANRXPR or CANRFPR =1 and CANMBIMR = 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	ABACK1[15:0]	All 0	R/W*	Notifies that requested transmission cancellation requested of the corresponding Mailbox has been performed successfully. Bits 15 to 0 correspond to Mailboxes 31 to 16 respectively. 0: Clearing condition: Write a 1 to this bit. 1: Corresponding Mailbox has cancelled transmission of message (Data or Remote Frame). Setting condition: Completion of transmission cancellation for the corresponding Mailbox

Note: * Only a write of 1 is allowed to clear the bit.

- CANABACK0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ABACK0_15	ABACK0_14	ABACK0_13	ABACK0_12	ABACK0_11	ABACK0_10	ABACK0_9	ABACK0_8	ABACK0_7	ABACK0_6	ABACK0_5	ABACK0_4	ABACK0_3	ABACK0_2	ABACK0_1	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	ABACK0[15:1]	All 0	R/W*	Notifies that requested transmission cancellation requested of the corresponding Mailbox has been performed successfully. Bits 15 to 1 correspond to Mailboxes 15 to 1 respectively. 0: Clearing condition: Write a 1 to this bit. 1: Corresponding Mailbox has cancelled transmission of message (Data or Remote Frame). Setting condition: Completion of transmission cancellation for the corresponding Mailbox
0	—	0	R	Reserved This bit is always 0 as this is receive-only. Writing a 1 to this bit has no effect. This bit is always read as 0.

Note: * Only a write of 1 is allowed to clear the bit.

Figure 23.1 is a block diagram of the HSPI.

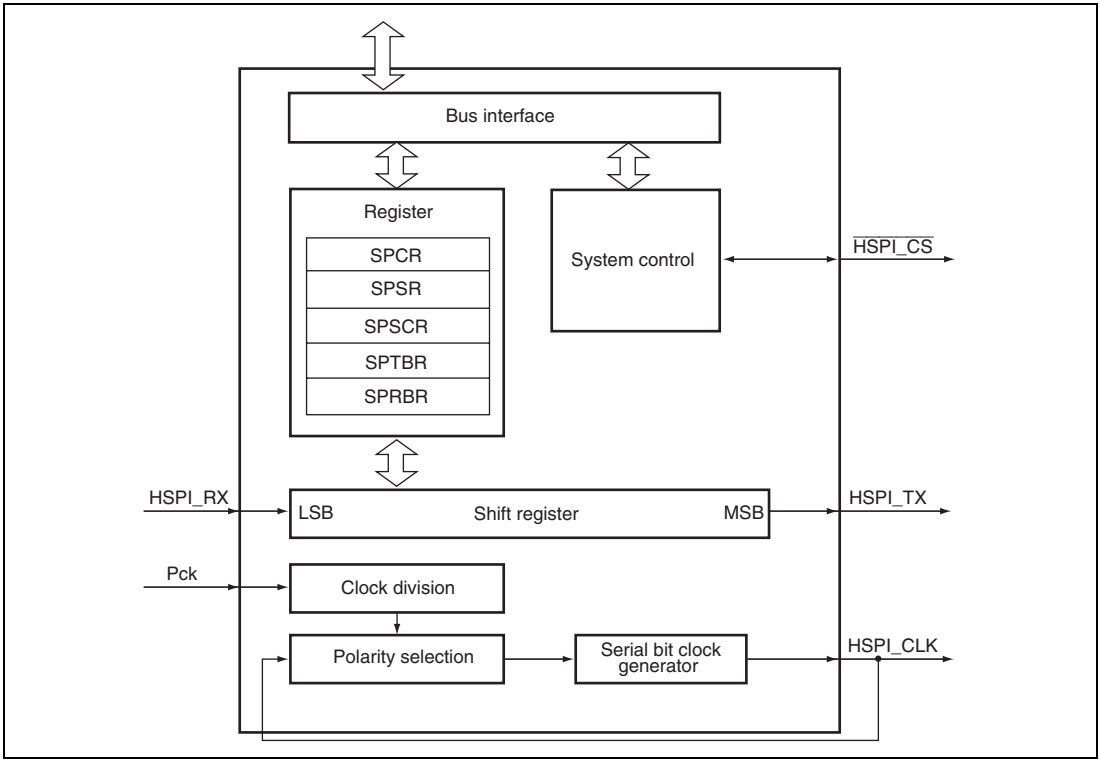

Figure 23.1 Block Diagram of HSPI

23.2 Input/Output Pins

The input/output pins of the HSPI is shown in table 23.1.

Table 23.1 Pin Configuration

Name	Abbreviation	I/O	Function
Serial bit clock pin	HSPI_CLK	Input/Output	Clock input/output
Transmit data pin	HSPI_TX	Output	Transmit data output
Receive data pin	HSPI_RX	Input	Receive data input
Chip select pin	$\overline{\text{HSPI\_CS}}$	Input/Output	Chip select

23.3.3 System Control Register (SPSCR)

SPSCR is a 32-bit readable/writable register that enables or disables interrupts or FIFO mode, selects either LSB first or MSB first in transmitting/receiving date, and master or slave mode.

If any of the FFEN, LMSB, CSA or MASL bit values are changed, then the module will undergo the HSPI software reset.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	TEIE	THIE	RNIE	RHIE	RFIE	FFEN	LMSB	CSV	CSA	TFIE	ROIE	RXDE	TXDE	MASL
Initial value:	-	-	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All —	R	Reserved These bits are always read as an undefined value. The write value should always be 0.
13	TEIE	0	R/W	Transmit FIFO Empty Interrupt Enable 0:Transmit FIFO empty interrupt disabled 1:Transmit FIFO empty interrupt enabled
12	THIE	0	R/W	Transmit FIFO Halfway Interrupt Enable 0:Transmit FIFO halfway interrupt disabled 1:Transmit FIFO halfway interrupt enabled
11	RNIE	0	R/W	Receive FIFO Not Empty Interrupt Enable 0: Receive FIFO not empty interrupt disabled 1: Receive FIFO not empty interrupt enabled
10	RHIE	0	R/W	Receive FIFO Halfway Interrupt Enable 0: Receive FIFO halfway interrupt disabled 1: Receive FIFO halfway interrupt enabled
9	RFIE	0	R/W	Receive FIFO Full Interrupt Enable 0: Receive FIFO full interrupt disabled 1: Receive FIFO full interrupt enabled

Bit	Bit Name	Initial value	R/W	Description
1	PF0MD1	0	R/W	PTF0 Mode
0	PF0MD0	0	R/W	00: Peripheral module (HSPI/MMCIF/SIM) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)

24.2.7 Port G Control Register (PGCR)

PGCR is a 16-bit readable/writable register that selects the pin function and input pull-up MOS control.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PG7 MD1	PG7 MD0	PG6 MD1	PG6 MD0	PG5 MD1	PG5 MD0	PG4 MD1	PG4 MD0	PG3 MD1	PG3 MD0	PG2 MD1	PG2 MD0	PG1 MD1	PG1 MD0	PG0 MD1	PG0 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
15	PG7MD1	0	R/W	PTG7 Mode
14	PG7MD0	0	R/W	00: Peripheral module (SCIF[0]) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)
13	PG6MD1	0	R/W	PTG6 Mode
12	PG6MD0	0	R/W	00: Peripheral module (SCIF[0]) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)
11	PG5MD1	0	R/W	PTG5 Mode
10	PG5MD0	0	R/W	00: Peripheral module (SCIF[0]) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)
9	PG4MD1	0	R/W	PTG4 Mode
8	PG4MD0	0	R/W	00: Peripheral module (SCIF[1]) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)

Bit	Bit Name	Initial value	R/W	Description
3	PJ1MD1	0	R/W	PTJ1 Mode
2	PJ1MD0	0	R/W	00: Peripheral module (DCK) 01: Port output Other than above: Setting prohibited
1, 0	—	All 0	R	Reserved These bits are always read as 0, and the write value should always be 0.

Note: *The following settings are prohibited: the combination of port3 set to output and port 4 to input or port3 to input and port4 to output.

24.2.10 Port K Control Register (PKCR)

PKCR is a 16-bit readable/writable register that selects the pin function and input pull-up MOS control.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PK7 MD1	PK7 MD0	PK6 MD1	PK6 MD0	PK5 MD1	PK5 MD0	PK4 MD1	PK4 MD0	PK3 MD1	PK3 MD0	PK2 MD1	PK2 MD0	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial value	R/W	Description
15	PK7MD1	0	R/W	PTK7 Mode
14	PK7MD0	0	R/W	00: Peripheral module (Reserved/AUD) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)
13	PK6MD1	0	R/W	PTK6 Mode
12	PK6MD0	0	R/W	00: Peripheral module (Reserved/AUD) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)
11	PK5MD1	0	R/W	PTK5 Mode
10	PK5MD0	0	R/W	00: Peripheral module (Reserved/AUD) 01: Port output 10: Port input (pull-up MOS: Off) 11: Port input (pull-up MOS: On)

28.4 Operation

28.4.1 TAP Control

Figure 28.2 shows the internal states of TAP controller. The state transitions conform to the JTAG standards.

- State transitions occur according to the TMS value at the rising edge of a TCK signal.
- The TDI value is sampled at the rising edge of a TCK signal and shifted at the falling edge of a TCK signal.
- The TDO value is changed at the falling edge of a TCK signal. The TDO signal is in a Hi-Z state other than in the Shift-DR or Shift-IR state.
- Clearing $\overline{\text{TRST}}$ to 0 places the TAP controller into the Test-Logic-Reset state asynchronously with a TCK signal.

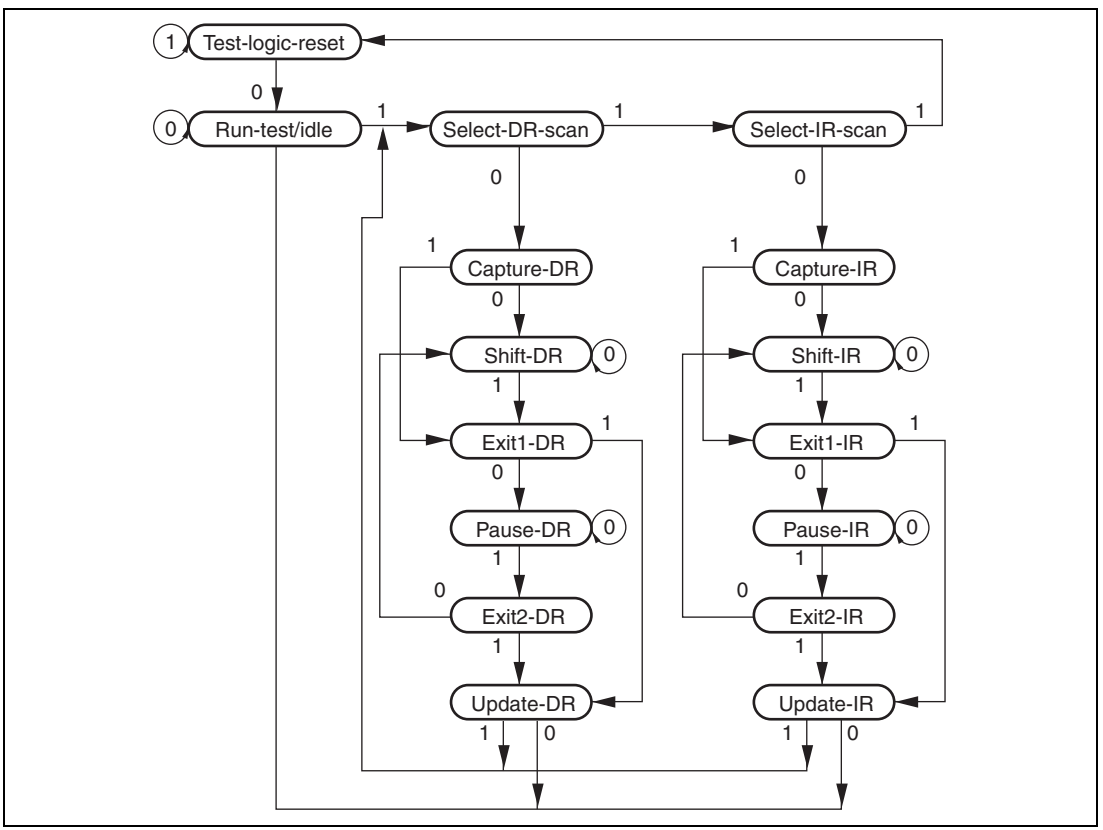

Figure 28.2 TAP Controller State Transitions

Section 30 LCD Controller (LCDC)

A unified memory architecture is adopted for the LCD controller (LCDC) so that the image data for display is stored in system memory. The LCDC module reads data from system memory, uses the palette memory to determine the colors, then puts the display on the LCD panel. It is possible to connect the LCDC to the LCD module of most types other than microcomputer bus interface types and NTSC/PAL types and those that apply the LVDS interface.

30.1 Features

The LCDC has the following features.

- Panel interface
  - Serial interface method
  - Supports data formats for STN/dual-STN/TFT panels (8/12/16/18-bit bus width) *[1]
- Supports 4/8/15/16-bpp (bits per pixel) color modes
- Supports 1/2/4/6-bpp grayscale modes
- Supports LCD-panel sizes from 16 × 1 to 1024 × 1024*[2]
- 24-bit color palette memory (16 of the 24 bits are valid; R:5/G:6/B:5)
- STN/DSTN panels are prone to flicker and shadowing. The controller applies 65536-color control by 24-bit space-modulation FRC with 8-bit RGB values for reduced flicker.
- Dedicated display memory is unnecessary using part of the SDRAM connected to area 3 of the CPU as system memory.
- The display is stable because of the large 2.4-kbyte line buffer
- Supports the inversion of the output signal to suit the LCD panel's signal polarity
- Supports the selection of data formats (the endian setting for bytes, backed pixel method) by register settings
- A hardware-rotation mode is included to support the use of landscape-format LCD panels as portrait-format LCD panels (the horizontal width of the panel before rotation must be within 320 pixels—see table 30.4).

Notes: 1. When connecting the LCDC to a TFT panel with an unwired 18-bit bus, the lower bit lines should be connected to GND or to the lowest bit from which data is output.
2. For details, see section 30.4.1, Size of LCD Modules Which Can Be Displayed with this LCDC.

Abbrev.	Bit 31/ 23/15/7	Bit 30/ 22/14/6	Bit 29/ 21/13/5	Bit 28/ 20/12/4	Bit 27/ 19/11/3	Bit 26/ 18/10/2	Bit 25/ 17/9/ 1	Bit 24/ 16/8/0	Module
DMAARXTCNT0	—	—	—	—	—	—	—	—	DMAC
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
DMAATXSAR1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
DMAARXDAR1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
DMAATXTCR1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
DMAARXTCR1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
DMAACR1	—	—	—	—	—	—	RAM1	RAM0	
	—	—	—	—	—	RAR	RDS	RDE	
	—	—	—	—	—	—	TAM1	TAM0	
	—	—	—	—	—	TAR	TDS	TDE	
DMAATXTCNT1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
DMAARXTCNT1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	

Abbrev.	Bit 31/ 23/15/7	Bit 30/ 22/14/6	Bit 29/ 21/13/5	Bit 28/ 20/12/4	Bit 27/ 19/11/3	Bit 26/ 18/10/2	Bit 25/ 17/9/ 1	Bit 24/ 16/8/0	Module
SSIRDR0	—	—	—	—	—	—	—	—	SSI(0)
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
SSICR1	—	—	—	DMEN	UIEN	OIEN	IIEN	DIEN	SSI(1)
	CHNL1	CHNL0	DWL2	DWL1	DWL0	SWL2	SWL1	SWL0	
	SCKD	SWSD	SCKP	SWSP	SPDP	SDTA	PDTA	DEL	
	BREN	CKDV	CKDV	CKDV	MUEN	CPEN	TRMD	EN	
SSISR1	—	—	—	DMRQ	UIRQ	OIRQ	IIRQ	DIRQ	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	CHNO1	CHNO0	SWNO	IDST	
SSITDR1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
SSIRDR1	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
HcRevision	—	—	—	—	—	—	—	—	USB
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	REV	REV	REV	REV	REV	REV	REV	REV	
HcControl	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	RWE	RWC	IR	
	HCFS1	HCFS0	BLE	CLE	IE	PLE	CBSR1	CBSR0	
HcCommand status	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	SOC1	SOC0	
	—	—	—	—	—	—	—	—	
	—	—	—	—	OCR	BLF	CLF	HCR	

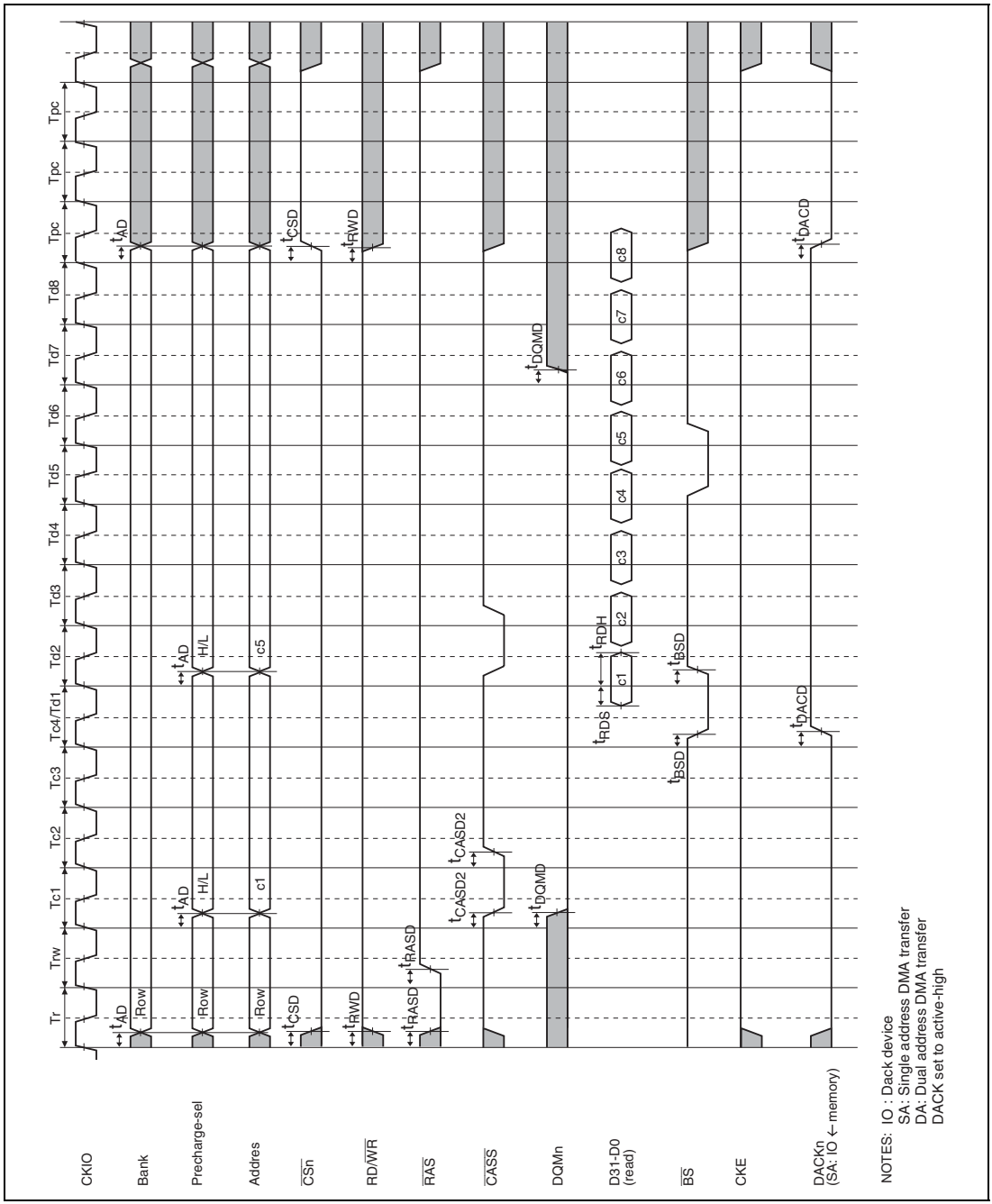

Figure 33.26 Synchronous DRAM Auto-Precharge Read Bus Cycle: Burst (RCD[1:0] = 01, CAS Latency = 3, TPC[2:0] = 011)