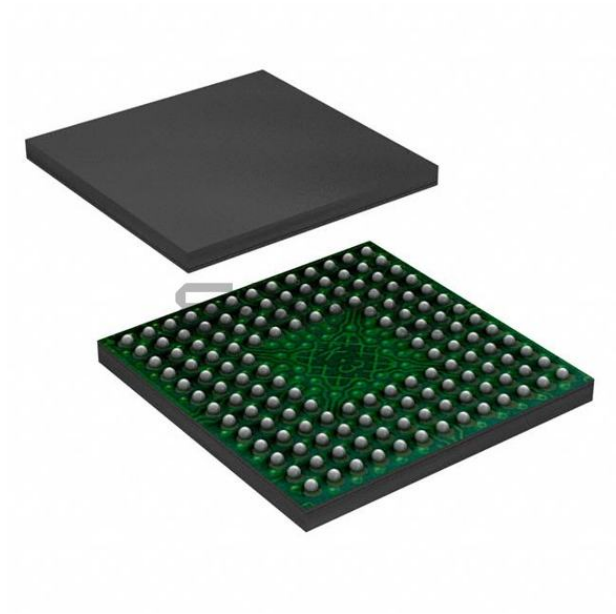

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Fingerprint Authentication
Core Processor	ARM7TDMI
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	16K x 8
Interface	EBI/EMI, SmartCard, SPI, SSIO, UART/USART, USB
Number of I/O	3
Voltage - Supply	2.25V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml67q5250-nnnlagz3a

• Internal RAM
- Working RAM for CPU : 16 Kbytes

• Internal Flash ROM
- 128 Kbyte Flash ROM
- Program ROM : 64 Kbytes
  This program ROM includes drivers for fingerprint authentication and peripherals.
  Erase/rewrite times : 100 max.
- Data ROM for storing fingerprint data : 64 Kbytes
  Erase/rewrite times : 10,000 max. (when enrolling one fingerprint data)

• External memory controller
- ROM/Flash
  • 1 bank x 4 Mbytes
  • Supports 16-bit devices
  • Bootable from external ROM/Flash
    This function can not be used during security function being activated.
- SRAM
  • 1 bank × 4 Mbytes
  • Supports 16-bit devices
- External I/O
  • 2-bank × 4 Mbytes
  • Supports 8-bit/16-bit devices
  • Enable to set address setup, RW/WE pulse, and data off timing in system clock cycle unit
  • Supports an access wait function by wait signal

• Interrupt control
- FIQ: 1 interrupt source
- IRQ: 22 interrupt sources
  7 priority levels can be set for each source.

• DMA controller (DMAC)
- 2 channels
- Enable to allocate multiple DMA transfer request sources for each channel.
- Channel priority: fixed mode/round robin mode
- DMA transfer mode: cycle steal mode/burst mode
- DMA request type: software requests/hardware requests
- Maximum transfer count : 65,536
- Data transfer size: 8 bits/16 bits/32 bits
- Transfer request source: CPU, SPI, Synchronous SIO, Smartcard IF

- GPIO
  - 13 bits × 1 channel, 14 bits × 1 channel, and 16 bits × 1 channel
  - Enable to setting input mode or output mode for each bit
  - Enable to setting as interruption source for each bit
  - Interruption mode: level/edge and positive logic/negative logic

- System timer
  - 16-bit auto reload timer × 1 channel

- Flexible timer (FTM)
  - 16-bit timer × 3 channels
  - Operating mode
    Auto reload timer (ART) /Compare Out (CMO) /pulse width modulation (PWM) /capture (CAP) mode.

- Watch dog timer (WDT)
  - 16-bits timer
  - 8.389 seconds max. (when CPU operating frequency is 32 MHz)
  - Enables generation of interrupt or reset by setting

- SIO (UART)
  - Full-duplex asynchronous mode
  - Built-in baud rate generator

- SPI
  - 2 channels of full-duplex serial peripheral interfaces
  - Operating mode: master mode/slave mode
  - Data transfer size: 8 bits (byte) / 16 bits (word)
  - Built-in 16-byte/16-word FIFO on the transmission side and the reception side
  - Supports DMA transfer (master/slave mode)

- Synchronous SIO (SSIO)
  - 8-bit clock synchronous serial port × 1 channel
  - Selectable clock polarity
  - Selectable LSB first or MSB first
  - Operation mode: master mode/slave mode
  - Supports DMAC transfer (in master mode only)

- Smart Card interface (Smartcard IF)
  - ISO UART × 1 channel
  - Built-in 16-byte FIFO
  - Built-in parity error counter in receive mode and transmit mode at automatic retransmission
  - Supports asynchronous protocol of T = 0 and T = 1 according to ISO7816 and EMV
  - Built-in error detection code generation and error detection functions by hardware
  - Supports DMA transfer

- USB2.0 full-speed device
  - Compliant with Universal Serial Bus (USB) 2.0
  - Full speed (12 Mbps) × 1 port.
  - End points: 5 or 6
  - Supports all data transfer types (control transfer, bulk transfer, interrupt transfer, isochronous transfer).
  - Built-in SOF generation and CRC5/16 generation functions
  - Access size to data transfer FIFOs: 8 bits/16 bits/32 bits

BLOCK DIAGRAM

Figure 1 shows a block diagram of this LSI.

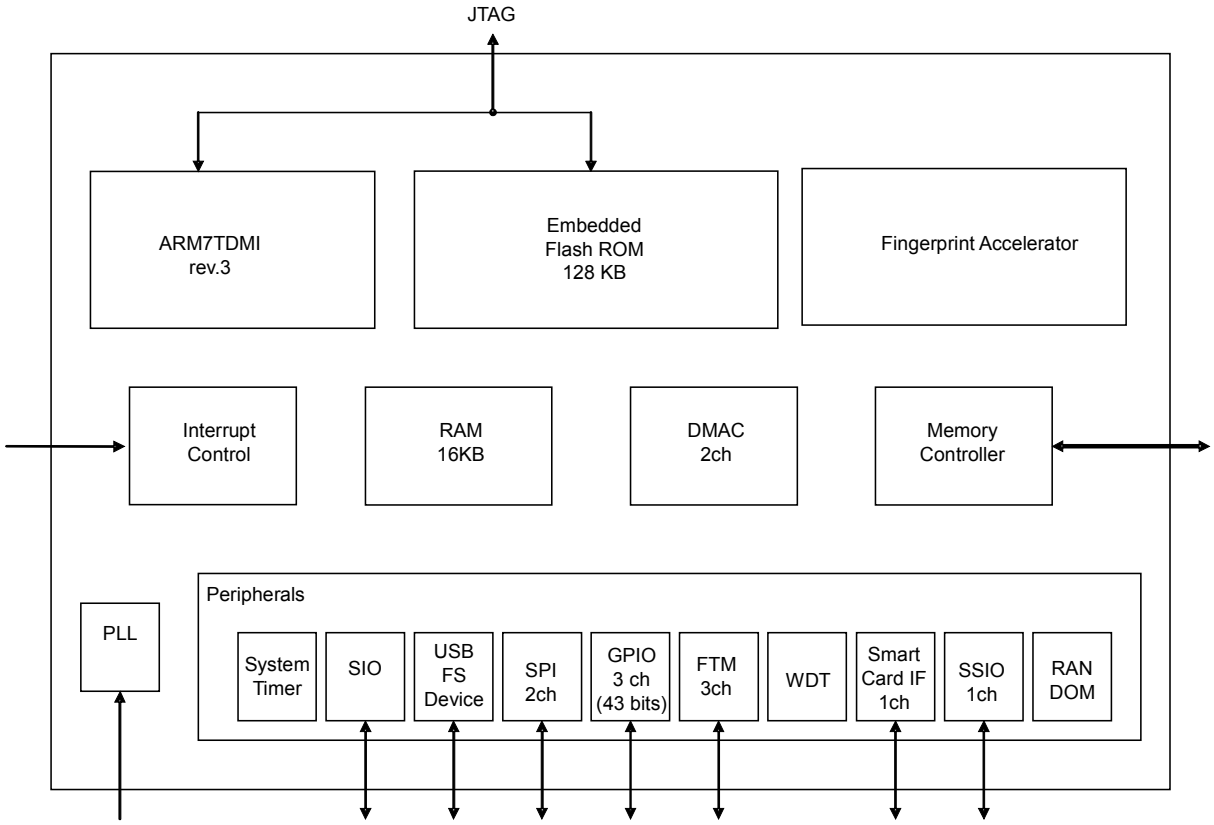


Figure 1 Block Diagram

Pin List

Pin No.	Pin name	I/O	Polarity (*2)	Description		Schmitt	PU/PD (*1)	Drive capability	5V Tolerant	Initial direction	Initial value
				Primary function	Secondary function						
	Clock										
E4	XI	—	—	Oscillation pin	—	—	—	—	—	I	—
E2	XO	—	—	Oscillation pin	—	—	—	—	—	O	—
	Reset										
D1	RESETN	I	N	System reset input	—	S	PU	4mA	—	I	—
	JTAG										
H10	JTAGE	I	P	JTAG enable	—	S	PD	4mA	—	I	—
	GPIO										
D5	PA13	I/O	P	General-purpose port A13	External interrupt input (Interrupt No. 30)	S	PD	4mA	—	I	—
A5	PA12	I/O	P	General-purpose port A12	Clock output (for sensor)	—	PD	4mA	—	I	—
A1	PA11	I	P	General-purpose port A11	External interrupt input (USB VBUS interrupt)	S	—	—	○	I	—
B1	PA10	I/O	P	General-purpose port A10	External interrupt input (Interrupt No. 28)	S	PD	4mA	—	I	—
C1	PA09	I/O	P	General-purpose port A9	External interrupt input (Interrupt No. 26)	S	PD	4mA	—	I	—
D3	PA08	I/O	P	General-purpose port A8	External FIQ interrupt input	S	PD	4mA	—	I	—
F2	PA07	I/O	P	General-purpose port A7	—	—	PD	4mA	—	I	—
F4	PA06	I/O	P	General-purpose port A6	Smartcard IF clock	—	PD	4mA	—	I	—
G4	PA05	I/O	P	General-purpose port A5	Smartcard IF reset	—	PD	4mA	—	I	—
G3	PA04	I/O	P	General-purpose port A4	Smartcard IF serial data	—	PD	4mA	—	I	—
G1	PA03	I/O	P	General-purpose port A3	Smartcard IF power control	—	PD	4mA	—	I	—
H1	PA02	I/O	P	General-purpose port A2	Smartcard IF voltage control 1	—	PD	4mA	—	I	—
J4	PA01	I/O	P	General-purpose port A1	Smartcard IF voltage control 0	—	PD	4mA	—	I	—
K2	PA00	I/O	P	General-purpose port A0	Smartcard IF card detection	—	PD	4mA	—	I	—
K8	PB12	I/O	P	General-purpose port B12	SIO receive data input	—	PD	4mA	—	I	—
M8	PB11	I/O	P	General-purpose port B11	SIO transmit data output	—	PD	4mA	—	I	—
M10	PB10	I/O	P	General-purpose port B10	FTM2 FTMIN[2]/FTMOUT[2] INOUT	—	PD	4mA	—	I	—
N10	PB09	I/O	P	General-purpose port B09	FTM1 FTMCLK[1] IN/FTMIN[1]/FTMOUT[1] INOUT	—	PD	4mA	—	I	—
L11	PB08	I/O	P	General-purpose port B08	FTM0 FTMCLK[0] IN/FTMIN[0]/FTMOUT[0] INOUT	—	PD	4mA	—	I	—
L13	PB07	I/O	P	General-purpose port B07	JTAG clock	S	PD	4mA	—	I	—

Pin No.	Pin name	I/O	Polarity (*2)	Description		Schmitt	PU/PD (*1)	Drive capability	5V Tolerant	Initial direction	Initial value
				Primary function	Secondary function						
	For System										
F3	BOOTP	I	P	Boot device select 1	—	S	PU	4mA	—	I	—
	For Testing										
A13	TESTF	I	P	Test pin	—	—	—	—	—	I	—
N13	TEST0	I	P	Test mode select signal 0	—	S	PD	4mA	—	I	—
B13	TEST1	I	P	Test mode select signal 1	—	S	PD	4mA	—	I	—
D8	TEST2	I	P	Test mode select signal 2	—	S	PD	4mA	—	I	—
C6	TEST3	I	P	Test mode select signal 3	—	S	PD	4mA	—	I	—

*1: PU/PD column:
PU: Pulled up with a built-in resistor
PD: Pulled down with a built-in resistor
*2: Polarity column:
P: Positive
N: Negative

Other Pins (Power supply pins, Unused pins)

Pin name	Description	Pin No.	Pin count
VDDCORE	Core power supply	C3, L2, L7, K11, F13, B4	6
GNDCORE	Core GND	C2, M1, L8, K12, D12, C5	6
VDDIO	IO power supply	E1, J2, N1, N5, N7, N11, H13, E11, C9, C7, C4	11
GNDIO	IO GND	F1, J1, L3, M6, K9, M13, G12, D10, A8, B5, B2	11
PLLVDD	PLL power supply	E3	1
PLLGND	PLL GND	D2	1
N.C.	Unused pin	G2, H3, B3, D4	4

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage CORE (2.5V)	V_{DD_CORE}	—	–0.3 to +3.6	V
Digital power supply voltage I/O (3.3V)	V_{DD_IO}		–0.3 to +4.6	
Input voltage (normal buffer)	V_I		–0.3 to V_{DD_IO}+0.3	
Input voltage (5 V tolerant)		V_{DD_IO} = 3.0 V to 3.6 V	–0.3 to 6.0	
		V_{DD_IO} < 3.0 V	–0.3 to V_{DD_IO}+0.3	
Output voltage (normal buffer)	V_O	—	–0.3 to V_{DD_IO}+0.3	
Output voltage (5 V tolerant)		V_{DD_IO} = 3.0 V to 3.6 V	–0.3 to 6.0	
		V_{DD_IO} < 3.0 V	–0.3 to V_{DD_IO}+0.3	
PLL power supply voltage (PLL)	V_{DD_PLL}	—	–0.3 to +3.6	
Input allowable current	I_I		–10 to +10	mA
"H" output allowable current	I_{OH}		+14	
"L" output allowable current	I_{OL}		–14	
Power dissipation	P_D	Ta = 85°C (per package)	600	mW
Storage temperature	T_{STG}	—	–50 to 150	°C

Guaranteed Operating Ranges

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply voltage (CORE) (*1)	V_{DD_CORE}	—	2.25	2.5	2.75	V
Digital power supply voltage (I/O)	V_{DD_IO}		3.0	3.3	3.6	
PLL power supply voltage (PLL) (*1)	V_{DD_PLL}		2.25	2.5	2.75	
CPU operating frequency	f_{OSC}	—	—	32	—	MHz
Ambient temperature	Ta	Other than below	–40	25	85	°C
	$T_{a\_flwrite}$	- When enrolling fingerprints - When rewriting Flash memory	–40	25	70	°C

* 1: Please supply from same power source to both V_{DD_CORE} pins and V_{DD_PLL} pin.

– Internal Flash ROM

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Guaranteed ambient temperature for write operations	$T_{a\_flwrite}$	—	–40	25	70	°C
Guaranteed ambient temperature for read operations	T_{a_flread}	—	–40	25	85	
Flash write count	C_{WR_CODE}	Program code rewrite $T_{a\_flwrite}$ = –40 to +70°C	—	—	100	—
	C_{WR_DATA01}	Fingerprint template data rewrite (for 1-finger enrollment) $T_{a\_flwrite}$ = –40 to +70°C	—	—	10,000	—
	C_{WR_DATA15}	Fingerprint template data rewrite (for 15-finger enrollment) $T_{a\_flwrite}$ = –40 to +70°C	—	—	1,000	—

DC Characteristics

– DC characteristics (Core/IO)

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	2.0	—	V_{DD_IO} +0.3	V
"L" input voltage	V_{IL}	—	–0.3	—	0.8	V
Schmitt trigger input threshold voltage (3.3 V)	V_{T+}	—	—	—	$V_{DD\_IO} \times 0.7$	V
	V_{T-}	—	$V_{DD\_IO} \times 0.2$	—	—	V
	ΔV_T	$V_{T+} - V_{T-}$	$V_{DD\_IO} \times 0.1$	—	—	V
Schmitt trigger input threshold voltage (5 V tolerant)	V_{T+}	—	—	—	$V_{DD\_IO} \times 0.7$	V
	V_{T-}	—	$V_{DD\_IO} \times 0.2$	—	—	V
	ΔV_T	$V_{T+} - V_{T-}$	$V_{DD\_IO} \times 0.1$	—	—	V
"H" output voltage	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
High level input current (*1)	I_{IH}	$V_{IH} = V_{DD\_IO}$	—	—	10	µA
		$V_{IH} = V_{DD\_IO}$, 50 kΩ pull-down	10	66	200	µA
High level input current (*2)		$V_{IH} = V_{DD\_IO}$	—	—	10	µA
		V_{IH} = 5.5 V	—	—	10	µA
Low level input current (*1)	I_{IL}	V_{IL} = 0 V	–10	—	—	µA
		V_{IL} = 0 V, 50 kΩ pull-up	–200	–66	–10	µA
Low level input current (*2)		V_{IL} = 0 V	–10	—	—	µA
3-state output leakage current	I_{OZH}	$V_{OH} = V_{DD\_IO}$	—	—	10	µA
		$V_{OH} = V_{DD\_IO}$, 50 kΩ pull-down	10	66	200	µA
	I_{OZL}	V_{OL} = 0 V	–10	—	—	µA
		V_{OL} = 0 V, 50 kΩ pull-up	–200	–66	–10	µA
Supply current (during STOP) (*4)	I_{DDS1_CORE}	V_{DD_CORE} = 2.75 V, Ta = 85°C	—	—	1000	µA
		V_{DD_CORE} = 2.5 V, Ta = 25°C	—	25	—	µA
	I_{DDS1_IO}	V_{DD_IO} = 3.6 V (*3), Ta = 85°C	—	—	200	µA
		V_{DD_IO} = 3.3 V (*3), Ta = 25°C	—	4	—	µA
	I_{DDS1_PLL}	V_{DD_PLL} = 2.75 V, Ta = 85°C	—	—	50	µA
		V_{DD_PLL} = 2.5 V, Ta = 25°C	—	1	—	µA
Supply current (during operation) (*5)	I_{DDO_CORE}	f_{OSC} = 32.0 MHz , no load	—	85	115	mA
	I_{DDO_IO}		—	7	15	mA
	I_{DDO_PLL}		—	6	10	mA

* 1: Pins other than 5 V tolerant pins
* 2: 5 V tolerant pins
* 3: Input ports: V_{DD_IO} or 0V
  Other ports: No load excluding the current flowing in pull-up/pull-down resistors
* 4: LSI supply current when going into LSI stop mode by stopping clock oscillation, PLL operation, and random number generator operation and setting USB power-down mode.
* 5: The current supplied to the LSI when fingerprint authentication is executed without USB operation under the conditions that the programs are stored in the built-in Flash ROM and no external memory are connected.

– DC characteristics (USB)

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ. (*1)	Max.	Unit
Differential input sensitivity	V_{DI}	Absolute value of the difference between the DP and DM pins	0.2	—	—	V
Differential common mode range	V_{CM}	Includes VDI range	0.8	—	2.5	V
Single end input threshold voltage	V_{SE}		0.8	—	2.0	V
High level output voltage	V_{OH}	15K W RL is connected to GND	2.8	—	—	V
Low level output voltage	V_{OL}	1.5K W RL to 3.6 V	—	—	0.3	V
Hi-Z state input/output leakage current	I_{LO}	0 V < VIN < 3.3 V	–10		10	μA
Driver output resistance (*2)	Z_{DRV}	Steady state	28		44	Ω

*1: "Typ.": V_{DD_IO} = 3.3 V, V_{DD_CORE} = 2.5 V, Tj = 25°C

*2: Z_{DRV} includes the resistance of external serial resistors (24Ω±1%).

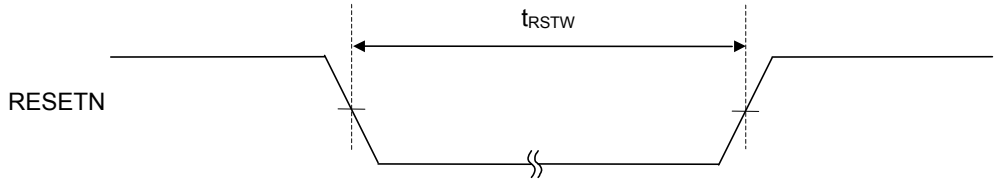
AC Characteristics

– Reset Timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset pulse width	t_{RSTW}	—	6.0	—	—	ms

○ Reset timing



*When power on, release the reset after the clock oscillation stabilization

– External ROM/RAM Timing

○ Access from CPU

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XROMCSN, XRAMCSN output delay time 1	t_{XCSD1}	C_L = 15 pF	—	—	4	ns
XROMCSN, XRAMCSN output delay time 2	t_{XCSD2}		—	—	$0.5*t_{BUSCLK}$ +8	
XROMCSN, XRAMCSN output hold time 1	t_{XCSH1}		–6	—	—	
XROMCSN, XRAMCSN output hold time 2	t_{XCSH2}		$0.5*t_{BUSCLK}$ –6	—	—	
XA output delay time 1	t_{XAD1}		—	—	4	
XA output delay time 2	t_{XAD2}		—	—	$0.5*t_{BUSCLK}$ +8	
XA output hold time 1	t_{XAH1}		–6	—	—	
XA output hold time 2	t_{XAH2}		0	—	—	
XA pulse width 1	t_{XAW1}		t_{RWIDTH} –12	—	t_{RWIDTH} +12	
XBSn output delay time 1	t_{XBSD1}		—	—	4	
XBSn output delay time 2	t_{XBSD2}		—	—	$0.5*t_{BUSCLK}$ +8	
XBSn output hold time 1	t_{XBSH1}		–6	—	—	
XBSn output hold time 2	t_{XBSH2}		$0.5*t_{BUSCLK}$ –6	—	—	
XBSn pulse width 1	t_{XBSW1}		t_{RWIDTH} –12	—	t_{RWIDTH} +12	
XWEN pulse width 1	t_{XWEW1}		t_{WWIDTH} –13	—	t_{WWIDTH} +13	
XD input setup time 1	t_{XDIS1}		22.5	—	—	
XD input setup time 2	t_{XDIS2}		22.5	—	—	
XD input hold time 1	t_{XDIH1}		0	—	—	
XD input hold time 2	t_{XDIH2}		0	—	—	
XD output delay time 1	t_{XDOD1}		$0.5*t_{BUSCLK}$ - 13	—	—	
XD output hold time 1	t_{XDOH1}		0	—	—	

t_{RWIDTH}: RE pulse width (set by register)
t_{WWIDTH}: WE pulse width (set by register)

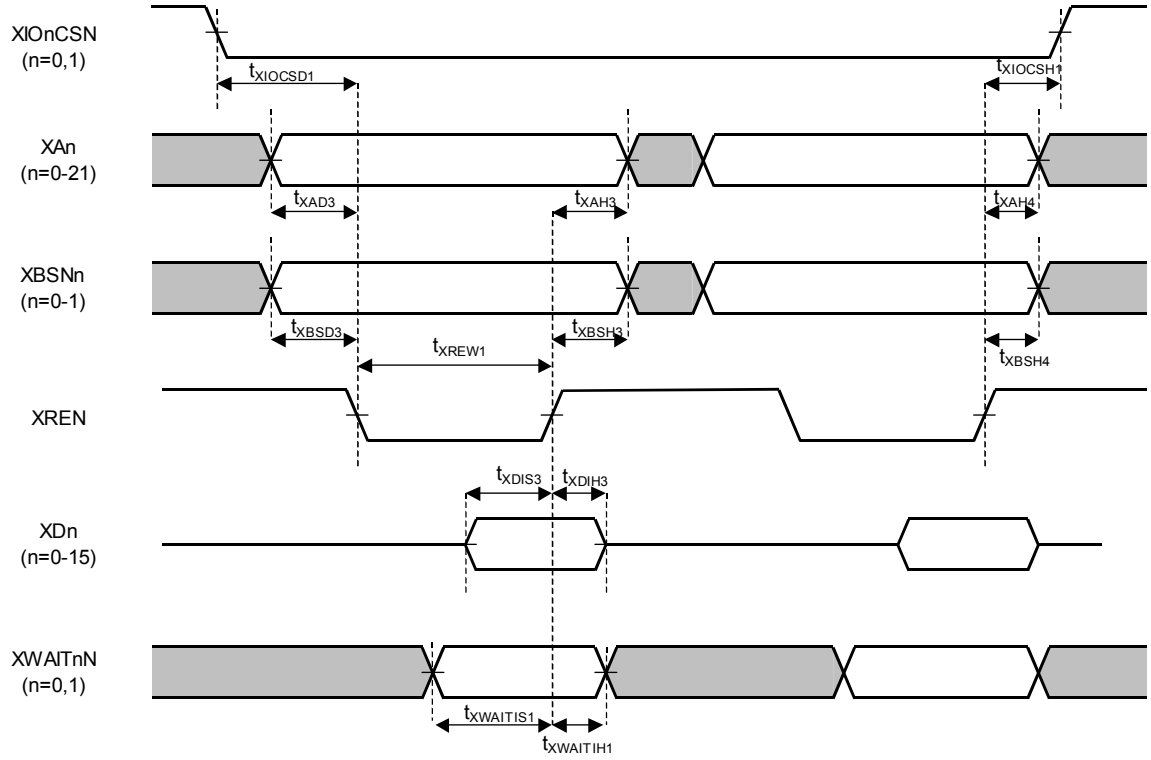
– External IO0, 1 Timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

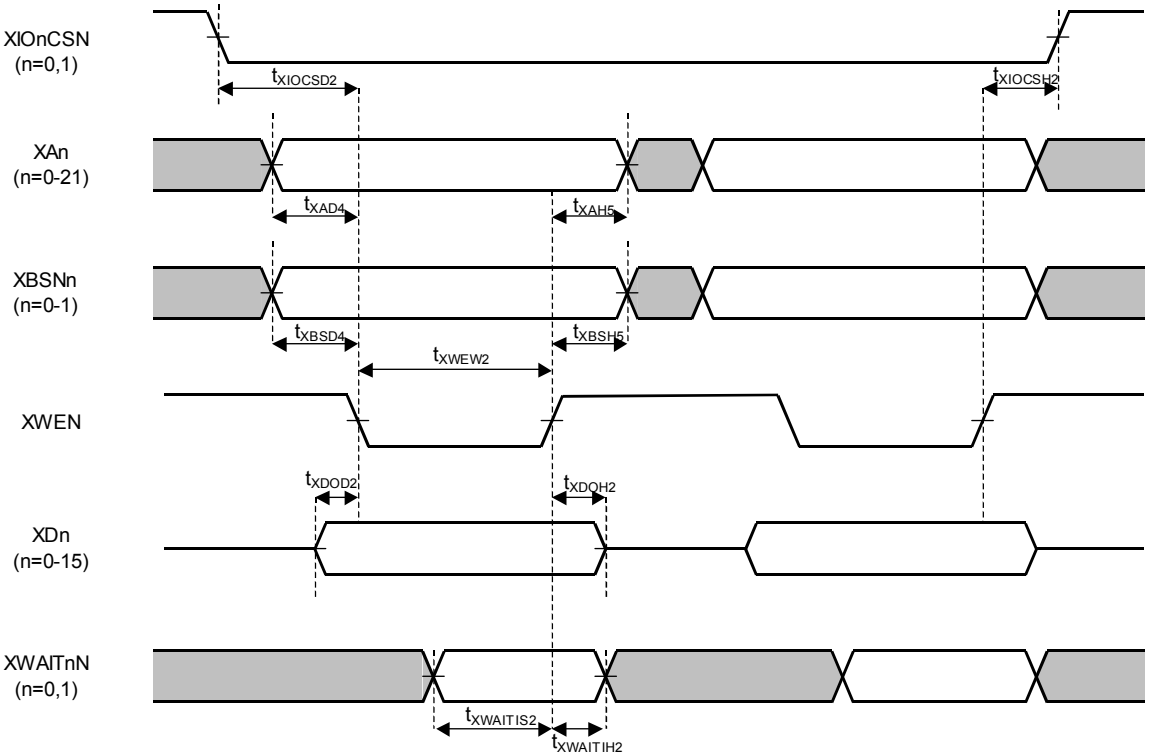
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XIOnCSN (n = 0,1) output delay time 1	$t_{XIOCSD1}$	C_L = 15 pF	—	—	t_{IOAS} +8	ns
XIOnCSN (n = 0,1) output delay time 2	$t_{XIOCSD2}$		—	—	1*t_{BUSCLK} + t_{IOAS} +8	
XIOnCSN (n=0,1) output hold time 1	$t_{XIOCSH1}$		1*t_{BUSCLK} –6	—	—	
XIOnCSN (n = 0,1) output hold time 2	$t_{XIOCSH2}$		1*t_{BUSCLK} –6	—	—	
XA output delay time 3	t_{XAD3}		—	—	t_{IOAS} + 8	
XA output delay time 4	t_{XAD4}		—	—	1*t_{BUSCLK} + t_{IOAS} +8	
XA output hold time 3	t_{XAH3}		–6	—	—	
XA output hold time 4	t_{XAH4}		1*t_{BUSCLK} –6	—	—	
XA output hold time 5	t_{XAH5}		1*t_{BUSCLK} –6	—	—	
XBSn output delay time 3	t_{XBSD3}		—	—	t_{IOAS} + 8	
XBSn output delay time 4	t_{XBSD4}		—	—	1*t_{BUSCLK} + t_{IOAS} +8	
XBSn output hold time 3	t_{XBSH3}		–6	—	—	
XBSn output hold time 4	t_{XBSH4}		1*t_{BUSCLK} –6	—	—	
XBSn output hold time 5	t_{XBSH5}		1*t_{BUSCLK} –6	—	—	
XREN pulse width 1	t_{XREW1}		$t_{IORWIDTH}$ –10	—	$t_{IORWIDTH}$ +10	
XWEN pulse width 2	t_{XWEW2}		$t_{IOWWIDTH}$ –10	—	$t_{IOWWIDTH}$ +10	
XD input setup time 3	t_{XDIS3}		20	—	—	
XD input hold time 3	t_{XDIH3}		0	—	—	
XD output delay time 2	t_{XDOD2}		t_{IOAS} - 13	—	—	
XD output hold time 2	t_{XDOH2}		1*t_{BUSCLK} –15	—	—	
XWAITn (n = 0,1) input setup time 1	$t_{XWAITIS1}$		1*t_{BUSCLK} + 20	—	—	
XWAITn (n = 0,1) input setup time 2	$t_{XWAITIS2}$		1*t_{BUSCLK} + 20	—	—	
XWAITn (n = 0,1) input hold time 1	$t_{XWAITIH1}$		5 –1*t_{BUSCLK}	—	—	
XWAITn (n = 0,1) input hold time 2	$t_{XWAITIH2}$		5 –1*t_{BUSCLK}	—	—	

t_{IOAS}: Address setup cycle (set by register)
$t_{IORWIDTH}$: RE pulse width (set by register)
$t_{IOWWIDTH}$: WE pulse width (set by register)

○ External IO0, 1 read timing



○ External IO0, 1 write timing



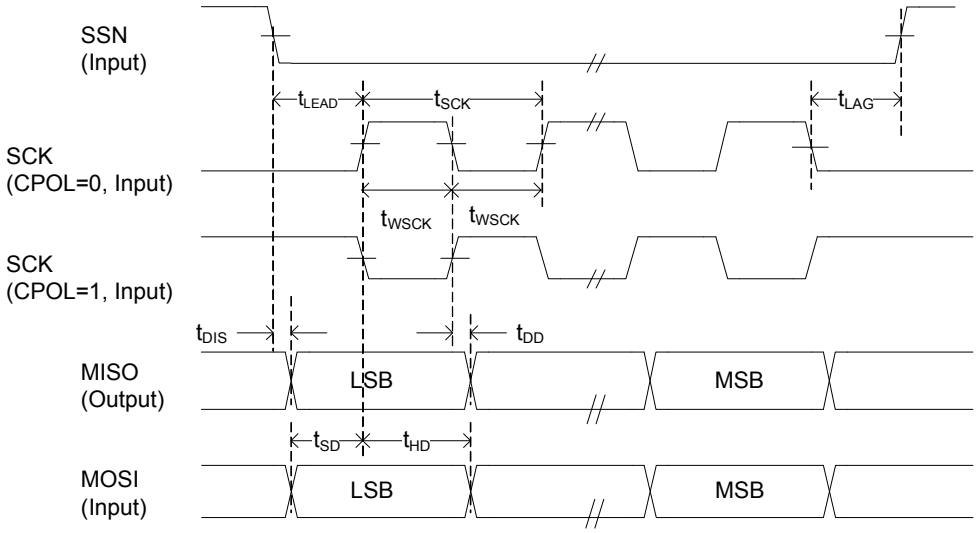
– USB Access Timing (Full-Speed)

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = −40 to +85°C)

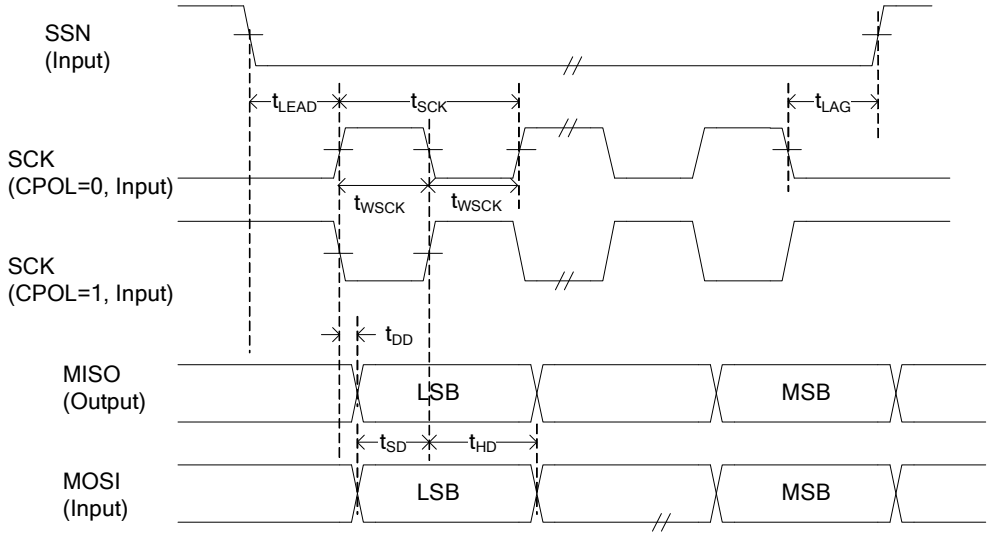
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied pin
Rise time (*1)	T_R	C_L = 50 pF	4	—	20	ns	DP,DM
Fall time (*1)	T_F	C_L = 50 pF	4	—	20	ns	
Output signal crossover voltage	V_{CRS}	C_L = 50 pF	0.8	—	2.5	V	
Data rate	T_{DRATE}	Average bit rate (12Mbps ±0.25%)	11.97	—	12.03	Mbps	

* 1: T_R and T_F: Rise time and fall time between 10% and 90% of the pulse amplitude, respectively

○ SPI slave mode timing (CPHA = 0)



○ SPI slave mode timing (CPHA = 1)



Note:
For CPHA and CPOL, see Chapter 15, “SPI”, in the ML67Q5250 User’s Manual.

– Synchronous SIO Access Timing

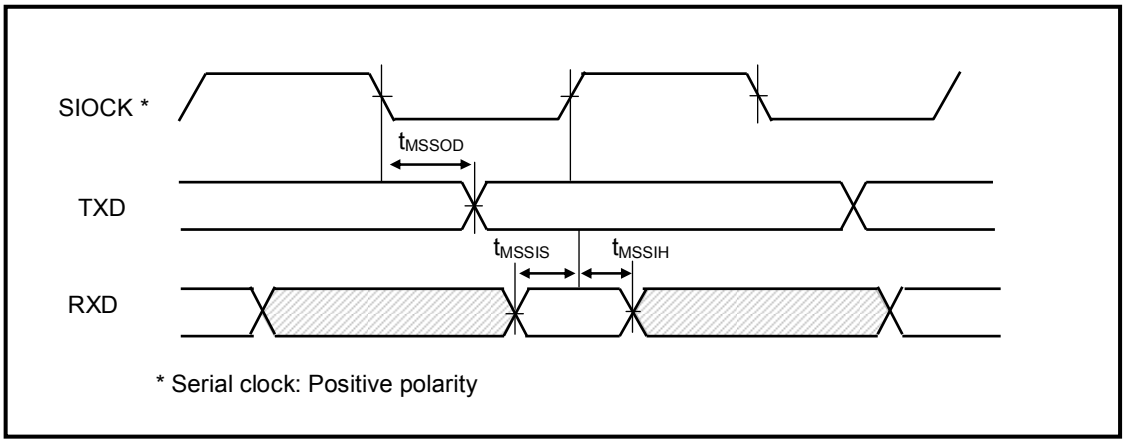
Switching between master mode and slave mode can be set for this synchronous SIO by the software register setting. Serial clock polarity can be switched.
When clock polarity is set to positive, data is transmitted (shifted out) on the falling edge of the clock and is received (shifted in) on the rising edge of the clock. At completion of 8-bit data transmission/reception, the clock stops at a high level and the last data is retained for data output.
When clock polarity is set to negative, data is transmitted (shifted out) on the rising edge of the clock and is received (shifted in) on the falling edge of the clock. At completion of 8-bit data transmission/reception, the clock stops at a low level and the last data is retained for data output.
The following waveforms show the cases where the clock polarity is positive.

• Maste mode

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	Remarks
Output data delay time	t_{MSSOD}	C_L = 30 pF	—	20	ns	
Input data setting time	t_{MSSIS}		30	—		
Input data retained time	t_{MSSIH}		10	—		

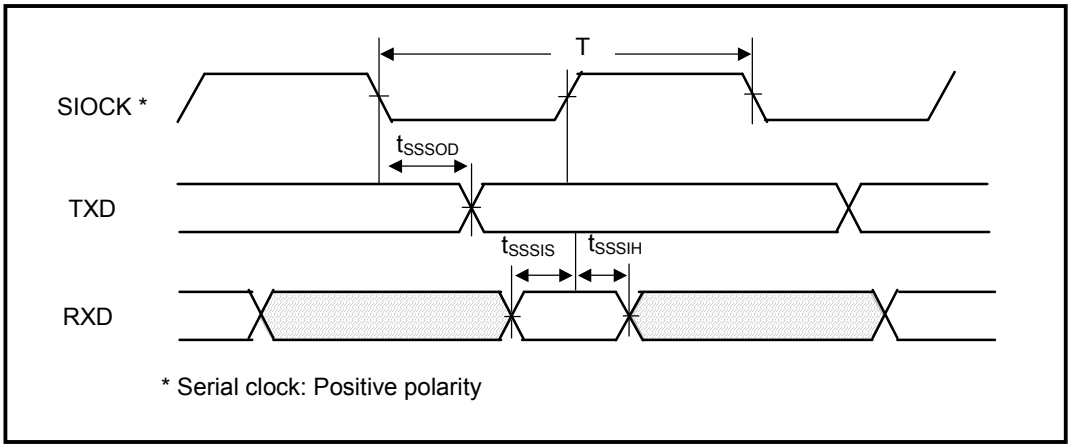
Note:
11 clock outputs for transferring is selectable from 2 synchronous SIO clock sources and the frequency divide ratios. For more details, see Chapter 16, Synchronous SIO, in the user's manual.



• Slave mode

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	Remarks
Serial clock cycle	T	C_L = 30 pF	62.5	—	ns	
Output data delay time	t_{SSSOD}		—	40		
Input data setting time	t_{SSSIS}		20	—		
Input data retained time	t_{SSSIH}		20	—		



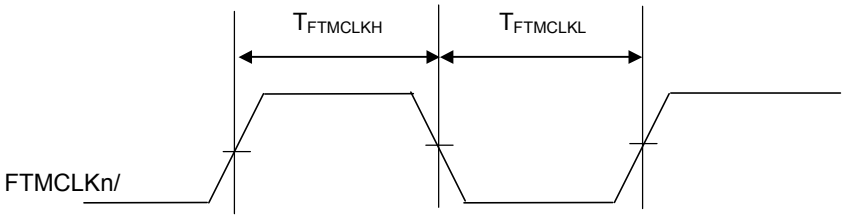
– FTM Access Timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FTMCLKn input H duration	$T_{FTMCLKH}$	—	t_{BUSCLK} ×2	—	—	ns
FTMCLKn input L duration	$T_{FTMCLKL}$	—	t_{BUSCLK} ×2	—	—	ns

Note 1: n = 0 to 2

○ FTMCLKn input timing (n = 0 to 2)



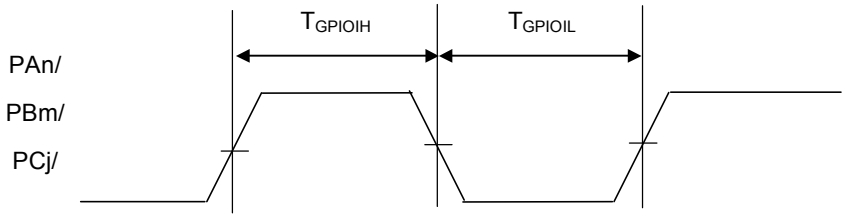
– GPIO (PA, PB, PC) Access Timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PAn, PBm, PCj input H duration	T_{GPIOIH}	—	t_{BUSCLK} ×2	—	—	ns
PAn, PBm, PCj input L duration	T_{GPIOIL}	—	t_{BUSCLK} ×2	—	—	ns

Note 1: n = 12 to 0, m=13 to 0, j = 15 to 0

○ PAn,PBm,PCj input timing (n = 12 to 0, m = 13 to 0, j = 15 to 0)



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL67Q5250-1	Nov. 9, 2007	–	–	Preliminary edition 1
FEDL67Q5250-1	Feb.22, 2008	–	–	Final edition 1
		11	11	Corrected "Core power supply" to "IO power supply" at Description of VDDIO in the Table of Other Pins. Corrected "Core GND" to "IO GND" at Description of GNDIO in the Table of Other Pins.
		12 to 30	12 to 30	Deleted all the sentences of "Note: The values in the table above are preliminary and are subject to change without notice." indicated in Chapter 22 of the preliminary version.
		12	12	Added "(*1)" to "Digital power supply voltage (CORE)" and "PLL power supply voltage (PLL)" in the specification table of Guaranteed Operating Ranges. Added " * 1: Please supply from same power source to both VDD_CORE pins and VDD_PLL pin." to the margin of this specification table. Changed "Taflw" into "Ta_flwrite" with the sign of the item of the ambient temperature of this table.
		14	14	Changed the specification value of "Supply current (during operation)" in the specification table of DC characteristics (Core/IO) Added "*5: The current supplied to the LSI…" at the lower column of the specification table of DC characteristics (Core/IO).
		15	15	Changed "|(YB)-(YBN)|" into “Absolute value of the difference between the DP and DM pins” at the condition column of "Differential input sensitivity" in the specification table of DC characteristics (USB). Deleted the maximum specification of "High level output voltage" and the minimum specification of "Low level output voltage" in the specification table of DC characteristics (USB).
		18, 19	18, 19	Changed the several specification values in the two tables of "Access from CPU" and "Access by DMA" of External ROM/RAM Timing.
		21	21	Changed the several specification value in the specification table of External IO0, 1 Timing.
		23	23	Changed the specification value of "Output signal crossover voltage" in the specification table of USB Access Timing (Full-Speed).