Zilog - Z8L18020FSC00TR Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8L180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l18020fsc00tr

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

$\overline{RD}$. Read (Output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$. Refresh (Output, active Low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the $\overline{REF}$ signal of the Z64180.*

$\overline{RTS0}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:
X = Do not care.
MC = Machine Cycle.

$\overline{TEND0}$, $\overline{TEND1}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT}. Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

$\overline{WAIT}$. Wait (Input, active Low). $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the $\overline{WAIT}$ input is sampled High, at which time execution continues.

$\overline{WR}$. WRITE (Output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics).

Several pins are used for different conditions, depending on the circumstance.

ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSI/O) channel.

Clock Generator. This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and provides the timing for both internal and external devices.

Bus State Controller. This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. Also includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

Memory Management Unit. The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1-MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object code maintains compatibility with the Z80 CPU, while offering access to an extended memory space. Accomplished by using an effective common-area/banked-area scheme.

Central Processing Unit. The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core is modified to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides high-speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1-MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI).

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

Programmable Reload Timers (PRT). This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

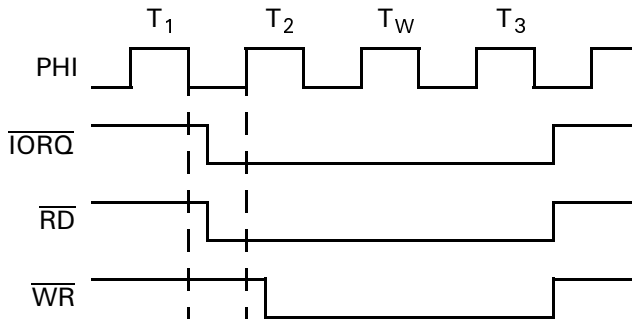


Figure 11. I/O Read and Write Cycles with $\overline{IOC}$ = 1

When $\overline{IOC}$ = 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing of the Z80. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. (Figure 12.)

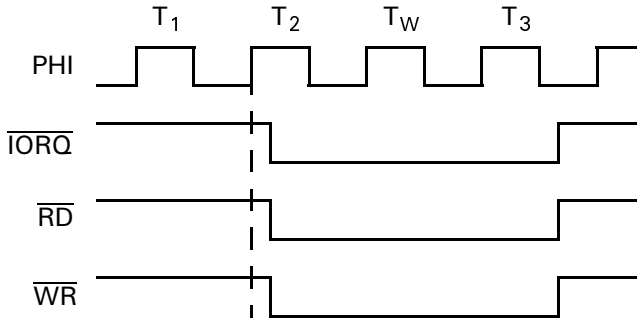


Figure 12. I/O Read and Write Cycles with $\overline{IOC}$ = 0

HALT and Low-Power Operating Modes. The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{HALT}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{HALT}$, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

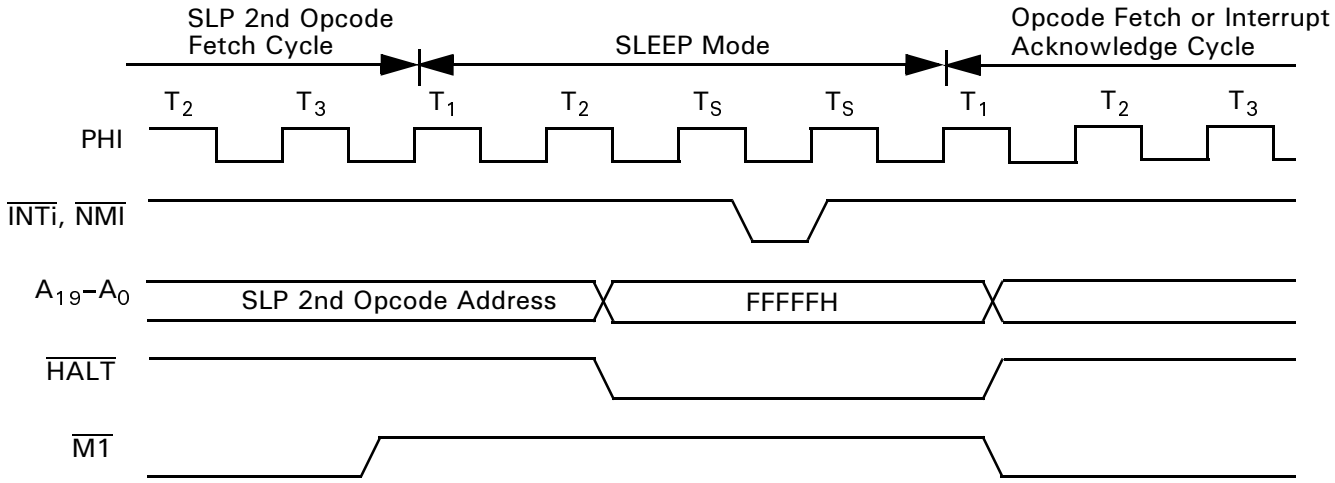


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{\text{RESET}}$, an external interrupt request on $\overline{\text{NMI}}$, or an external interrupt request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{\text{NMI}}$, or due to an enabled external interrupt request when the $\overline{\text{IEF}}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.

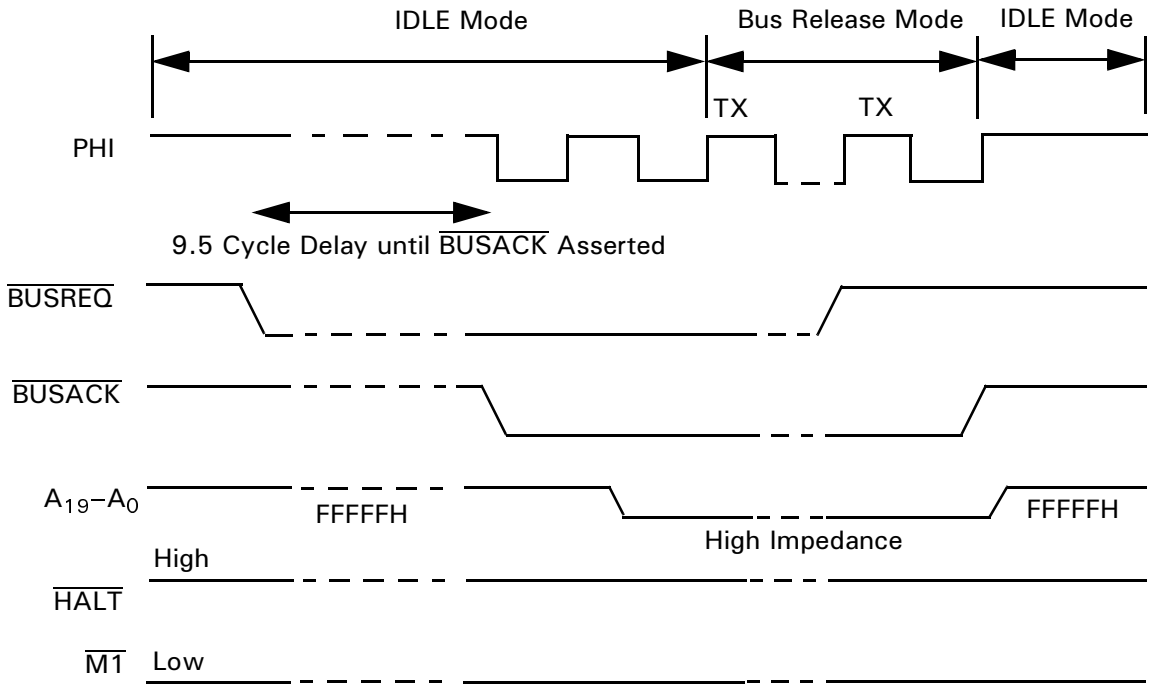


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0–2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to V_{SS} (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to V_{OL} MAX or V_{OL} MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

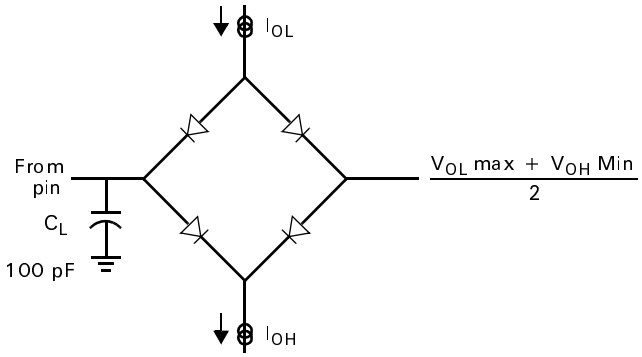


Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 ~ +7.0	V
Input Voltage	V_{IN}	–0.3 ~ V_{cc} +0.3	V
Operating Temperature	T_{OPR}	0 ~ 70	°C
Extended Temperature	T_{EXT}	–40 ~ 85	°C
Storage Temperature	T_{STG}	–55 ~ +150	°C

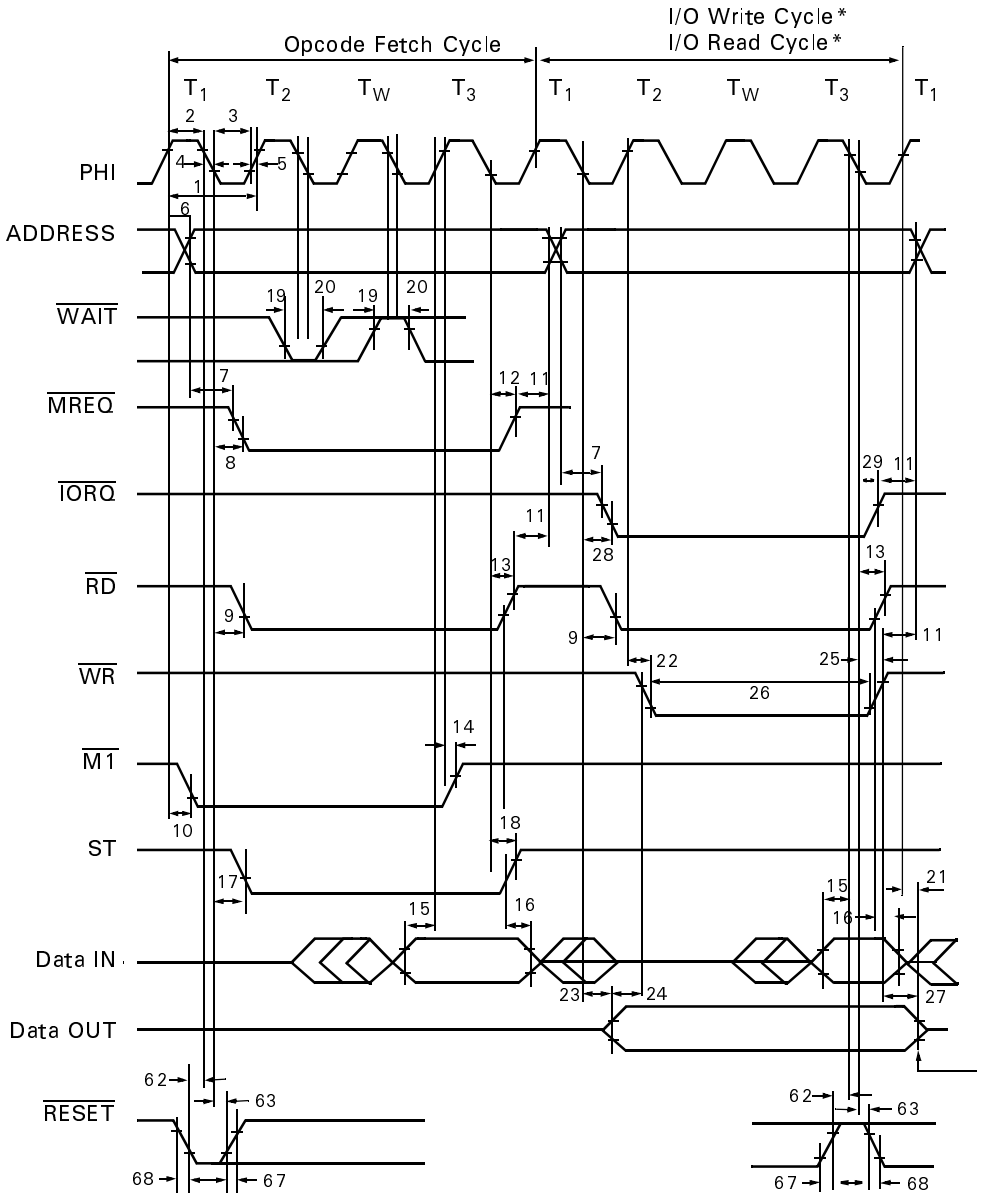
Note: Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

AC CHARACTERISTICS—Z8S180

Table 8. Z8S180 AC Characteristics
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
1	t_{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t_{CHW}	Clock "H" Pulse Width	15	—	10	—	ns
3	t_{CLW}	Clock "L" Pulse Width	15	—	10	—	ns
4	t_{CF}	Clock Fall Time	—	10	—	5	ns
5	t_{CR}	Clock Rise Time	—	10	—	5	ns
6	t_{AD}	PHI Rise to Address Valid Delay	—	30	—	15	ns
7	t_{AS}	Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall)	5	—	5	—	ns
8	t_{MED1}	PHI Fall to $\overline{MREQ}$ Fall Delay	—	25	—	15	ns
9	t_{RDD1}	PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0	—	25	—	15	
10	t_{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	—	15	ns
11	t_{AH}	Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High	5	—	5	—	ns
12	t_{MED2}	PHI Fall to $\overline{MREQ}$ Rise Delay	—	25	—	15	ns
13	t_{RDD2}	PHI Fall to $\overline{RD}$ Rise Delay	—	25	—	15	ns
14	t_{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	—	40	—	15	ns
15	t_{DRS}	Data Read Set-up Time	10	—	5	—	ns
16	t_{DRH}	Data Read Hold Time	0	—	0	—	ns
17	t_{STD1}	PHI Fall to ST Fall Delay	—	30	—	15	ns
18	t_{STD2}	PHI Fall to ST Rise Delay	—	30	—	15	ns
19	t_{WS}	$\overline{WAIT}$ Set-up Time to PHI Fall	15	—	10	—	ns
20	t_{WH}	$\overline{WAIT}$ Hold Time from PHI Fall	10	—	5	—	ns
21	t_{WDZ}	PHI Rise to Data Float Delay	—	35	—	20	ns
22	t_{WRD1}	PHI Rise to $\overline{WR}$ Fall Delay	—	25	—	15	ns
23	t_{WDD}	PHI Fall to Write Data Delay Time	—	25	—	15	ns
24	t_{WDS}	Write Data Set-up Time to $\overline{WR}$ Fall	10	—	10	—	ns
25	t_{WRD2}	PHI Fall to $\overline{WR}$ Rise Delay	—	25	—	15	ns
26	t_{WRP}	$\overline{WR}$ Pulse Width (Memory Write Cycle)	80	—	45	—	ns
26a		$\overline{WR}$ Pulse Width (I/O Write Cycle)	150	—	70	—	ns
27	t_{WDH}	Write Data Hold Time from $\overline{WR}$ Rise	10	—	5	—	ns
28	t_{IOD1}	PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0	—	25	—	15	
29	t_{IOD2}	PHI Fall to $\overline{IORQ}$ Rise Delay	—	25	—	15	ns
30	t_{IOD3}	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	125	—	80	—	ns
31	t_{INTS}	$\overline{INT}$ Set-up Time to PHI Fall	20	—	15	—	ns

TIMING DIAGRAMS



Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states (T_W), and $\overline{MREQ}$ is active instead of $\overline{IORQ}$.

Figure 20. CPU Timing
(Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)

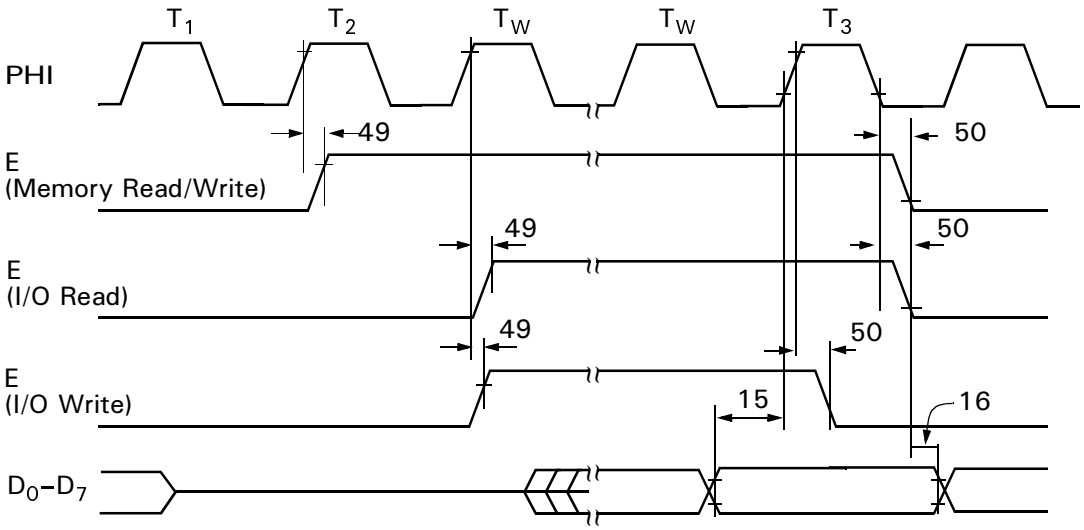


Figure 24. E Clock Timing
(Memory Read/Write Cycle, I/O Read/Write Cycle)

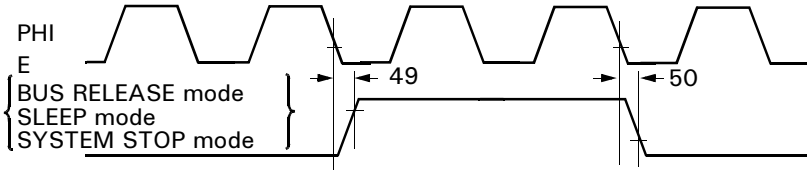


Figure 25. E Clock Timing
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

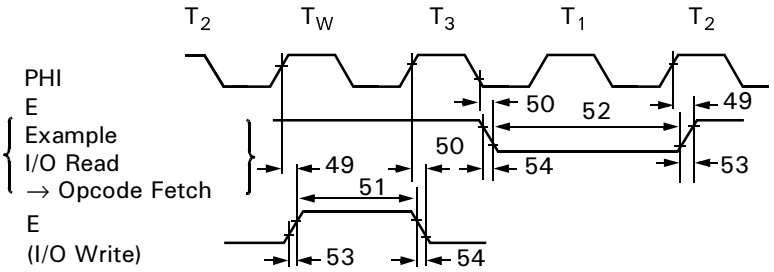


Figure 26. E Clock Timing
(Minimum Timing Example of P_{WEL} and P_{WEH})

CPU CONTROL REGISTER

CPU Control Register (CCR). This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low-noise options (Figure 31).

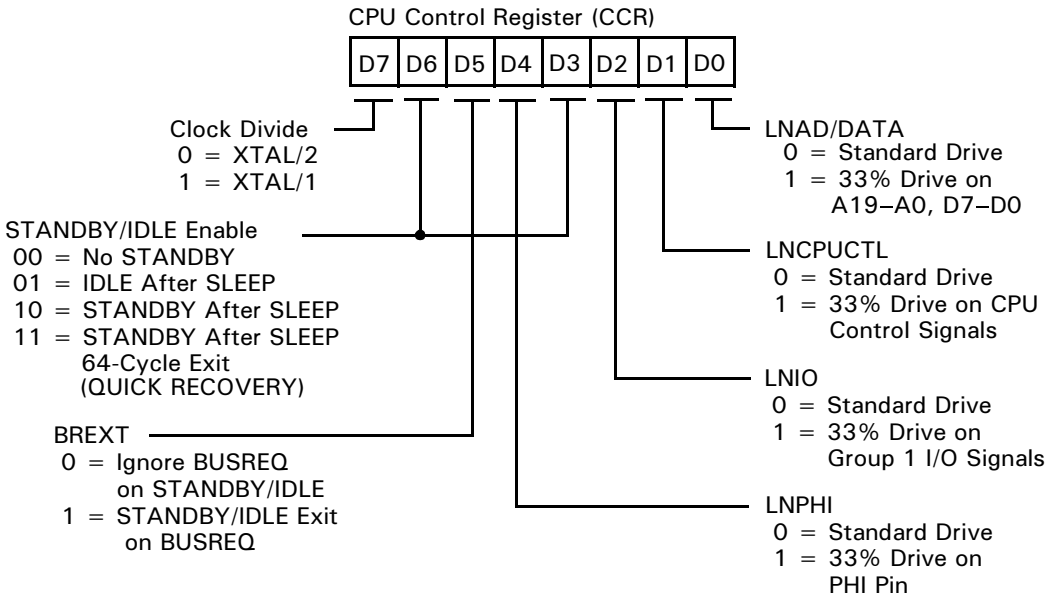


Figure 31. CPU Control Register (CCR) Address 1FH

Bit 7. Clock Divide Select. If this bit is 0, as it is after a RESET, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

Bits 6 and 3. STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 2^{17} (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER modes, describes the subject more fully.

Bit 5 BREXT. This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4 LNPHI. This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{RTS0}$	TxS
CKA1/$\overline{TEND0}$	CKA0/$\overline{DREQ0}$
TXA0	TXA1
$\overline{TENDi}$	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{BUSACK}$	$\overline{RD}$
$\overline{WR}$	$\overline{M1}$
$\overline{MREQ}$	$\overline{IORQ}$
$\overline{RFSH}$	$\overline{HALT}$
E	TEST
ST	

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

ASCI REGISTER DESCRIPTION

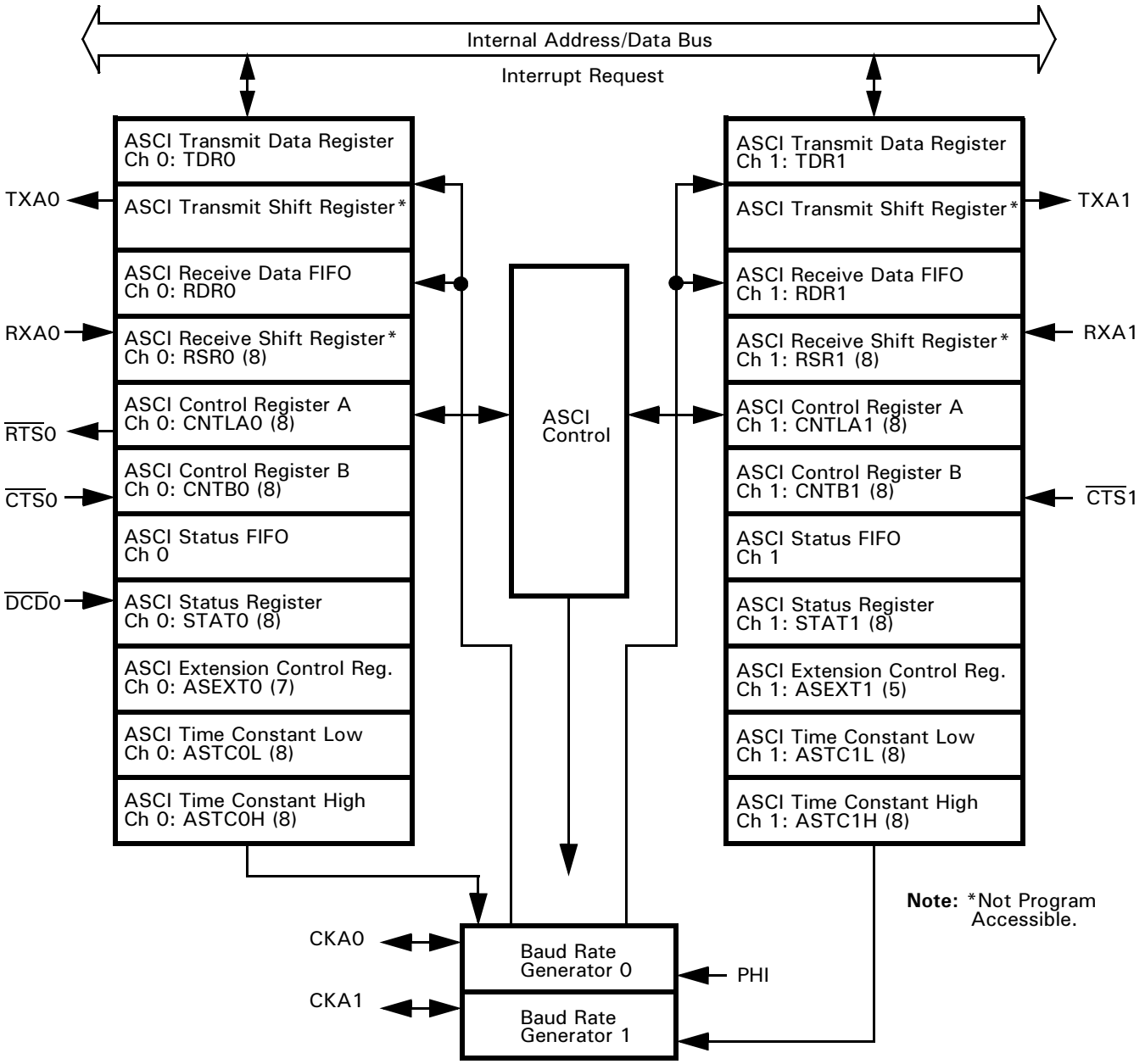


Figure 32. ASCI Block Diagram

ASCI Transmit Shift Register 0,1. When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR idles by outputting a continuous High level. This register is not program-accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

ASCI TIME CONSTANT REGISTERS

If the SS2–0 bits of the CNTLB register are not 111, and the BRG mode bit in the ASEXT register is 1, the ASCI divides the PHI clock by two times the registers' 16-bit value, plus two. As a result, the clock is presented to the transmitter and receiver for division by 1, 16, or 64, and is output on the CKA pin.

If the SS2–0 bits in an ASCI CNTLB register are not 111, and the BRG mode bit in its Extension Control Register is 1, its *new* baud rate generator divides PHI for serial clocking, as follows:

$$\text{bits/second} = f_{PHI}/(2*(TC+2) \times \text{sampling rate})$$

where TC is the 16-bit value programmed into the ASCI Time Constant High and Low registers. If the ASCI multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the sampling rate, as follows:

$$f_{CKAout} = f_{PHI}/(2*(TC+2))$$

Find the TC value for a particular serial bit rate as follows:

$$TC = (f_{PHI}/(2 \times \text{bits/second} \times \text{sampling rate})) - 2$$

ASCI Time Constant Register 0 Low (ASTC0L, I/O Address 1AH)
ASCI Time Constant Register 1 Low (ASTC1L, I/O Address 1CH)

Bit	7	6	5	4	3	2	1	0
	LS 8 Bits of Time Constant							

ASCI Time Constant Register 0 High (ASTC0H, I/O Address 1BH)
ASCI Time Constant Register 1 High (ASTC1H, I/O Address 1DH)

Bit	7	6	5	4	3	2	1	0
	MS 8 Bits of Time Constant							

Figure 53. ASCI Time Constant Registers

CLOCK MULTIPLIER REGISTER

(Z180 MPU Address 1EH)

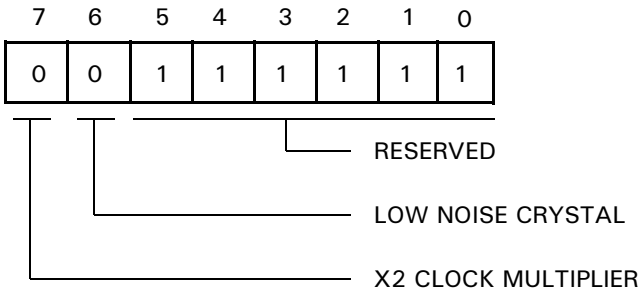


Figure 54. Clock Multiplier Register

Bit 7. X2 Clock Multiplier Mode. When this bit is set to 1, the programmer can double the internal clock speed from the speed of the external clock. This feature only operates effectively with frequencies of 10–16 MHz (20–32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

Bit 6. Low Noise Crystal Option. Setting this bit to 1 enables the low-noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If a low-noise option is required, and normal device operation is required, use the clock multiplier feature.

Table 13. Low Noise Option

Low Noise ADDR 1E, bit 6 = 1	Normal ADDR 1E, bit 6 = 0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

DMA MEMORY ADDRESS REGISTER CHANNEL 1

The DMA Memory Address Register Channel 1 specifies the physical memory address for channel 1 transfers. The address may be a destination or a source memory location. The register contains 20 bits and may specify up to 1024 KB memory addresses.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L
Address 28H

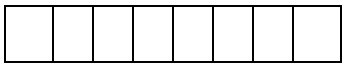


Figure 65. DMA Memory Address Register, Channel 1L

DMA Memory Address Register, Channel 1H

Mnemonic MAR1H
Address 29H

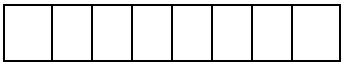


Figure 66. DMA Memory Address Register, Channel 1H

DMA Memory Address Register, Channel 1B

Mnemonic MAR1B
Address 2AH

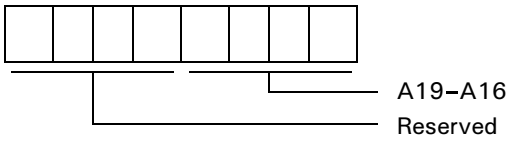


Figure 67. DMA Memory Address Register, Channel 1B

DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, Completed or In Progress.

DMA Status Register

Mnemonic DSTAT
Address 30H

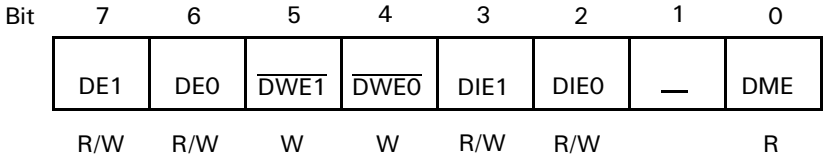


Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (Bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, $\overline{\text{DWE1}}$ should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (Bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0, $\overline{\text{DWE0}}$ should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DE0 is cleared to 0 during RESET.

$\overline{\text{DWE1}}$: DE1 Bit Write Enable (Bit 5). When performing any software WRITE to DE1, this bit should be written with 0 during the same access. $\overline{\text{DWE1}}$ always reads as 1.

$\overline{\text{DWE0}}$: DE0 Bit Write Enable (Bit 4). When performing any software WRITE to DE0, this bit should be written with 0 during the same access. $\overline{\text{DWE0}}$ always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (Bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DIE0: DMA Interrupt Enable Channel 0 (Bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DME: DMA Main Enable (Bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

Note: DME cannot be directly written. The bit is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

All TRAPs occur after fetching an undefined second opcode byte following one of the prefix opcodes (CBH, DDH, EDH, or FDH) or after fetching an undefined third opcode byte following one of the double-prefix opcodes (DDCBH or FDCBH).

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the opcode generated the TRAP. If UFO = 0, the starting address of the invalid instruction is the stacked PC–1. If UFO = 1, the starting address of the invalid instruction is equal to the stacked PC–2.

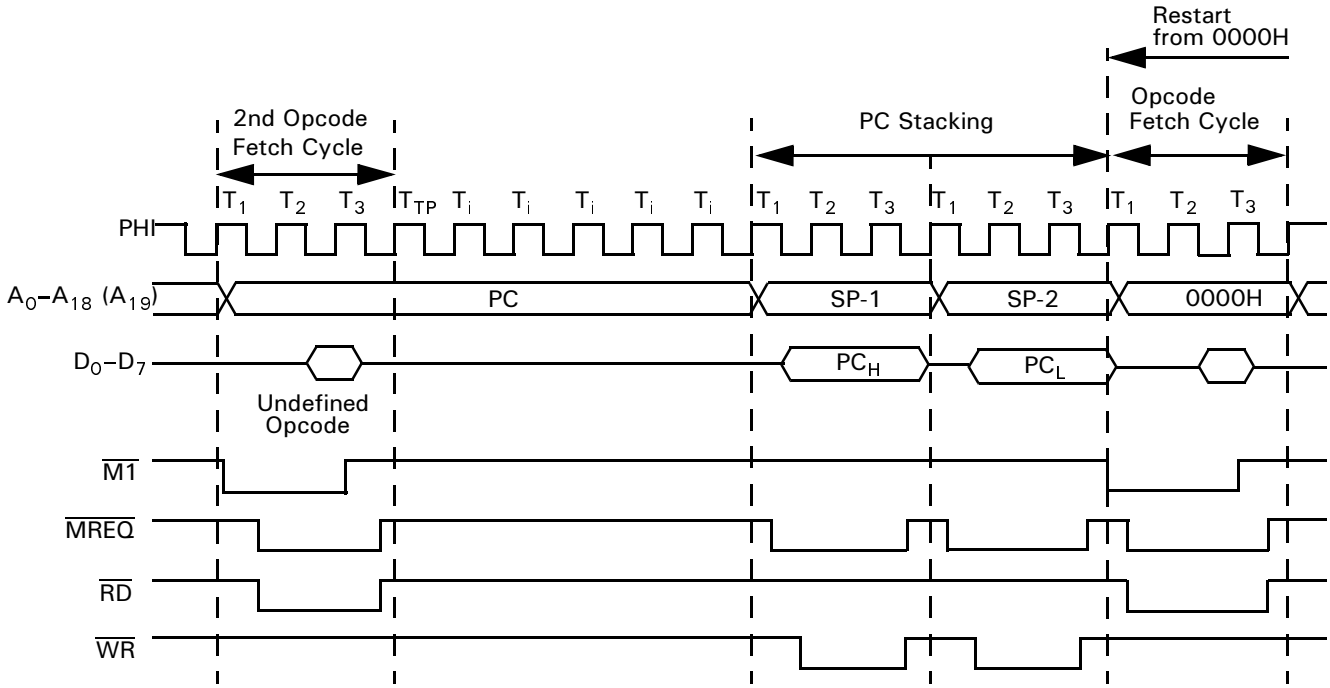


Figure 75. TRAP Timing—2nd Opcode Undefined

REFRESH CONTROL REGISTER

Mnemonic RCR
Address 36H

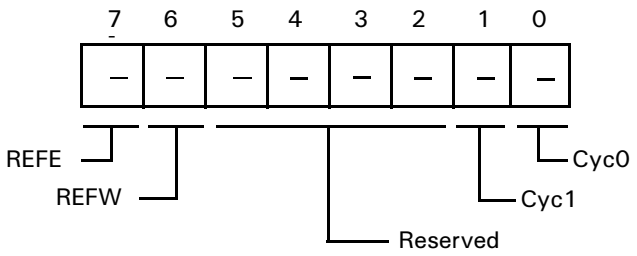


Figure 77. Refresh Control Register (RCR: I/O Address = 36H)

The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

REFE: Refresh Enable (Bit 7). REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (Bit 6). REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

CYC1, 0: Cycle Interval (Bit 1,0). CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

Table 18. DRAM Refresh Intervals

			Time Interval				
CYC1	**CYC0**	**Insertion Interval**	**PHI: 10 MHz**	**8 MHz**	**6 MHz**	**4 MHz**	**2.5 MHz**
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.6 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

Note: *calculated interval.

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

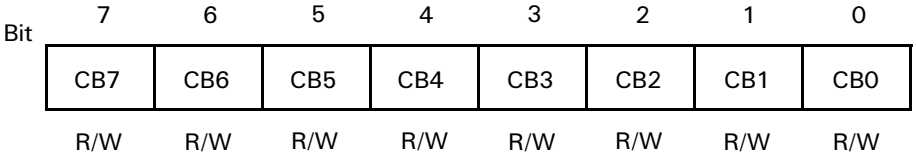


Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

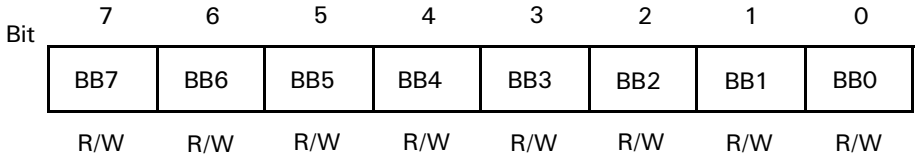


Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

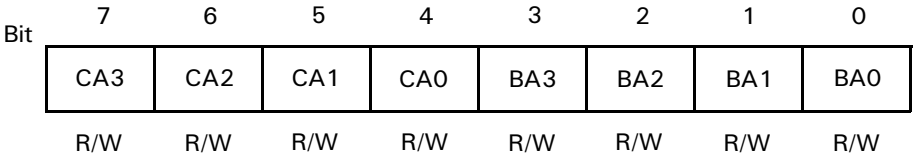


Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR
Address 3EH

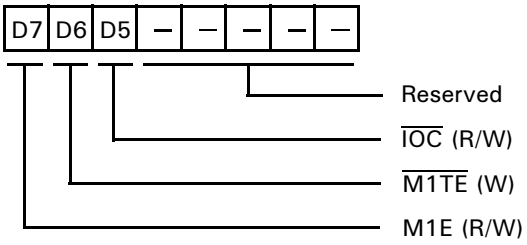


Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

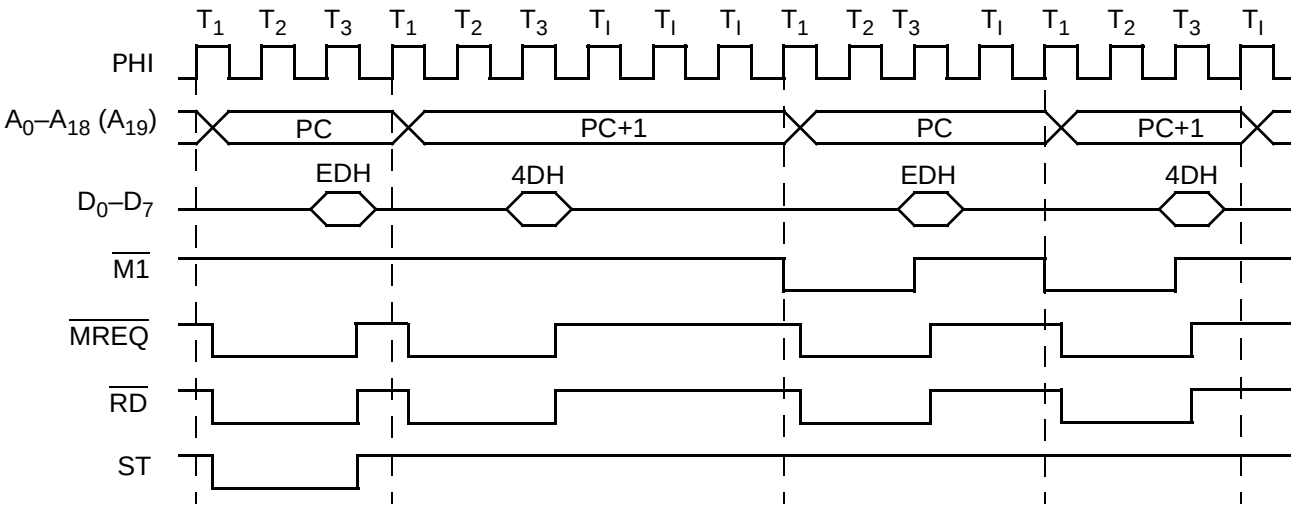


Figure 82. RETI Instruction Sequence with M1E = 0