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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010fec

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{\text{NMI}}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{\text{INT0}}$		IN	IN	IN
5	11	10	$\overline{\text{INT1}}$		IN	IN	IN
6	12	11	$\overline{\text{INT2}}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V _{SS}		V _{SS}	V _{SS}	V _{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T _{OUT}		N/A	OUT	OUT
32	34	32	V _{DD}		V _{DD}	V _{DD}	V _{DD}
33	35		A19		3T	3T	High
34	36	33	V _{SS}		V _{SS}	V _{SS}	V _{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{\text{RTS0}}$		High	OUT	High
46	46	43	$\overline{\text{CTS0}}$		IN	OUT	IN
47	47	44	$\overline{\text{DCD0}}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{\text{DREQ0}}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{\text{TEND0}}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{\text{CTS1}}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		High	OUT	High
61	60	56	$\overline{\text{HALT}}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		High	OUT	High
65	62	58	$\overline{\text{IORQ}}$		High	3T	High
66	63	59	$\overline{\text{MREQ}}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{\text{M1}}$		High	High	High
69	66	62	$\overline{\text{WR}}$		High	3T	High
70	67	63	$\overline{\text{RD}}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V _{SS}		GND	GND	GND
73	2		V _{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

\overline{RD} . Read (Output, active Low, 3-state). \overline{RD} indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

\overline{RFSH} . Refresh (Output, active Low). Together with \overline{MREQ} , \overline{RFSH} indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the \overline{REF} signal of the Z64180.*

$\overline{RTS0}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCII channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCII channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCII channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and \overline{HALT} output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	\overline{HALT}	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:

X = Do not care.

MC = Machine Cycle.

$\overline{TEND0}$, $\overline{TEND1}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT} . Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCII channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

\overline{WAIT} . Wait (Input, active Low). \overline{WAIT} indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the \overline{WAIT} input is sampled High, at which time execution continues.

\overline{WR} . WRITE (Output, active Low, 3-state). \overline{WR} indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see [DC Characteristics](#)).

Several pins are used for different conditions, depending on the circumstance.

Table 4. Multiplexed Pin Descriptions

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T _{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0/ $\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected.
CKA1/ $\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS/ $\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.

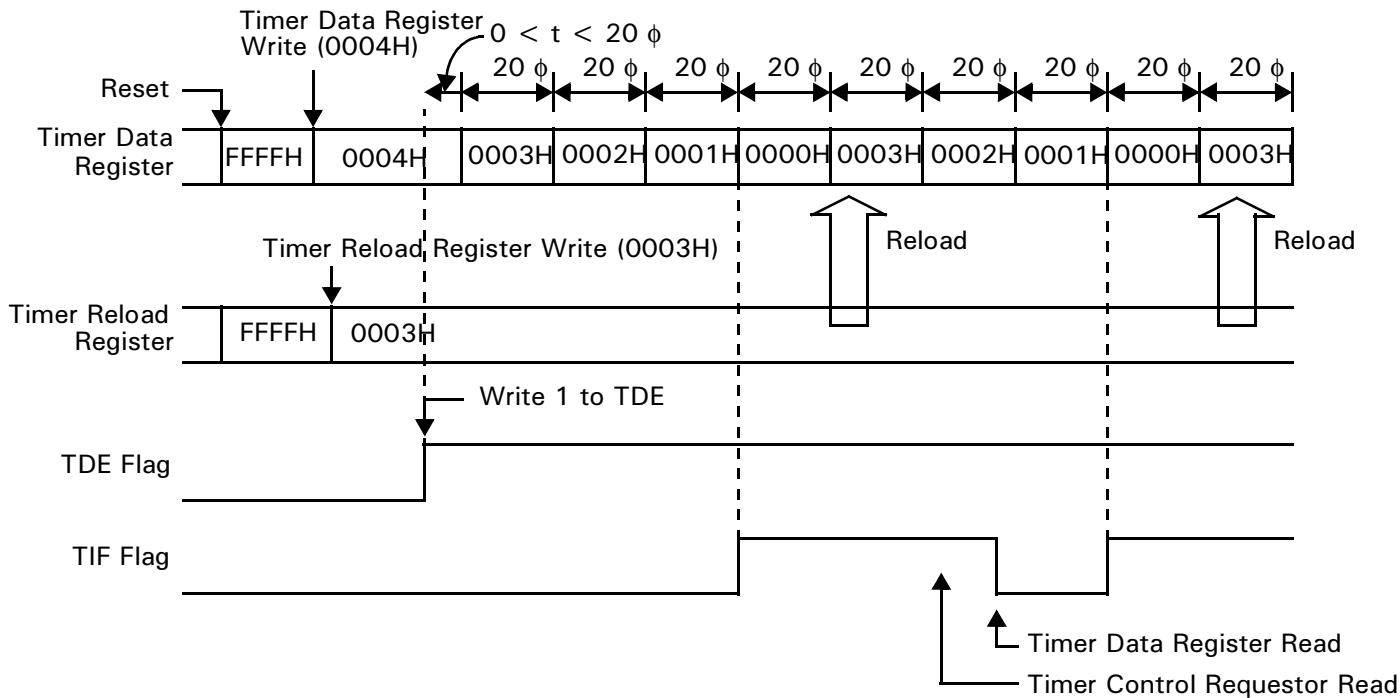


Figure 5. Timer Initialization, Count Down, and Reload Timing

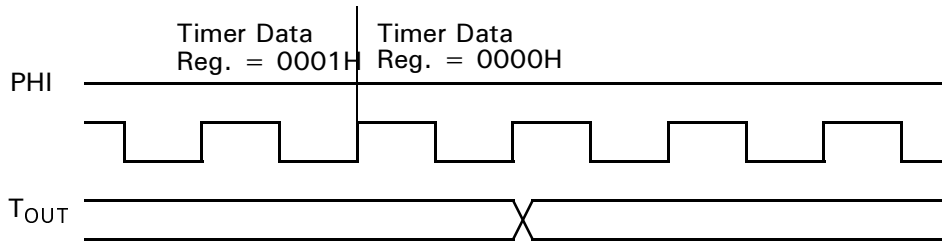


Figure 6. Timer Output Timing

Clocked Serial I/O (CSI/O). The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

Note: TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

ARCHITECTURE (Continued)

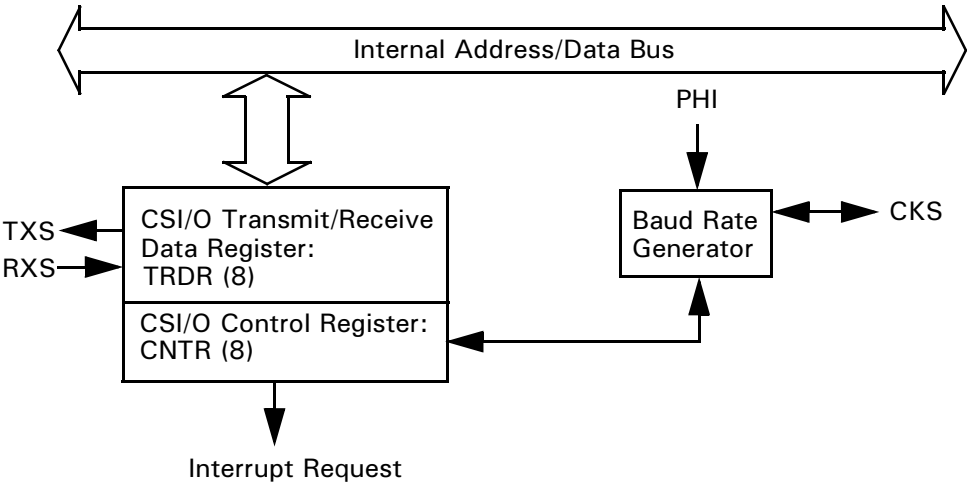


Figure 7. CSI/O Block Diagram

OPERATION MODES

Z80 versus 64180 Compatibility. The Z8S180/Z8L180 is descended from two different “ancestor” processors, ZiLOG’s original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

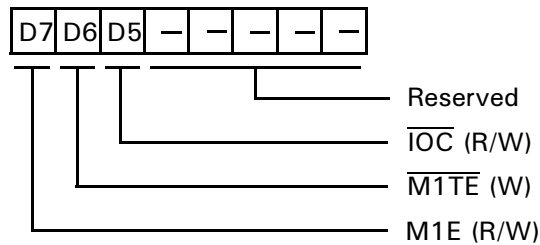


Figure 8. Operating Control Register
(OMCR: I/O Address = 3EH)

M1E ($\overline{\text{M1}}$ Enable). This bit controls the $\overline{\text{M1}}$ output and is set to a 1 during RESET.

When $\text{M1E} = 1$, the $\overline{\text{M1}}$ output is asserted Low during op-code fetch cycles, Interrupt Acknowledge cycles, and the first machine cycle of an NMI acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch a RETI instruction one time. When fetching a RETI from a zero-wait-state memory location, the processor uses three clock bus cycles. These bus cycles are not fully Z80-timing compatible.

When $\text{M1E} = 0$, the processor does not drive $\overline{\text{M1}}$ Low during the instruction fetch cycles. After fetching a RETI instruction with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{\text{M1}}$ Low. This option may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 5 show the RETI sequence when M1E is 0.

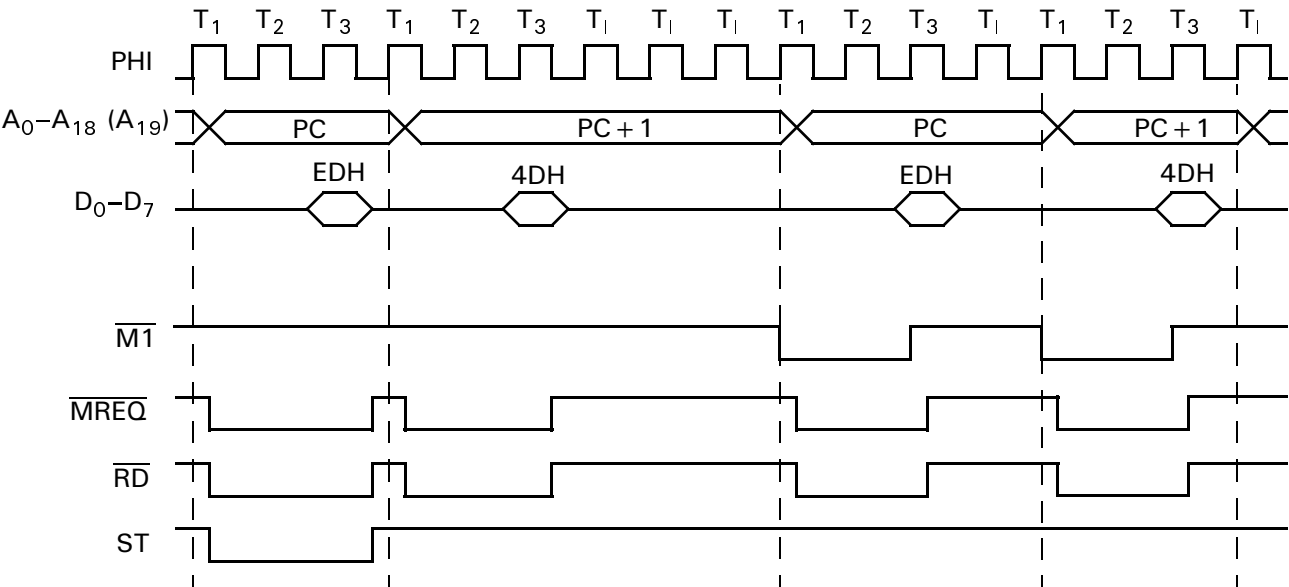


Figure 9. RETI Instruction Sequence with M1E = 0

OPERATION MODES (Continued)

Table 5. RETI Control Signal States

Machine Cycle	States	Address	Data	\overline{RD}	\overline{WR}	\overline{MREQ}	\overline{IORQ}	$\overline{M1}$ M1E =	$\overline{M1}$ M1E =	\overline{HALT}	ST
								1	0		
1	T1–T3	1st Opcode	EDH	0	1	0	1	0	1	1	0
2	T1–T3	2nd Opcode	4DH	0	1	0	1	0	1	1	0
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
3	T1–T3	1st Opcode	EDH	0	1	0	1	0	0	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
4	T1–T3	2nd Opcode	4DH	0	1	0	1	0	1	1	1
5	T1–T3	SP	Data	0	1	0	1	1	1	1	1
6	T1–T3	SP + 1	Data	0	1	0	1	1	1	1	1

$\overline{M1TE}$ ($\overline{M1}$ Temporary Enable). This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on $\overline{M1}$ after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE} = 1$, there is no change in the operation of the $\overline{M1}$ signal, and M1E controls its function. When $\overline{M1TE} = 0$, the $\overline{M1}$ output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This condition is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure 10).

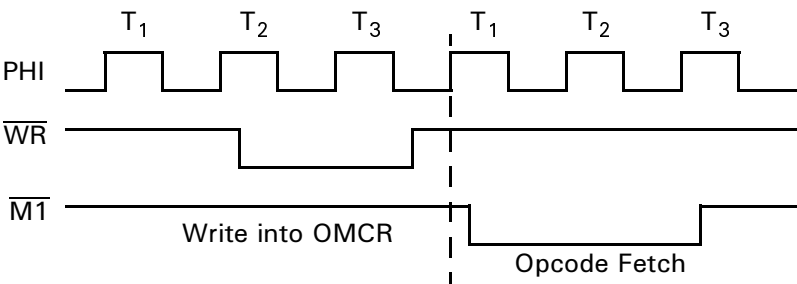
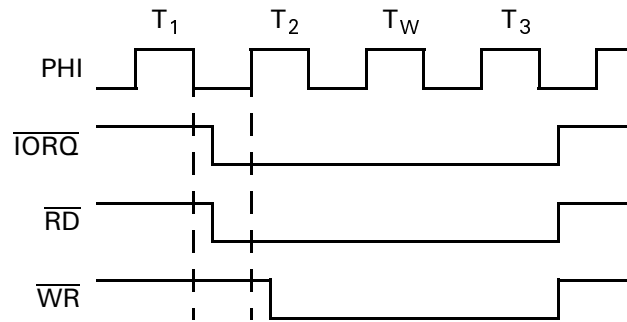


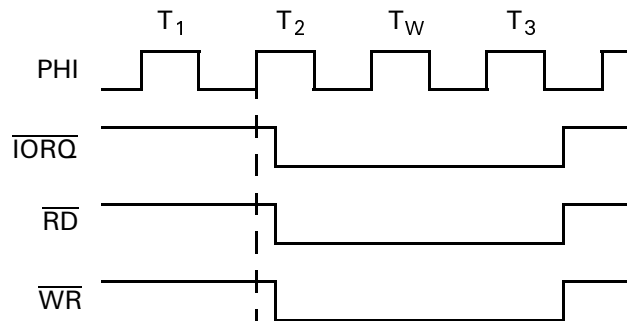
Figure 10. M1 Temporary Enable Timing

IOC (I/O Compatibility). This bit controls the timing of the \overline{IORQ} and \overline{RD} signals. The bit is set to 1 by RESET.

When $\overline{IOC} = 1$, the \overline{IORQ} and \overline{RD} signals function the same as the Z64180 (Figure 11).

Figure 11. I/O Read and Write Cycles with $\overline{\text{IOC}} = 1$

When $\overline{\text{IOC}} = 0$, the timing of the $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals match the timing of the Z80. The $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals go active as a result of the rising edge of T2. (Figure 12.)

Figure 12. I/O Read and Write Cycles with $\overline{\text{IOC}} = 0$

HALT and Low-Power Operating Modes. The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{\text{HALT}}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{\text{HALT}}$, ST and $\overline{\text{M1}}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

OPERATION MODES (Continued)

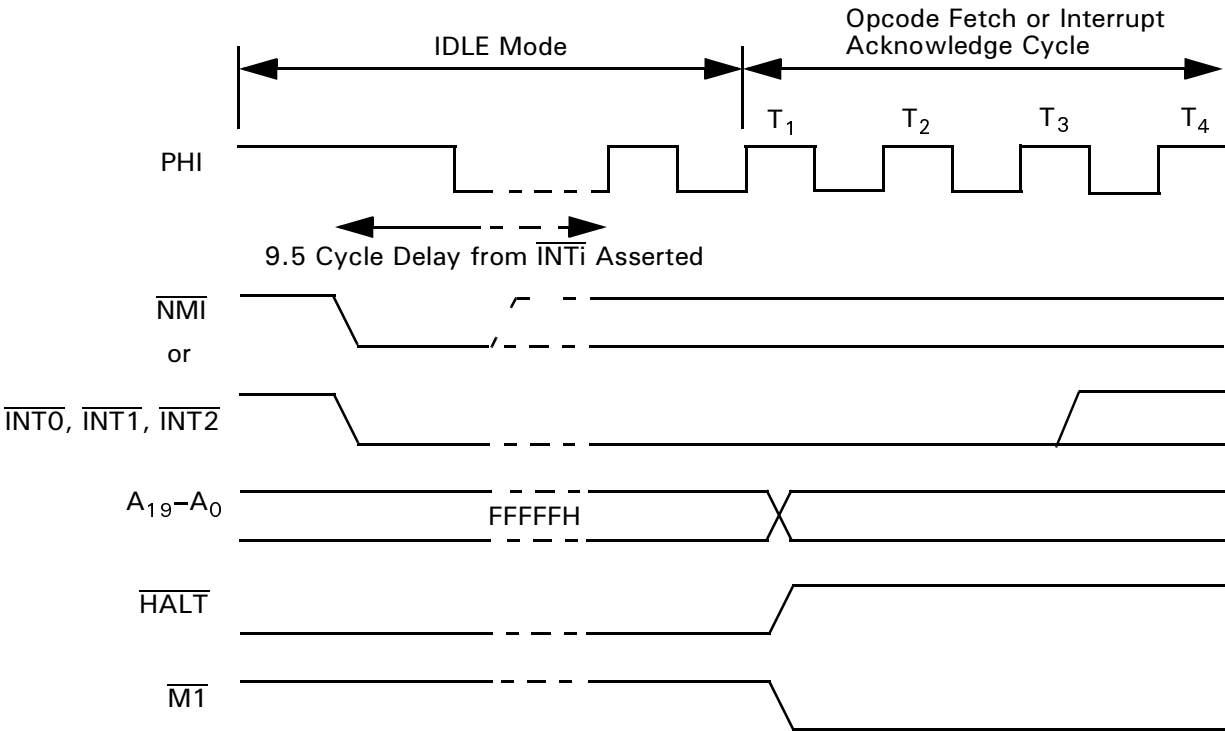


Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

Note: A response to a bus request takes 8 clock cycles longer than in normal operation.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

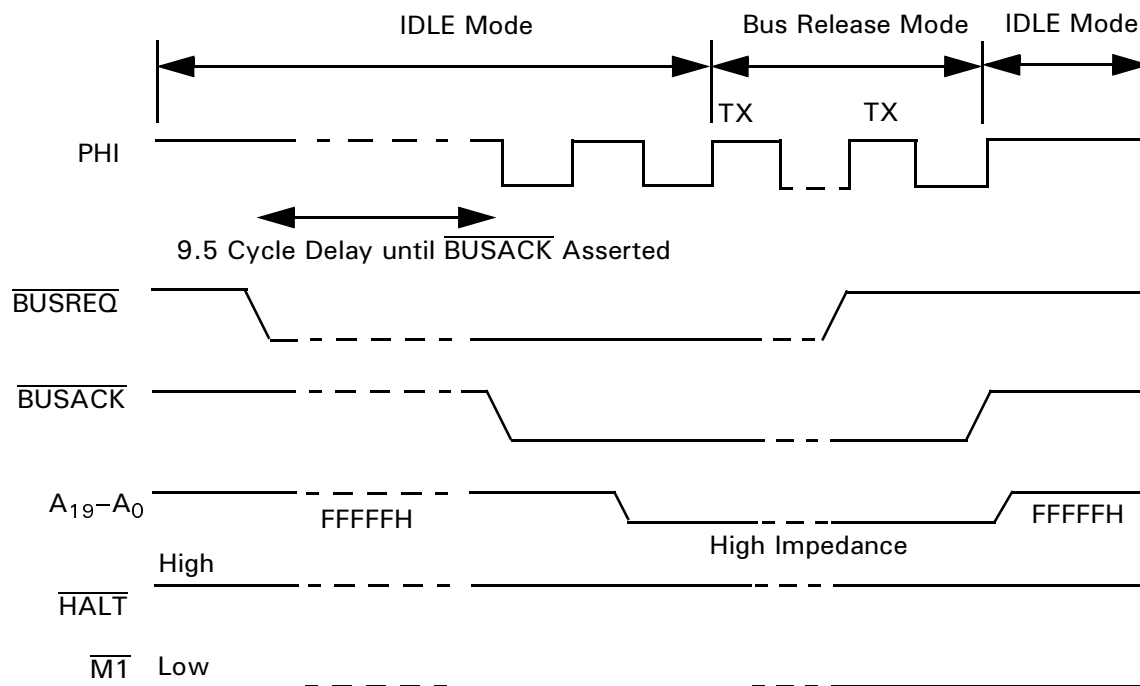


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10 μ A.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0-2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

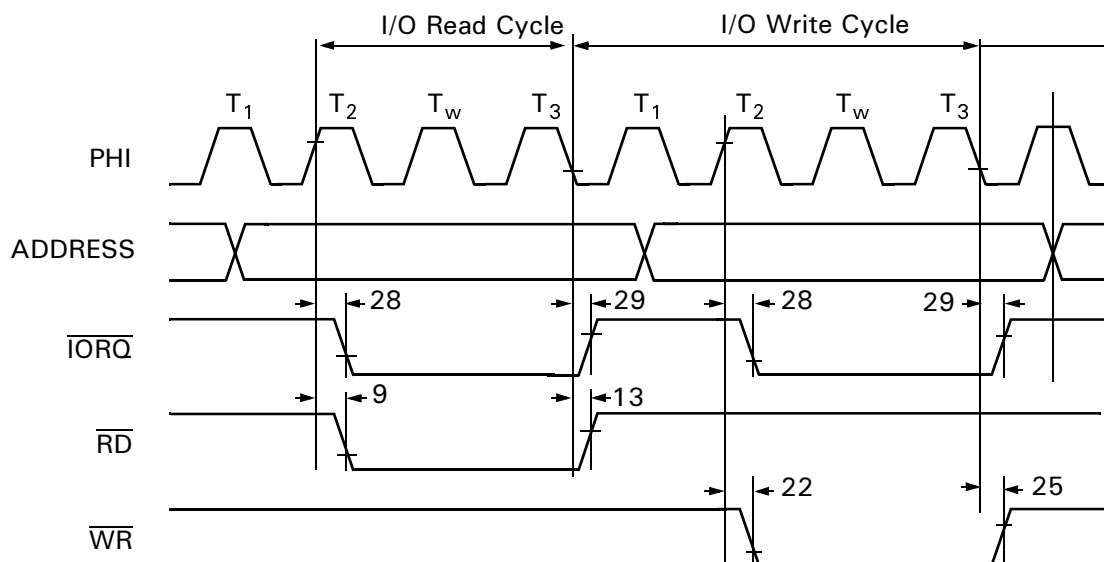
AC CHARACTERISTICS—Z8S180

Table 8. Z8S180 AC Characteristics

 $V_{DD} = 5V \pm 10\%$ or $V_{DD} = 3.3V \pm 10\%$; 33-MHz Characteristics Apply Only to 5V Operation

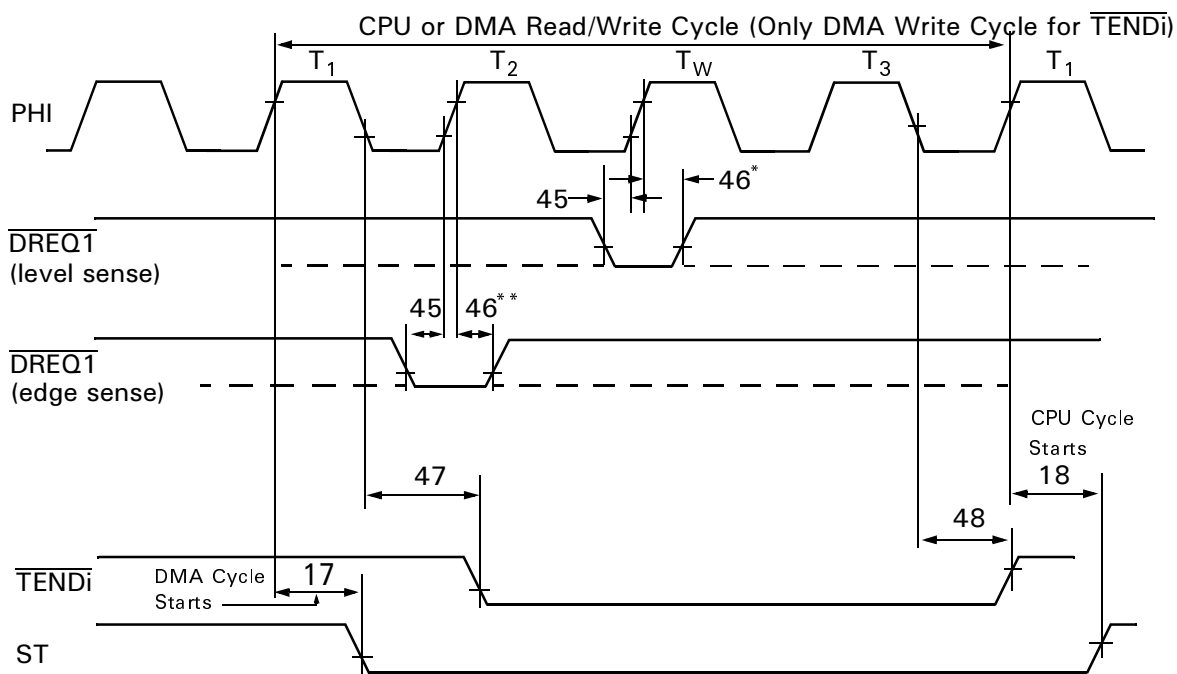
Number	Symbol	Item	Z8S180—20 MHz		Z8S180—33 MHz		Unit
			Min	Max	Min	Max	
1	t_{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t_{CHW}	Clock "H" Pulse Width	15	—	10	—	ns
3	t_{CLW}	Clock "L" Pulse Width	15	—	10	—	ns
4	t_{CF}	Clock Fall Time	—	10	—	5	ns
5	t_{CR}	Clock Rise Time	—	10	—	5	ns
6	t_{AD}	PHI Rise to Address Valid Delay	—	30	—	15	ns
7	t_{AS}	Address Valid to \overline{MREQ} Fall or \overline{IORQ} Fall)	5	—	5	—	ns
8	t_{MED1}	PHI Fall to \overline{MREQ} Fall Delay	—	25	—	15	ns
9	t_{RDD1}	PHI Fall to \overline{RD} Fall Delay $\overline{IOC} = 1$	—	25	—	15	ns
		PHI Rise to \overline{RD} Rise Delay $\overline{IOC} = 0$	—	25	—	15	
10	t_{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	—	15	ns
11	t_{AH}	Address Hold Time from \overline{MREQ} , \overline{IOREQ} , \overline{RD} , \overline{WR} High	5	—	5	—	ns
12	t_{MED2}	PHI Fall to \overline{MREQ} Rise Delay	—	25	—	15	ns
13	t_{RDD2}	PHI Fall to \overline{RD} Rise Delay	—	25	—	15	ns
14	t_{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	—	40	—	15	ns
15	t_{DRS}	Data Read Set-up Time	10	—	5	—	ns
16	t_{DRH}	Data Read Hold Time	0	—	0	—	ns
17	t_{STD1}	PHI Fall to ST Fall Delay	—	30	—	15	ns
18	t_{STD2}	PHI Fall to ST Rise Delay	—	30	—	15	ns
19	t_{WS}	\overline{WAIT} Set-up Time to PHI Fall	15	—	10	—	ns
20	t_{WH}	\overline{WAIT} Hold Time from PHI Fall	10	—	5	—	ns
21	t_{WDZ}	PHI Rise to Data Float Delay	—	35	—	20	ns
22	t_{WRD1}	PHI Rise to \overline{WR} Fall Delay	—	25	—	15	ns
23	t_{WDD}	PHI Fall to Write Data Delay Time	—	25	—	15	ns
24	t_{WDS}	Write Data Set-up Time to \overline{WR} Fall	10	—	10	—	ns
25	t_{WRD2}	PHI Fall to \overline{WR} Rise Delay	—	25	—	15	ns
26	t_{WRP}	\overline{WR} Pulse Width (Memory Write Cycle)	80	—	45	—	ns
26a		\overline{WR} Pulse Width (I/O Write Cycle)	150	—	70	—	ns
27	t_{WDH}	Write Data Hold Time from \overline{WR} Rise	10	—	5	—	ns
28	t_{IOD1}	PHI Fall to \overline{IORQ} Fall Delay $\overline{IOC} = 1$	—	25	—	15	ns
		PHI Rise to \overline{IORQ} Fall Delay $\overline{IOC} = 0$	—	25	—	15	
29	t_{IOD2}	PHI Fall to \overline{IORQ} Rise Delay	—	25	—	15	ns
30	t_{IOD3}	$\overline{M1}$ Fall to \overline{IORQ} Fall Delay	125	—	80	—	ns
31	t_{INTS}	\overline{INT} Set-up Time to PHI Fall	20	—	15	—	ns

TIMING DIAGRAMS (Continued)



CPU Timing ($\overline{I/O} = 0$)

Figure 22. CPU Timing ($\overline{I/O} = 0$)
(I/O Read Cycle, I/O Write Cycle)



Notes:

* T_{DRQS} and T_{DRQH} are specified for the rising edge of the clock followed by T_3 .

** T_{DRQS} and T_{DRQH} are specified for the rising edge of the clock.

Figure 23. DMA Control Signals

ASCI REGISTER DESCRIPTION

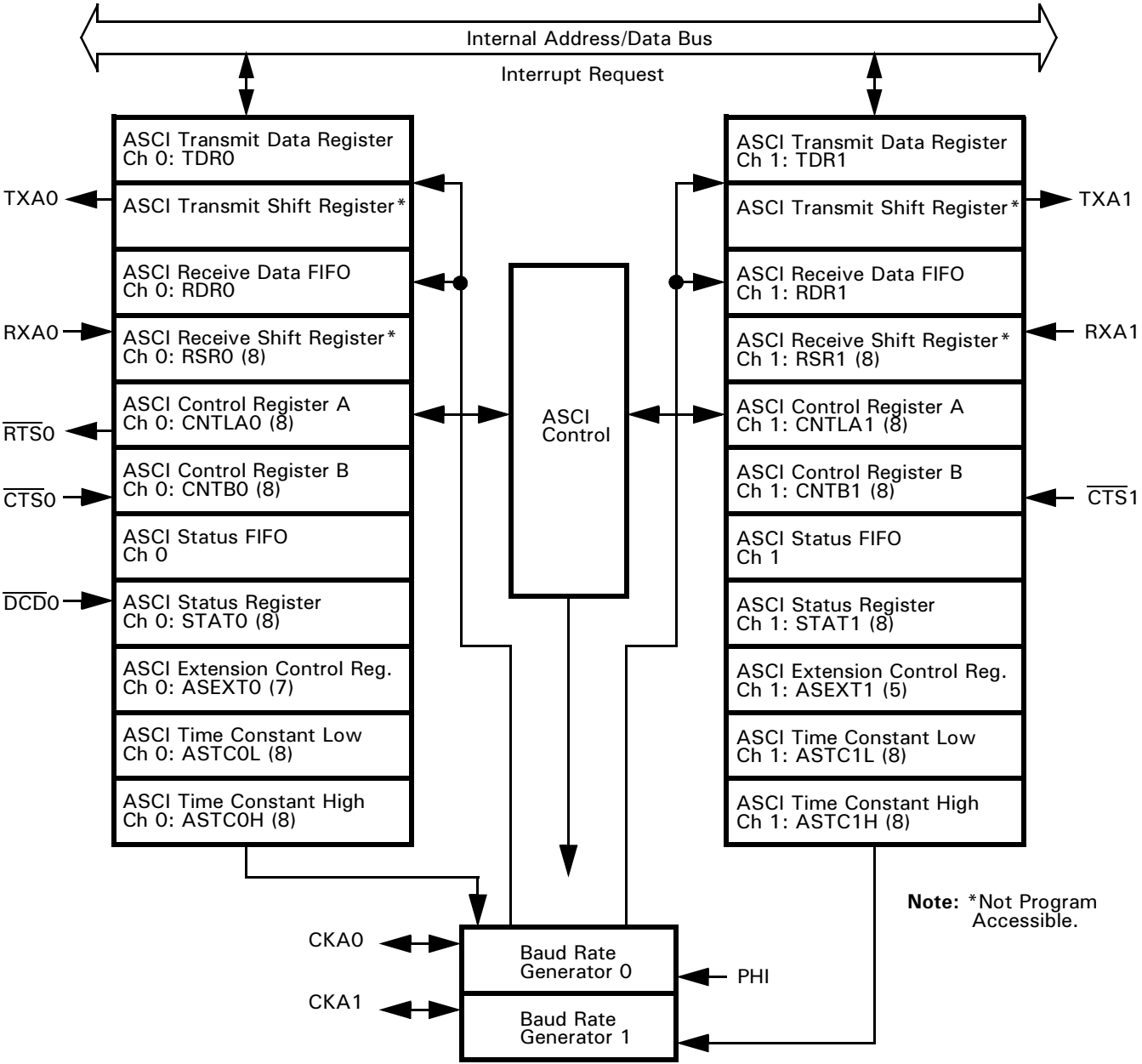


Figure 32. ASCI Block Diagram

ASCI Transmit Shift Register 0,1. When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for trans-

mission, TSR idles by outputting a continuous High level. This register is not program-accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

ASCI0 requests an interrupt when $\overline{\text{DCD0}}$ goes High. RIE is cleared to 0 by RESET.

$\overline{\text{DCD0}}$: Data Carrier Detect (Bit 2 STAT0). This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXTO register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

$\overline{\text{CTS1E}}$: Clear To Send (Bit 2 STAT1). Channel 1 features an external $\overline{\text{CTS1}}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

TDRE: Transmit Data Register Empty (Bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{\text{CTS0}}$ pin is auto-enabled in the ASEXTO register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (Bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0
Address 06H

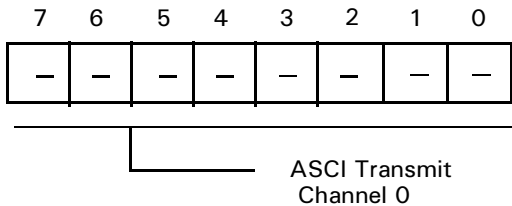


Figure 36. ASCII Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1
Address 07H

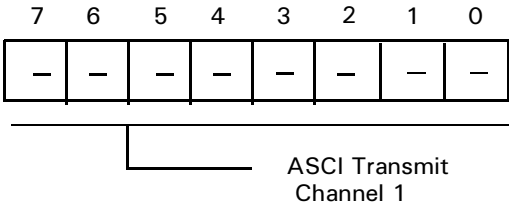


Figure 37. ASCII Register

ASCII EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1

The ASCII Extension Control Registers (ASEXT0 and ASEXT1) control functions that have been added to the

ASCIIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.

ASCII Extension Control Register 0 (ASEXT0 I/O Address = 12H)								
Bit	7	6	5	4	3	2	1	0
	Reserved	DCD0 Disable	CTS0 Disable	X1	BRG0 Mode	Break Enable	Break	Send Break

ASCII Extension Control Register 1 (ASEXT1 I/O Address = 13H)								
Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	X1	BRG1 Mode	Break Enable	Break	Send Break

Figure 47. ASCII Extension Control Registers, Channels 0 and 1

DCD0 Disable (Bit 6, ASCII0 Only). If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCII0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. If this bit is 1, the state of the $\overline{\text{DCD}}$ -pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

CTS0 Disable (Bit 5, ASCII0 Only). If this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCII0 transmitter, in that when the pin is negated/High, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTS0}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLB0 register.

X1 (Bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

BRG Mode (Bit 3). If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCII Baud Rate Generator

divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2–0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (Bit 2). If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

Break Detect (Bit 1). The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

Send Break (Bit 0). If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, bits 17–16 of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0 Low

Mnemonic SAR0L
Address 20H

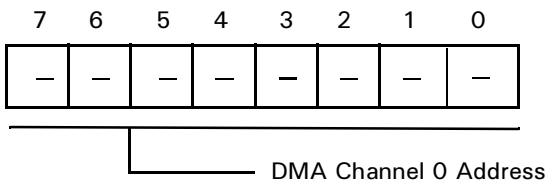


Figure 55. DMA Source Address Register 0 Low

DMA Source Address Register, Channel 0 High

Mnemonic SAR0H
Address 21H

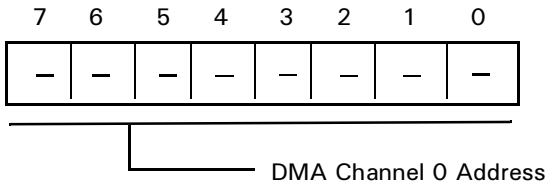


Figure 56. DMA Source Address Register 0 High

DMA Source Address Register Channel 0B

Mnemonic SAR0B
Address 22H

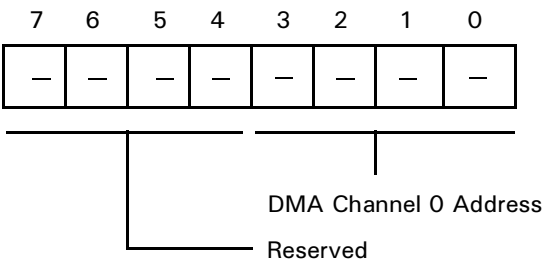


Figure 57. DMA Source Address Register 0B

If the source is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	RDRF (ASCIO)
1	0	RDRF (ASC11)
1	1	Reserved

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L
Address 23H

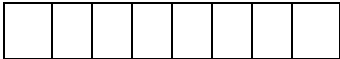


Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H
Address 24H



Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B
Address 25H

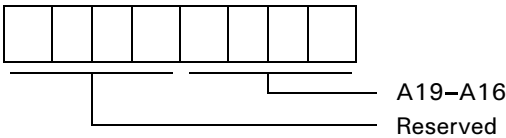


Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCII0)
1	0	TDR1 (ASCII1)
1	1	Not Used

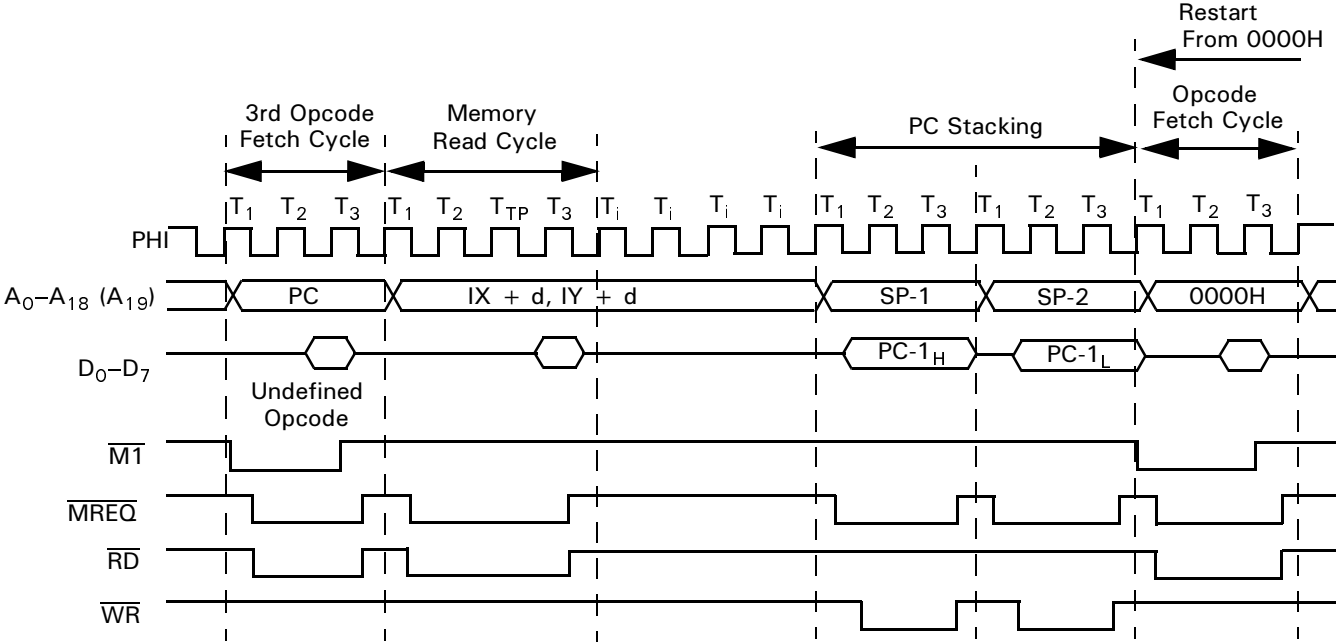


Figure 76. TRAP Timing—3rd Opcode Undefined

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG’s original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR
Address 3EH

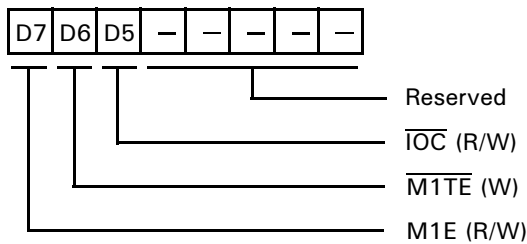


Figure 81. Operating Control Register
(OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When $M1E = 1$, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the \overline{NMI} acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When $M1E = 0$, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

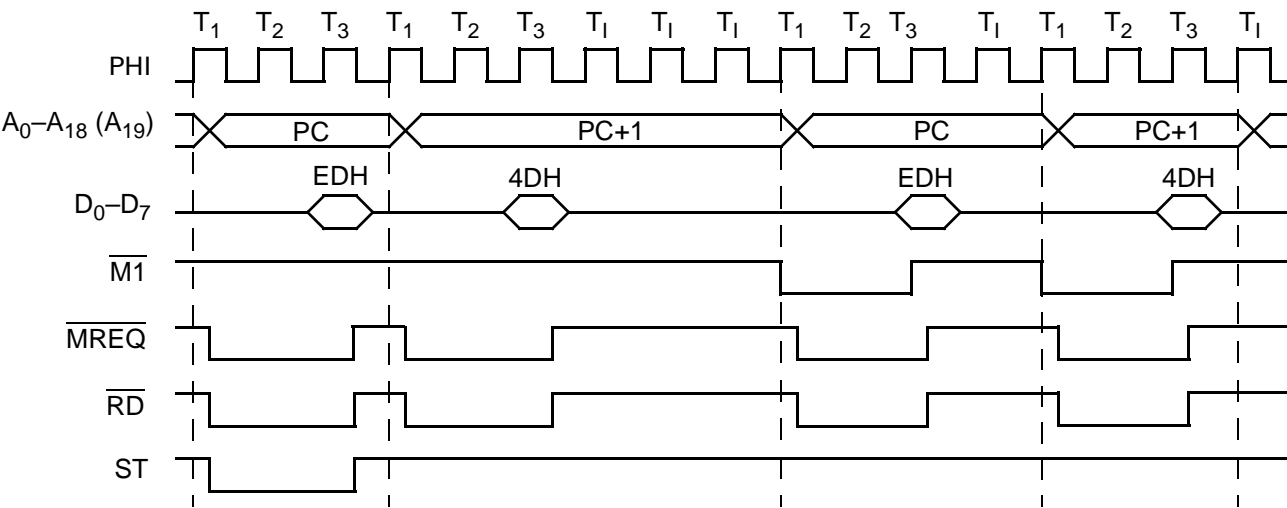


Figure 82. RETI Instruction Sequence with M1E = 0